Quiescent Current Control for the RF Integrated Circuit Device Family

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INTRODUCTION

This application note introduces a bias control circuit that can be used with the Freescale family of RF integrated circuits. The MHVIC915 device is used as an example in this paper, but the principle and theory of this controller can also be applied to other IC devices such as the MW4IC915, MWIC930, MW4IC2020, MW4IC2230 and MW5IC2030.

The quiescent current management of LDMOS devices has a strong effect on its performance because the critical RF performance parameters, such as intermodulation distortion products, are dependent on the quiescent current level [1]. The control goal of the bias circuitry is to maintain the quiescent current constant in all amplifier stages even if the environmental and device temperature changes significantly. Carefully selecting the control strategy will optimize the device's linearity performance and enable the built-in quiescent current thermal tracking circuit to work properly.

This application note examines the built-in quiescent current thermal tracking system characteristics of the MHVIC915 device and introduces several bias control strategies. Verifications of the typical circuit performance are also provided.

THERMAL TRACKING CIRCUIT

A typical LDMOS FET IV curve (Current, Drain-to-Source (I_{DS}) versus Voltage, Gate-to-Source (V_{GS})) relationship is shown in Figure 1. The gate leakage current of the traditional LDMOS device is very small (less than one micro amp).

In the MHVIC915 device, the gate current is relatively large due to the supply requirements of the built-in thermal tracking circuit (Figure 2). The thermal tracking circuit contains a thermal tracking transistor with its gate and drain connected together and its source connected to ground, along with several voltage settings and current limiting resistors. As a result of the additional components in this thermal tracking circuit, the gate current draw is in the milliamp range (not in the micro amp range) and follows the change of the drain current (Figure 3). The thermal tracking circuit is physically located on the die right next to the active RF LDMOS die area so its operating temperature is closely tied to that of the main amplifier circuit. The MHVIC915 has three major subcircuits, each with their own thermal tracking circuit:

- Bias reference FET for self-bias application
- Active RF LDMOS amplifier stage 1 driver section
- Stage 2 output section [2].

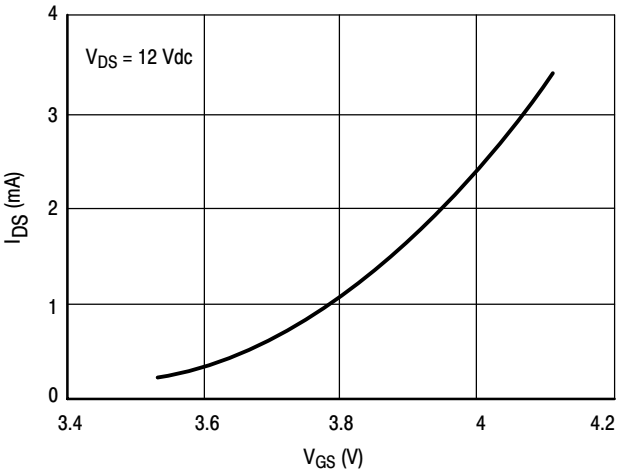

Figure 1. I_{DS} versus V_{GS}

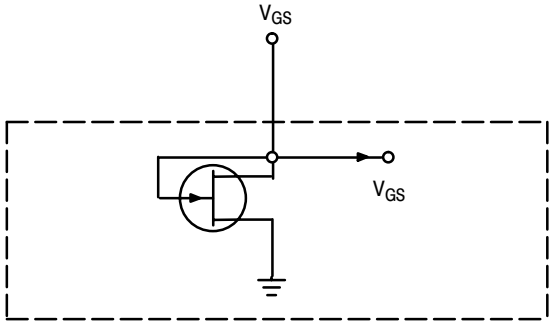

Figure 2. Thermal Tracking Circuit

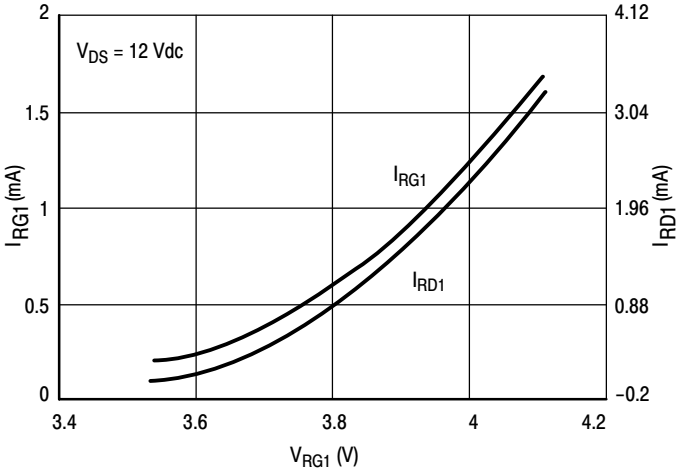

Figure 3. I_{RG1} and I_{RD1} versus V_{RG1}

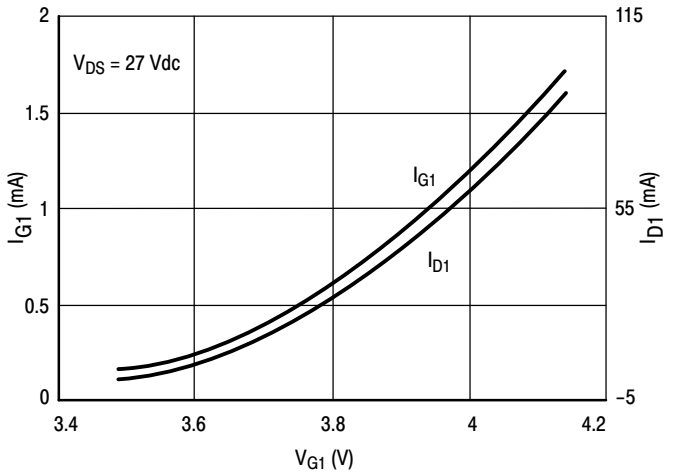

Figure 4. I_{G1} and I_{D1} versus V_{G1}

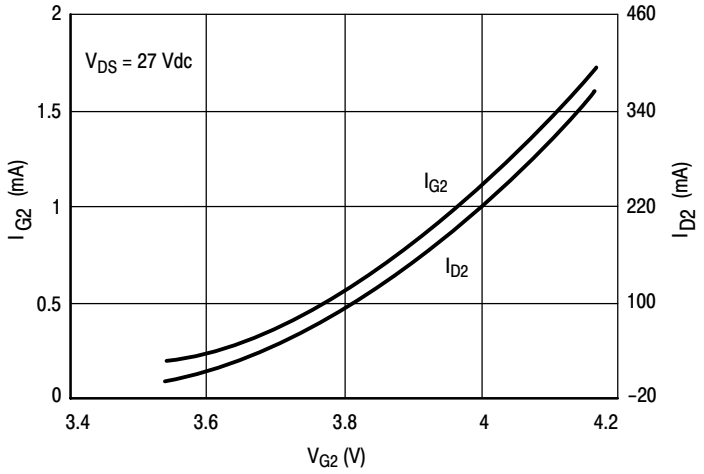

Figure 5. I_{G2} and I_{D2} versus V_{G2}

Figure 3 shows that IV curves for all of the FET structures are very similar. The current reference FET1 gate-to-source (I_{RG1}) and the current reference FET1 drain-to-source (I_{RD1}) curves are parallel when the scales are properly adjusted for the different device's periphery. This similarity also exists between the RF amplifier's stage 1 and stage 2 sections of the complete IC device as shown in Figures 4 and 5.

The thermal tracking circuits in the MHVIC915 are designed to compensate for the normal RF amplifier bias current changes over wide temperature variations. If a current source is supplied to the gate of the thermal tracking FET to set up the initial quiescent current bias setting, this FET draws a constant current and adjusts its gate voltage over a wide temperature range to maintain the constant drain current. This phenomena and the similarity of I_G and I_D allow for the ability to set the DC bias at each stage in terms of a constant gate current instead of constant gate voltage.

BIAS CONTROL CIRCUIT IMPLEMENTATION

The first step in the design of the power amplifier bias compensation circuit is to collect the values of each gate current, drain current and gate voltage for each stage of the device at a constant temperature. Table 1 lists the values for the MHVIC915.

Table 1. I_G and I_D versus V_G at Each Stage

V_G (V)	I_G (mA)	I_{RD1} (mA)	I_{D1} (mA)	I_{D2} (mA)
		V_{RD1} = 12 V	V_{D1} = 27 V	V_{D2} = 27 V
3.53	0.10	0.22	4.62	26.1
3.64	0.20	0.45	10.8	50.6
3.70	0.30	0.66	16.8	74.9
3.76	0.40	0.87	23.3	100
3.81	0.50	1.09	30.0	123
3.84	0.60	1.30	36.0	148
3.88	0.70	1.51	42.4	171
3.91	0.80	1.73	48.9	197
3.94	0.90	1.95	55.1	220
3.97	1.00	2.17	61.3	246
3.99	1.10	2.37	67.5	268
4.02	1.20	2.59	73.8	290
4.05	1.30	2.80	79.9	313
4.07	1.40	3.00	86.1	340
4.09	1.50	3.23	91.0	365
4.11	1.60	3.44	98.2	395

The next step is to select the desired drain current per stage (I_{D1} and I_{D2}) depending on the desired operating condition or end use application. For this application note designed around the MHVIC915, the optimum CDMA performance levels are achieved with V_{DS1} = 12 Volts and I_{DQ1} = 80 mA and V_{DS2} = 27 Volts and I_{DQ2} = 120 mA. The data in Table 1 shows that those individual stage bias settings are associated with the bias FET tracking setting of I_{G1} = 1.30 mA and I_{G2} = 0.50 mA. Note that the stage 1 RF amplifier section is biased at a higher milliamp per millimeter periphery ratio and closer toward Class A operation so that it will have a minimal distortion contribution to the overall device performance. This is why it requires a higher reference FET bias setting current than does the output stage.

For convenience, I_{RG1} was selected to equal the I_{G2} value. Other values could have been chosen as well, as long as the I_{RD1} value is within the limits of the specifications defined in the data sheet. Once the I_{BRG1} value is selected, the I_{RD1} value is fixed according to the choice of I_{RG1}.

Figure 6 shows one example of a voltage source, active bias compensation controller circuit [3] in conjunction with the MHVIC915 746-960 MHz test circuit. All component values are listed in Table 2. The active bias compensation circuit, in conjunction with the built-in bias reference FET inside the MHVIC915, form the self bias setting control system. The bias reference FET is an added silicon die feature that was built into this family of devices using a uniform wafer fabrication layout and assembly process across the entire die area. The I_G and I_D versus V_{GS} characteristic of the bias reference FET should be equivalent to the I_G and I_D versus V_{GS} characteristics of the rest of the RF LDMOS FETs that are used in the amplifier stages 1 and 2. The similarity of I_G versus I_D curves across the entire die, including the bias reference FET and all of the subsequent gain stages of the device, allows the use of one reference FET to set and control the biasing of all stages, even though the temperature compensation is performed on a per stage basis. To prevent the sensing resistor value from impacting the drain currents on the rest of the gain stages, the value of the drain resistor (R6) on the bias reference FET circuit was set based on the desired I_{RD1} value. The other control voltages were selected per Table 1.

CIRCUIT ACCURACY

The functionality of the active bias compensation circuit is to set up the optimal bias in the bias reference FET circuit [3] according to the characterization data listed in Table 1. The selected drain current of the bias reference FET is set by the D1 and R6 components in the circuit. The controller circuit senses the drain quiescent current of the bias reference FET and adjusts the bias voltage accordingly to maintain the optimal selected drain current value. Two voltage dividers, formed by R14/R15 and R16/R17, are configured to adjust the bias voltages of stages 1 and 2 of the amplifier. These resistor divider networks are designed to take into account the expected gate current flow for each stage using the data listed in Table 1. All of the important gate currents (I_{RG1}, I_{G1} and I_{G2}) are set by the node voltage at the connection of R12, R14 and R16. Figure 6 shows a relatively simple, well performing circuit with a minimum of components but with a limitation in bias setting accuracy of about ±10%. More complex circuits can be used to improve on this bias setting accuracy.

A current source bias controller is shown in Figure 7 as an alternative. The components are listed in Table 3. A two-stage current source controller replaces the voltage dividers of the previous example. The bias control system now has three sections: the active bias compensation circuit, the current source controller and the bias reference FET. The design process begins with the selection of the desired stage drain currents, I_{D1} and I_{D2}, and the corresponding I_{G1} and I_{G2} from Table 1 is then identified.

The I_{RG1} value that was selected is close to the I_{G2} value for convenience and circuit simplicity. I_{RD1} is fixed by the corresponding selection of I_{RG1} from Table 1. The two-stage current controller sets the gate currents proportionally between the two RF LDMOS amplifier stages. R12 and R13 set the ratio of I_{G1} and $I_{RG1} + I_{G2}$. I_{RG1} and I_{G2} are set nearly equal. (Otherwise, two emitter resistors are required to set up the current ratio.) The drain resistor (R6) of the bias reference FET feed circuit was selected based on the I_{RD1} values from the table and the control voltage at D1. The collector current from Q1 splits three ways according to the ratio set by the current source bias controller.

The circuit in Figure 7 is slightly more complex than the example shown in Figure 6, but the added complexity pays off in better bias setting accuracy. This circuit is capable of setting the typical bias within a ±7% accuracy window.

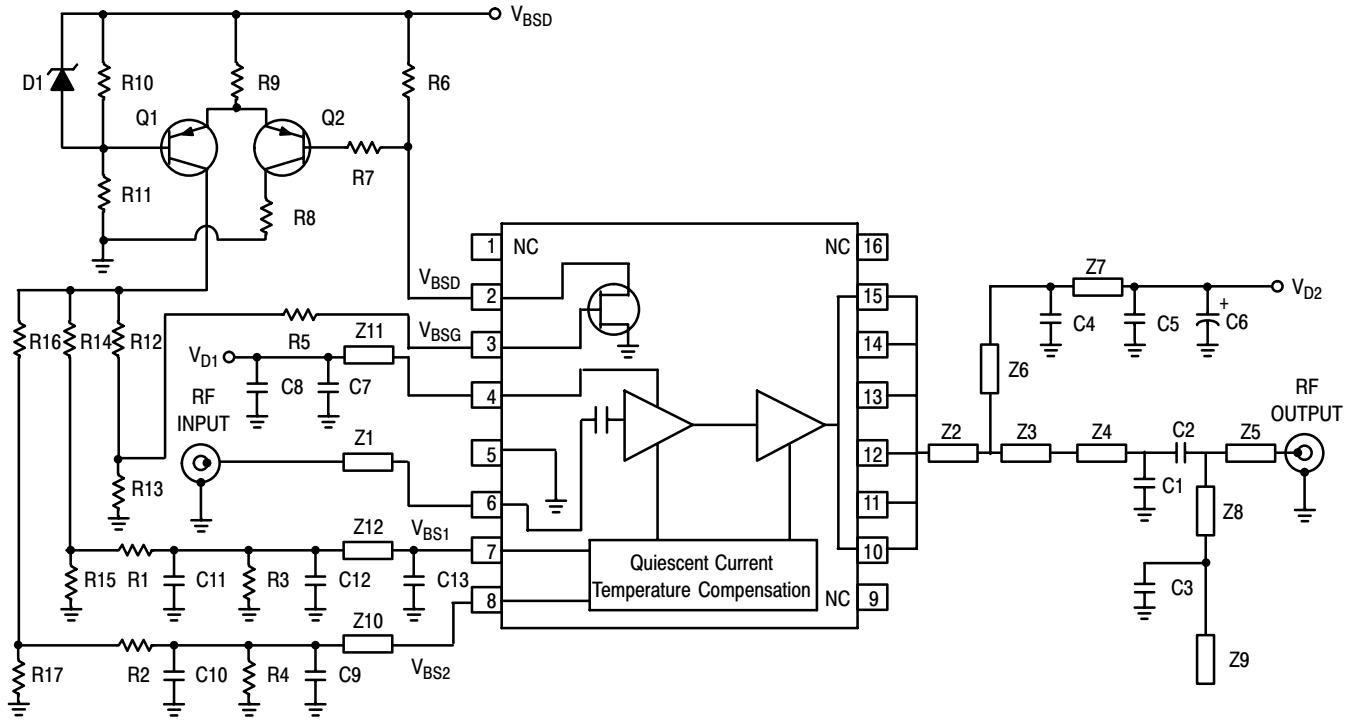

Figure 6. Active Bias Compensation Controller

Table 2. Active Bias Compensation Controller Component List (MHVIC915 746-960 MHz RF LDMOS Power Amplifier)

Parts	Description
C1,C2	4.7 pF High Q ATC Capacitors (0603)
C3,C4	47 pF NPO Capacitors (0805)
C5,C8,C10,C11	1 μFX7R chip Capacitors (1214)
C6	10 μF, 50 V Electrolytic Capacitor
C7,C9,C12	0.01 μFX7R Chip Capacitors (0805)
C13	8.2 pF NPO Chip Capacitor (0805)
D1	250 mW, 15.3 V Zener Diode
Q1,Q2	BC857ALT1, ON Semiconductor (SOT-23)
R1,R2,R5	1 kΩ Chip Resistors (0603)
R3,R4	100 kΩ Chip Resistors (0603)
R6,R15	15 kΩ Chip Resistors (0805)
R7	510 Ω Chip Resistors (0805)
R8	5.1 kΩ Chip Resistors (0805)
R9	3 kΩ Chip Resistors (0805)
R10	16 kΩ Chip Resistors (0805)
R11	8.2 kΩ Chip Resistors (0805)
R12,R16	10 kΩ Chip Resistors (0805)
R13,R17	18 kΩ Chip Resistors (0805)
R14	3.6 kΩ Chip Resistors (0805)

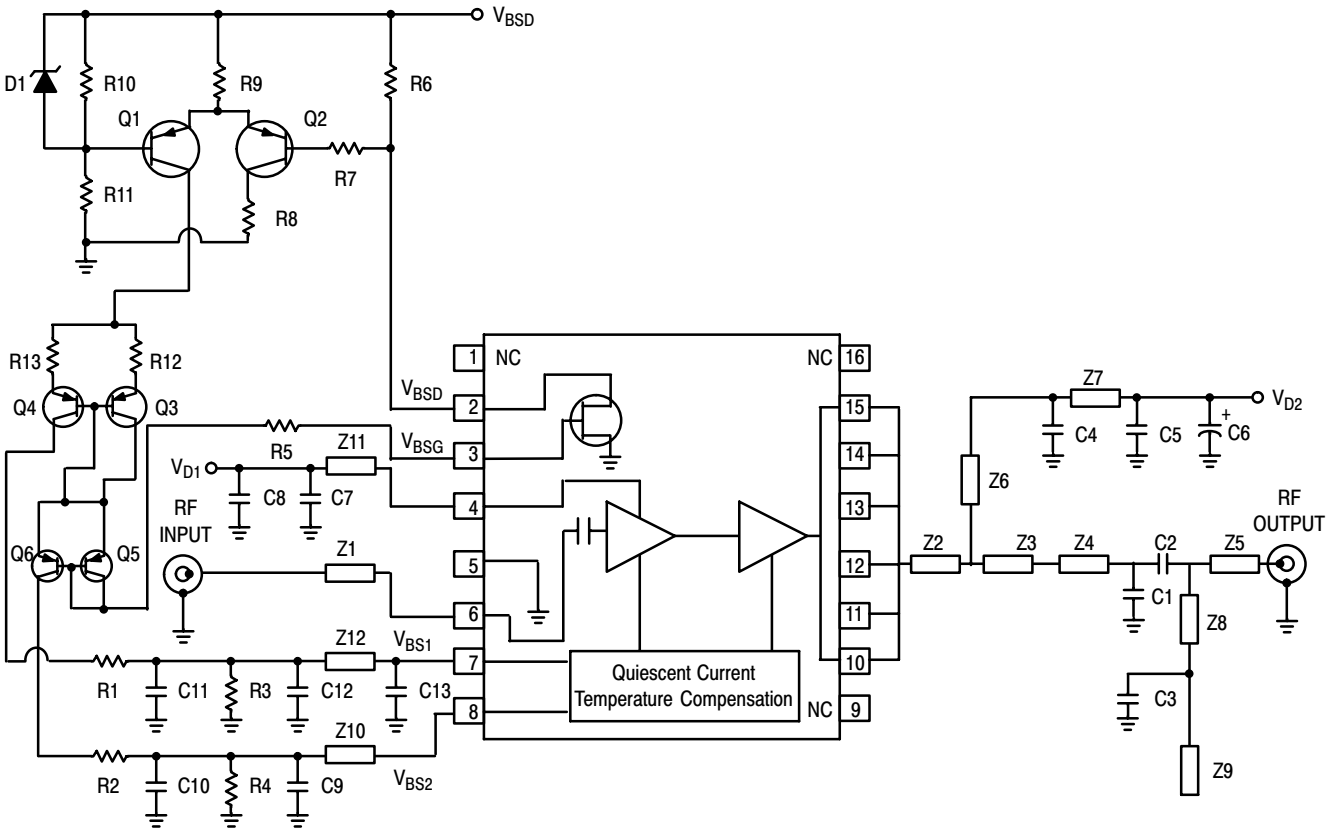

Figure 7. Current Source Bias Controller

Table 3. Current Source Bias Controller Component List (MHVIC915 746-960 MHz RF LDMOS Power Amplifier)

Parts	Description
C1,C2	4.7 pF High Q ATC Capacitors (0603)
C3,C4	47 pF NPO Capacitors (0805)
C5,C8,C10,C11	1 μFX7R chip Capacitors (1214)
C6	10 μF, 50 V Electrolytic Capacitor
C7,C9,C12	0.01 μFX7R Chip Capacitors (0805)
C13	8.2 pF NPO Chip Capacitor (0805)
D1	250 mW, 15.3 V Zener Diode
Q1-Q6	BC857ALT1, ON Semiconductor (SOT-23)
R1,R2,R5	1 kΩ Chip Resistors (0603)
R3,R4	100 kΩ Chip Resistors (0603)
R6,R10	16 kΩ Chip Resistors (0805)
R7	510 Ω Chip Resistors (0805)
R8	5.1 kΩ Chip Resistors (0805)
R9	3 kΩ Chip Resistors (0805)
R11	8.2 kΩ Chip Resistors (0805)
R12	1.6 kΩ Chip Resistors (0805)
R13	1.2 kΩ Chip Resistors (0805)

Table 4. Active Bias Compensation Controller Data

Index	I_{RG1}	I_{G1}	I_{G2}	I_{RD1}	I_{D1}	I_{D2}
Lot1-1	0.45	1.26	0.45	1.02	79.7	121
Lot1-2	0.45	1.24	0.44	1.03	77.1	119
Lot1-3	0.46	1.28	0.46	1.02	79.5	125
Lot1-4	0.48	1.32	0.48	1.02	83.0	128
Lot1-5	0.45	1.25	0.44	1.02	78.4	116
Lot2-1	0.44	1.22	0.44	1.02	78.3	117
Lot2-2	0.46	1.27	0.46	1.02	83.7	124
Lot2-3	0.43	1.19	0.42	1.02	76.7	117
Lot2-4	0.45	1.25	0.45	1.02	81.1	124
Lot2-5	0.43	1.21	0.43	1.02	78.4	114
Lot3-1	0.45	1.24	0.44	1.02	77.4	119
Lot3-2	0.45	1.24	0.44	1.02	78.9	125
Lot3-3	0.45	1.24	0.45	1.02	78.0	117
Lot3-4	0.45	1.25	0.44	1.02	75.6	120
Lot3-5	0.45	1.26	0.45	1.02	82.3	119
Avg	0.45	1.25	0.45	1.02	79.2	120
Min	0.43	1.19	0.42	1.02	75.6	114
Min(%)	-4.4	-4.6	-5.8	-0.3	-4.6	-5.2
Max	0.48	1.32	0.48	1.03	83.7	128
Max(%)	6.7	5.8	7.6	0.4	5.7	6.7
Var	-	-	-	-	5.6	17.0
Var(%)	-	-	-	-	7.1	14.1

Table 5. Current Source Bias Controller

Index	I_{RG1}	I_{G1}	I_{G2}	I_{RD1}	I_{D1}	I_{D2}
Lot1-1	0.51	1.27	0.45	1.14	80.5	123
Lot1-2	0.51	1.26	0.45	1.16	78.4	122
Lot1-3	0.51	1.28	0.46	1.13	79.7	125
Lot1-4	0.52	1.29	0.46	1.1	81.8	125
Lot1-5	0.51	1.07	0.45	1.15	79.9	119
Lot2-1	0.5	1.26	0.45	1.17	80.6	121
Lot2-2	0.51	1.27	0.46	1.13	84.0	124
Lot2-3	0.51	1.27	0.45	1.15	79.4	119
Lot2-4	0.51	1.27	0.45	1.15	82.6	126
Lot2-5	0.5	1.25	0.45	1.18	81.0	118
Lot3-1	0.51	1.27	0.45	1.16	79.0	121
Lot3-2	0.51	1.26	0.45	1.15	80.8	128
Lot3-3	0.5	1.24	0.45	1.19	80.1	123
Lot3-4	0.51	1.26	0.45	1.15	76.4	122
Lot3-5	0.51	1.27	0.46	1.15	83.3	120
Avg	0.51	1.25	0.45	1.15	80.5	122
Min	0.50	1.07	0.45	1.10	76.4	118
Min(%)	-1.7	-14.6	-0.6	-4.4	-5.1	-3.3
Max	0.52	1.29	0.46	1.19	84.0	128
Max(%)	2.2	3.0	1.6	3.4	4.3	4.8
Var	-	-	-	-	3.7	8.4
Var(%)	-	-	-	-	4.6	6.9

CIRCUIT CHARACTERIZATION

The active bias compensation controller in Figure 6 was designed based on the reference data in Table 1 that was collected on a set of typical MHVIC915 devices. The similarities of the I_G versus V_{GS} curves among bias reference FET and the other on-die amplifier stages is expected, but they are not necessarily perfectly matched. Process variations, on-die thermal gradients and component tolerances all tend to add variability to the overall bias setting accuracy of this circuit-device combination. To fully characterize the circuit's bias setting capability, five components were tested, each from three different production wafer lots in an effort to estimate the variations of MHVIC915 devices in one fixed-value circuit. The results of this study are tabulated in Table 4.

From Table 4, the average values for the drain currents V_{D1} and V_{D2} are 79.2 mA and 120 mA, respectively. These values are very close to the design targets of 80 mA and 120 mA. The maximum value of V_{D1} is 83.7 mA, or a 5.7% deviation from the average. The maximum value of V_{D2} is 128 mA, or a 6.7% deviation from the average. Given that a 15% variation in bias setting is needed to significantly alter the RF performance characteristics of the device, this circuit should be adequate for most applications.

The same five devices, each from three different wafer lots, were also tested in the alternative current source bias controller circuit shown in Figure 7. This circuit controls the drain currents by adjusting the gate currents instead of gate voltages. The similarities of the I_G versus V_{GS} properties at all stages is expected to be equal, but the same production variables still apply. Table 5 lists the performance and bias setting accuracy of the current source bias controller using the same 15 devices, in the same sequence, that generated the active bias compensation controller data listed in Table 3.

The average values of drain currents V_{D1} and V_{D2} are 80.5 mA and 122 mA, respectively, and are very close to the targeted design values 80 mA and 120 mA. The maximum value of V_{D1} is 84 mA, or a 4.3% deviation from the average. The maximum value of V_{D2} is 128 mA, or a 4.8% deviation from the average.

Compared to the results of the active bias compensation controller in Figure 6, the quiescent drain currents of the current source bias controller has less variance by about one or two percentage points. The current source bias controller circuit also takes full advantage of the thermal tracking transistor to keep the gate/drain currents maintain constants.

Note that the variation of I_{D1} and I_{D2} in Tables 4 and 5 are mainly to the internal variations of the devices, i.e., the

variations I_D versus V_{GS} curve from device to device. Other variations, such as I_G versus V_{GS} curve of the same device, could also contribute to the bias setting tolerance capability. Figure 8 shows variations between I_{RG1}, I_{G1} and I_{G2} for one typical MHVIC915 device.

The circuit components also have strong influences on the bias setting tolerance. The precision of the bias sensing drain resistor (R6) affects the overall drain current tolerance of the controller, as does the reference voltage provided by D1. To reduce the bias setting tolerance, the same type of PNP transistors are recommended for both Q1 and Q2.

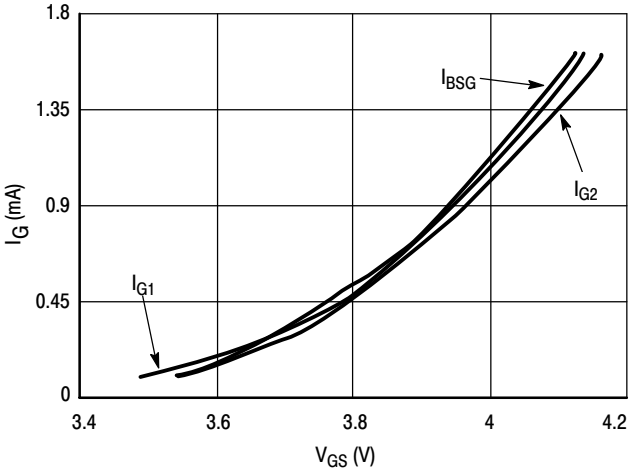

Figure 8. I_{G1}, I_{G2} and I_{BSG} versus V_G

SUMMARY

These newly developed RF power IC bias controller circuits are intended to set the optimized drain quiescent currents for these multi-stage amplifier devices without the need for any external adjustments. A fixed-tune circuit for both the DC and RF sections is now possible. These circuits take full advantage of the on-die temperature compensation circuits built into the devices and produce relatively constant bias settings across the full production device variation range and the expected temperature operating range.

REFERENCES

1. Freescale Application Note AN1977, *Quiescent Current Thermal Tracking Circuit in RF Integrated Circuit Family*. Pascal Gola, Antoine Rabany, Samay Kapoor and David Maurin.
2. MHVIC915R2, *The RF Line 746-960 MHz RF LDMOS Wideband Integrated Power Amplifier.* Freescale Semiconductor Technical Data Sheet.
3. Amplifier with Active Bias Compensation and Method for Adjusting Quiescent Current. Daniel Brayton, U.S. Patent No. 6046642.

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