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SGA-8343 GPS Application Circuits

RFMD Worldwide Applications
Design Application Note -- AN-061

Abstract

RFMD's SGA-8343 is a high performance SiGe amplifier designed for operation from DC to 6GHz. This application note illustrates application circuits for GPS (Global Positioning System) frequency band (1575MHz). The first application circuit is optimized for noise performance; the second one is optimized for input return loss. Introduction The application circuits were designed to achieve the optimum combination of NF, input return loss, and stability. All recommended components are standard values available from well-known manufacturers. Components specified in the bill of materials (BOM) have known parasitics which in some cases are critical to the circuit's performance. Deviating from the recommended BOM may result in a performance shift due to varying parasitics. Matching component placement is critical to each circuit's performance.

Circuit Details

SMDI will provide the detailed layout (AutoCAD format) to users wishing to use the exact same layout and PCB material shown in the following circuits. The circuits recommended within this application note were designed using the following PCB stack up:

Material: GETEKTM ML 200C

Core thickness: 0.031"

Copper cladding: 1 oz. both sides

Dielectric constant: 4.1

Dielectric loss tangent: 0.0089 (at 1GHz)

Customers not wishing to use the exact material and layouts shown in this application note can design their own PCB using the critical transmission line impedances and phase lengths shown in the BOMs and layouts.

NOTE: Many of our sample evaluation boards may come with an additional substrate and copper layer for mechanical stability. It has been assumed that the backside layer has no effect on the RF performance or circuit design.

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Design Considerations and Trade-Offs - Biasing Techniques

All HBT amplifiers are subject to device current variation due to the decreasing nature of the internal VBE with increasing temperature. In the absence of an active bias circuit or resistive feedback, the decreasing VBE will result in increased base and collector currents. As the collector current continues to increase under constant VCE conditions, the device may eventually exceed its maximum dissipated power limit resulting in permanent device damage. The designs included in this application note contain passive bias circuits that stabilize the device current over temperature and desensitize the circuit to device process variation. The passive bias circuits used in these designs include a dropping resistor in the collector bias line and a voltage divider from the collector-to-base. Using this scheme, the amplifier can be biased from a single supply voltage. The collector dropping resistor is sized to drop >20% VCE, depending on the desired VCE. The voltage divider from collector-to-base, in conjunction with the dropping resistor, will stabilize the device current over temperature. The effectiveness increases with increasing voltage drop in collector bias line. Configuring the voltage divider such that the shunt current is 5-10 times larger than the desired base current desensitizes the circuit to beta variation. These two feedback mechanisms are sufficient to insure consistent performance over temperature and device process variations. Note that the voltage drop is clearly dependent on the nominal collector current and can be adjusted to generate the desired VCE from a fixed supply rail. The user should test the circuit over the operational extremes to guarantee adequate performance. An active bias circuit can be implemented if the user does not wish to sacrifice the voltage required by the aforementioned passive circuit. There are various active bias schemes suitable for HBTs. The user should choose an active bias circuit that best meets his/her cost, complexity, and performance requirements.

Other Application Circuits Available (see AN-044)

1. 800MHz to 1000MHz, single-ended with series feedback, optimized for NF and S11<-10dB.
2. 1800MHz to 2000MHz, single ended, optimized for NF and S11<-8dB.
3. 2400MHz to 2500MHz, single-ended, optimized for NF and S11<-10dB.

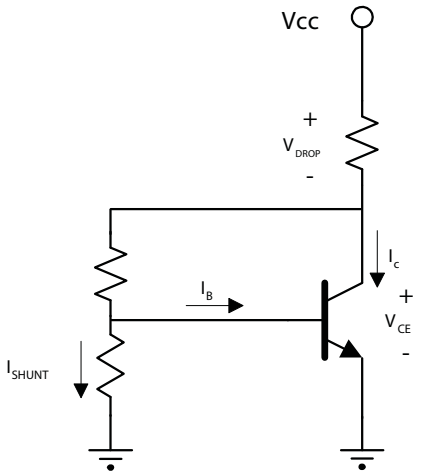

Figure 1. Passive Bias Circuit Topology

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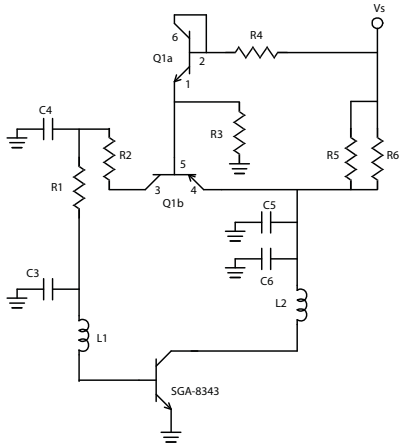
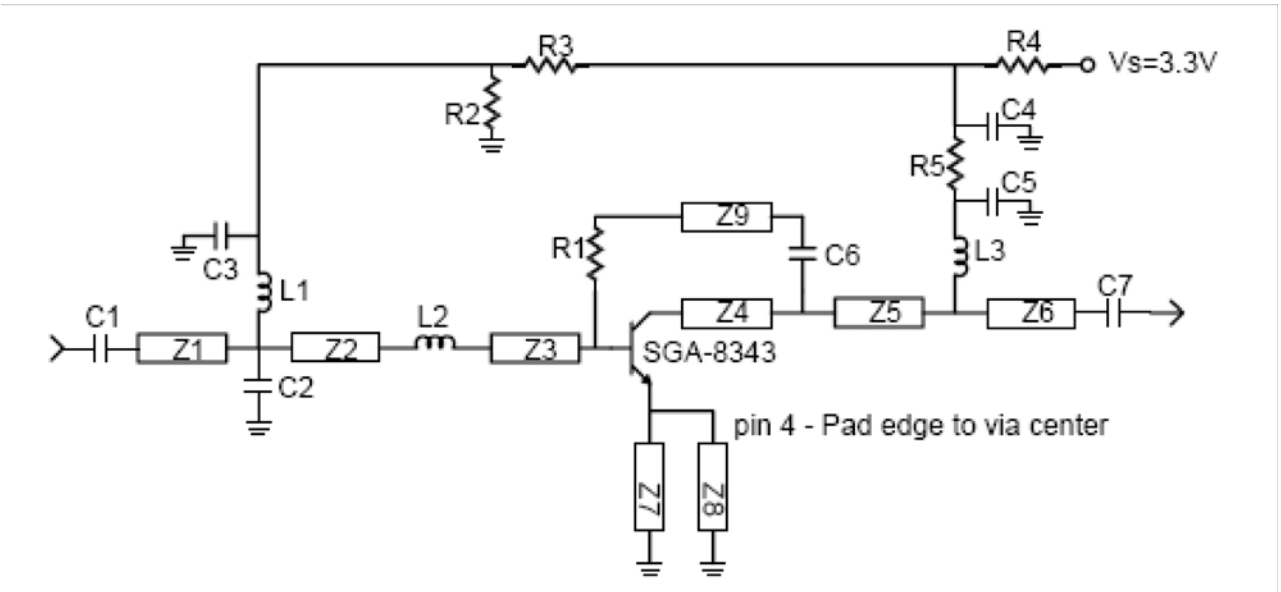


Figure 2. Active Bias Circuit Topology

SGA-8343(Z)-EVB4 1575 MHz Application Schematic



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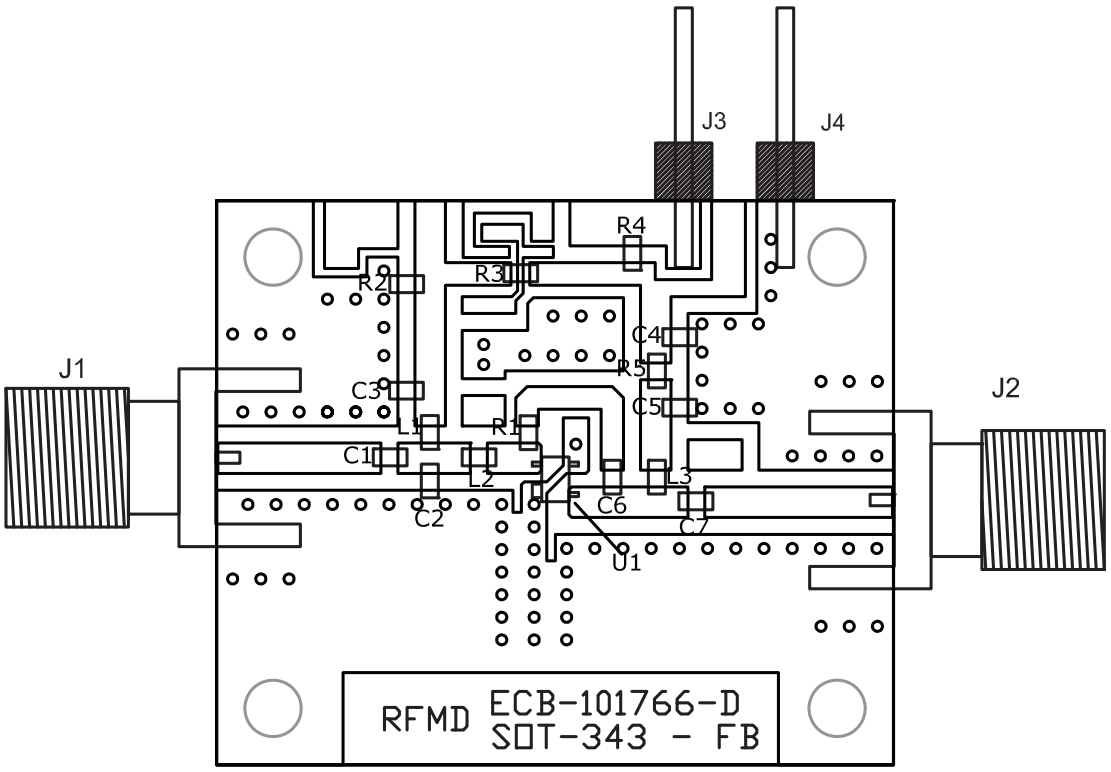
SGA-8343(Z)-EVB4 1575MHz Evaluation Board



Ref. Des	Part Number	Value
C1, 5, 7	ROHM MCH185A150J	15pF
C2	ROHM MCH185A1R2C	1.2pF
C3, 4, 6	Samsung CL 10B104KONC	0.1uF
L1	TOKO LL 1608-FS39NJ	39nH
L2	TOKO LL 1608-FS1N8S	1.8nH
L3	TOKO LL 1608-FS3N9S	3.9nH
R1, 3	ROHM MCR03J222	2.2KΩ
R2	ROHM MCR03J102	1.0KΩ
R4	ROHM MCR03J620	62Ω
R5	ROHM MCR03J100	10Ω
Z1	non-critical	50Ω
Z2	6.5 degrees at 1575MHz	50Ω
Z3	7.8 degrees at 1575MHz	50Ω
Z4	6.4 degrees at 1575MHz	50Ω
Z5	6.4 degrees at 1575MHz	50Ω
Z6	non-critical	50Ω
Z7	11.1 degrees at 1575MHz	50Ω
Z8	6.3 degrees at 1575MHz	50Ω
Z9	26.0 degrees at 1575MHz	60Ω

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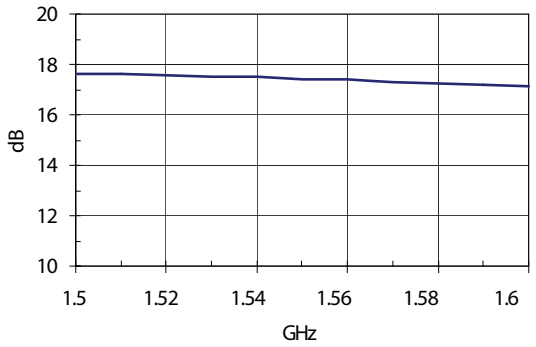
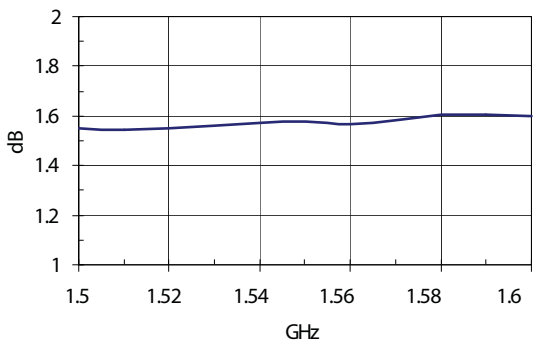
Typical Performance: Optimal S11 Application Circuit (V_S=3.3V, I_{CQ}=10mA, 25C)

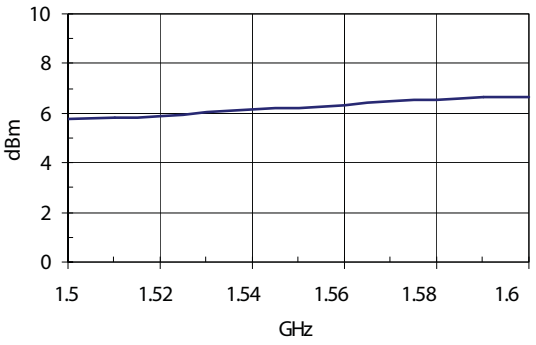
Gain vs. Frequency



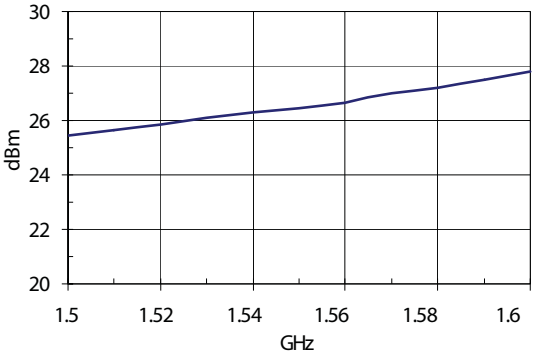
NF vs. Frequency



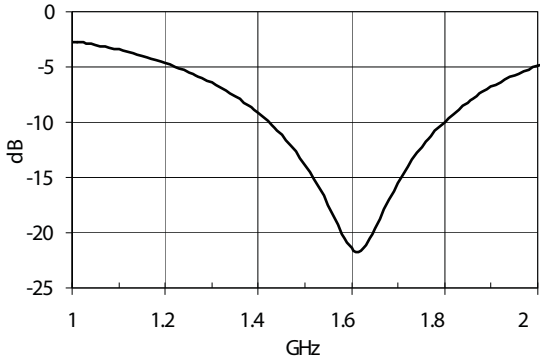
P1dB vs. Frequency



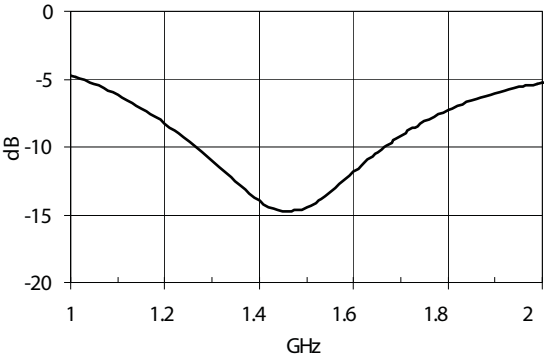
OIP3 vs. Frequency



S11 vs. Frequency



S22 vs. Frequency



Freq (GHz)	P1dB (dBm)	OIP3 (dBm)	Gain (dB)	S11 (dB)	S22 (dB)	NF (dB)
1.550	6.2	26.5	17.4	-17	-13	1.6
1.575	6.5	27.0	17.3	-20	-12	1.6
1.600	6.6	27.8	17.1	-21	-12	1.6

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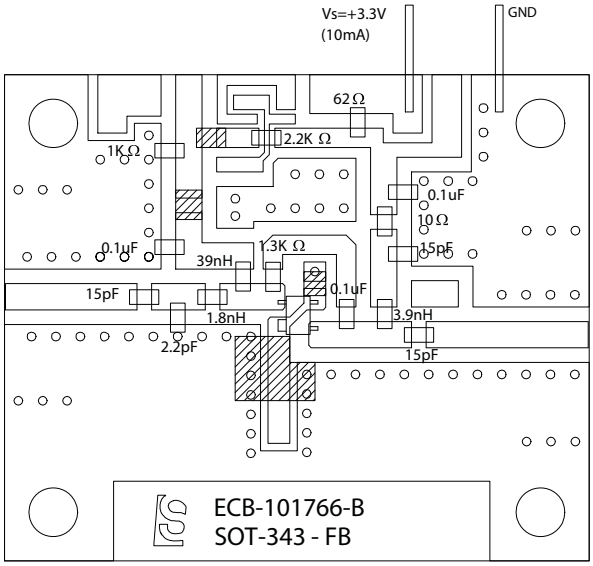
Optimal S11 Appl ication Circuit (V S =3.3V, V CE =2.7V, I CQ =10mA)



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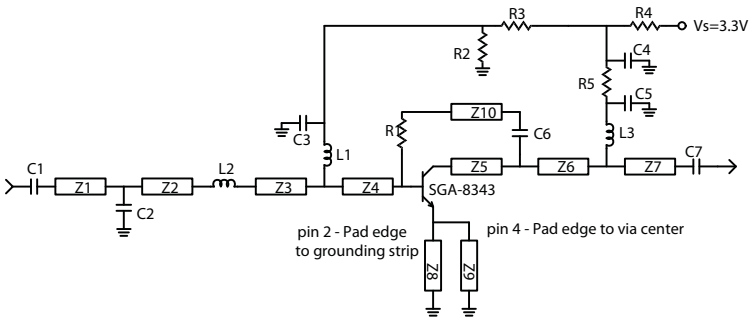
C1, 5, 7	ROHM MCH185A150J	15 pF
C2	ROHM MCH185A2R2C	2.2 pF
C3, 4, 6	Samsung CL10B104KONC	0.1uF
L1	TOKO LL1608-FS39NJ	39 nH
L2	TOKO LL1608-FS1N8S	1.8 nH
L3	TOKO LL1608-FS3N9S	3.9 nH
R1	ROHM MCR03J132	1.3K Ω
R2	ROHM MCR03J102	1.0K Ω
R3	ROHM MCR03J222	2.2K Ω
R4	ROHM MCR03J620	62 Ω
R5	ROHM MCR03J100	10 Ω

Ref. Des.	Part Number	Value
Z1	non-critical	50 Ω
Z2	4.6 degrees @ 1575 MHz	50 Ω
Z3	3.9 degrees @ 1575 MHz	50 Ω
Z4	7.1 degrees @ 1575 MHz	50 Ω
Z5	6.4 degrees @ 1575 MHz	50 Ω
Z6	6.4 degrees @ 1575 MHz	50 Ω
Z7	non-critical	50 Ω
Z8	3.2 degrees @ 1575 MHz	50 Ω
Z9	6.3 degrees @ 1575 MHz	50 Ω
Z10	26.0 degrees @ 1575 MHz	60 Ω

Optimal S11 Schematic



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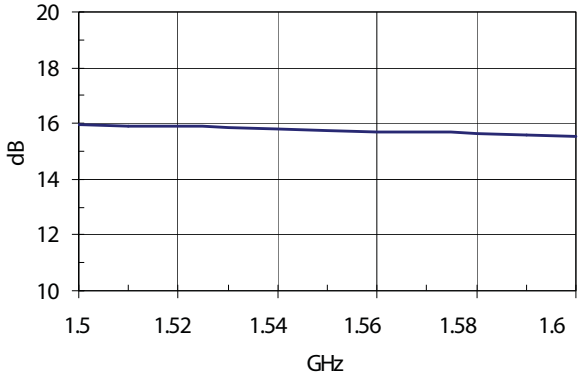
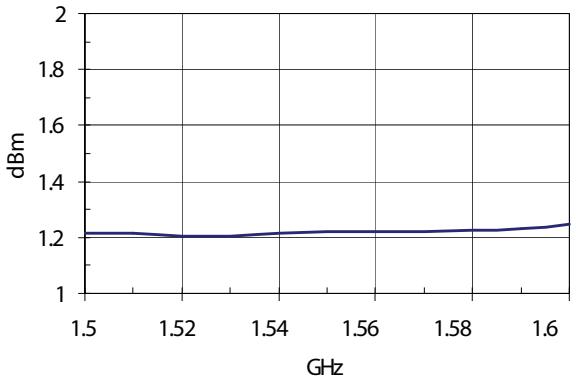
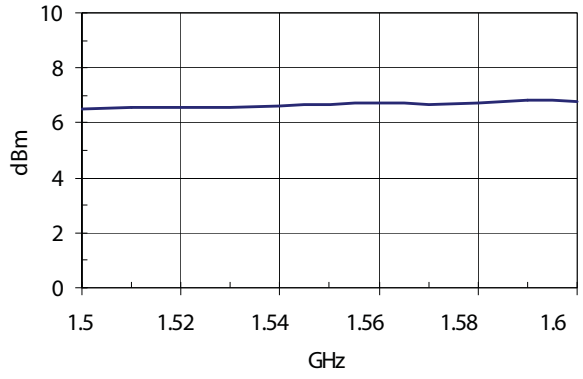
Gain vs. Frequency



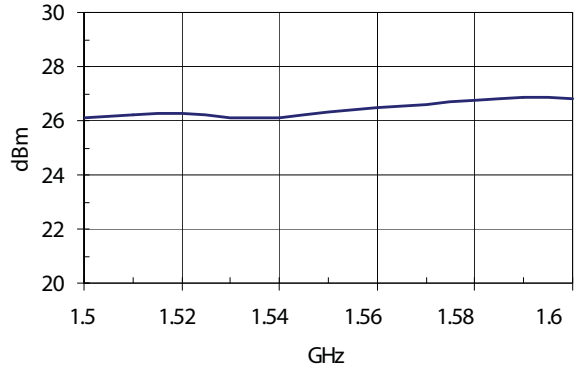
NF vs. Frequency



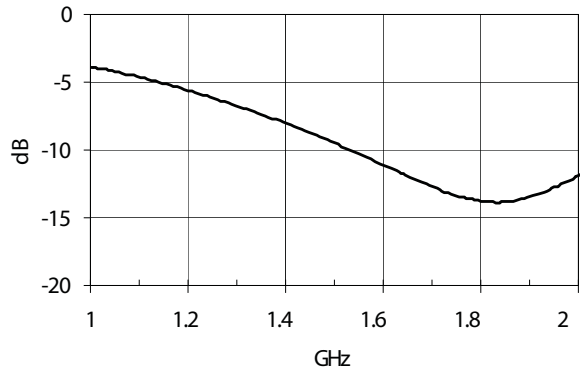
P1dB vs. Frequency



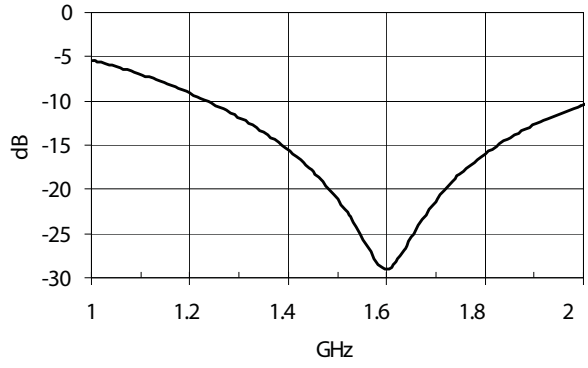
OIP3 vs. Frequency



S11 vs. Frequency



S22 vs. Frequency



Freq (GHz)	P1dB (dBm)	OIP3 (dBm)	Gain (dB)	S11 (dB)	S22 (dB)	NF (dB)
1.550	6.7	26.3	15.8	-10	-26	1.22
1.575	6.8	26.5	15.7	-11	-28	1.22
1.600	6.8	26.8	15.6	-11	-29	1.25

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