

# SZA-5044 Biasing, $V_{PC}$ Selection, and Performance versus Supply Voltage

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## Overview

The SZA-5044 is a very flexible amplifier in terms of biasing. It can be run deep class AB for best efficiency and up to near class A for the best linearity. The power on/off control voltages are accessible for each of the three stages and nominal currents are set via externally chosen series resistors for each stage. It can support power on voltage logic ( $V_{PC}$ ) from +2.9V to +5V by simply choosing the right resistor network for the desired quiescent current and  $V_{PC}$  power enable voltage. This application note addresses  $V_{PC}$  resistor selection,  $V_{PC}$  voltage selection, associated performance tradeoffs of the various configurations over temperature, and performance over supply voltage variation. If  $V_{CC} < 3.6V$  is required. The STA-6033(Z) is recommended.

## $V_{PC}$ Power Enable Bias Resistor Selection for Various $V_{PC}$ Voltage Levels

The schematic and table shown below describe the two recommended  $I_Q$  settings of 220mA and 270mA for  $V^+ = V_{CC} = 5V$ . The  $I_Q = 220mA$  bias has the best combination of  $P_{OUT}$  over temperature at 3% EVM (802.11a 54Mb/s). The  $I_Q = 270mA$  bias point has the best IM3 performance as compared to  $I_Q = 220mA$ . Table 1 shows resistor values for  $V_{CC} = 5V$  and  $V_{PC}$  range of 2.9V – 5V. Table 2 shows resistor values for other combinations of  $V_{CC}$  and  $V_{PC}$  levels.

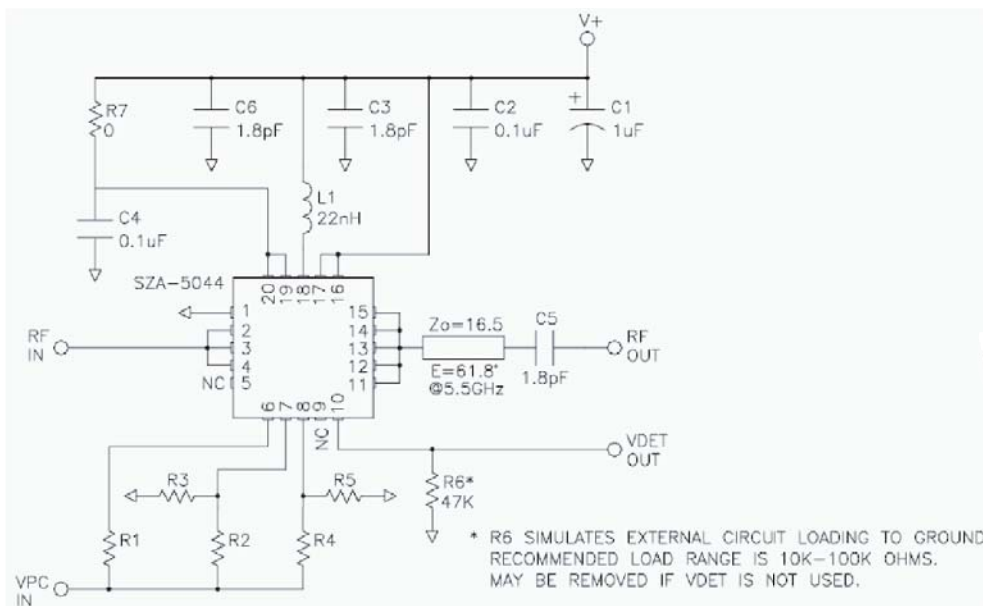


Figure 1. Application Schematic

Table 1

$V_{PC}=2.9V$ to $5.0V$										
$V_{CC}=5V$	$I_{CQ}=220mA$					$I_{CQ}=270mA$				
	Stage 1 (41mA)	Stage 2 (94mA)		Stage 3 (85mA)		Stage 1 (41mA)	Stage 2 (94mA)	Stage 3 (135mA)		
$V_{PC}$	R1 ( $\Omega$ )	R2 ( $\Omega$ )	R3	R4 ( $\Omega$ )	R5	R1 ( $\Omega$ )	R2 ( $\Omega$ )	R3	R4 ( $\Omega$ )	R5
2.9	0	698	OUT	221	OUT	0	698	OUT	10	OUT
3	174	1.10K	OUT	604	OUT	174	1.10K	OUT	261	OUT
3.1	348	1.37K	OUT	909	OUT	348	1.37K	OUT	499	OUT
3.2	511	1.78K	OUT	1.24K	OUT	511	1.78K	OUT	750	OUT
3.3	698	2.15K	OUT	1.50K	OUT	698	2.15K	OUT	1.00K	OUT
5	3.74K	2.49K	7.5K	7.15K	OUT	3.74K	2.49K	7.5K	2.6K	7.5K

Table 2

$V_{CC}=4.9V$ to $5.5V$ and $V_{PC}=2.9V$ to $5.0V$											
		$I_{CQ}=220mA$					$I_{CQ}=270mA$				
		Stage 1 (41mA)	Stage 2 (94mA)		Stage 3 (85mA)		Stage 1 (41mA)	Stage 2 (94mA)	Stage 3 (135mA)		
$V_{CC}(V)$	$V_{PC}(V)$	R1 ( $\Omega$ )	R2 ( $\Omega$ )	R3	R4 ( $\Omega$ )	R5	R1 ( $\Omega$ )	R2 ( $\Omega$ )	R3	R4 ( $\Omega$ )	R5
4.9	2.9	0	200	OUT	249	OUT	0	200	OUT	0	OUT
4.9	3	182	412	OUT	562	OUT	182	412	OUT	237	OUT
4.9	3.1	365	604	OUT	909	OUT	365	604	OUT	475	OUT
4.9	3.2	562	825	OUT	1.21K	OUT	562	825	OUT	698	OUT
4.9	3.3	698	1.02K	OUT	1.50K	OUT	698	1.02K	OUT	1.00K	OUT
5.1	2.9	0	243	OUT	301	OUT	0	243	OUT	20	OUT
5.1	3	182	442	OUT	619	OUT	182	442	OUT	274	OUT
5.1	3.1	340	665	OUT	1.00K	OUT	340	665	OUT	511	OUT
5.1	3.2	511	825	OUT	1.24K	OUT	511	825	OUT	750	OUT
5.1	3.3	698	1.10K	OUT	1.62K	OUT	698	1.10K	OUT	1.02K	OUT
5.1	5	3.74K	2.61K	7.5K	7.32K	OUT	3.74K	2.61K	7.5K	2.8K	7.5K
5.2	2.9	10	249	OUT	332	OUT	10	249	OUT	49.9	OUT
5.2	3	174	475	OUT	665	OUT	174	475	OUT	301	OUT
5.2	3.1	348	681	OUT	1.02K	OUT	348	681	OUT	562	OUT
5.2	3.2	562	887	OUT	1.37K	OUT	562	887	OUT	825	OUT
5.2	3.3	698	1.10K	OUT	1.69K	OUT	698	1.10K	OUT	1.10K	OUT
5.2	5	3.74K	2.61K	7.5K	7.50K	OUT	3.74K	2.61K	7.5K	2.87K	7.5K
5.3	2.9	10	274	OUT	348	OUT	10	274	OUT	82.5	OUT
5.3	3	196	499	OUT	698	OUT	196	499	OUT	340	OUT
5.3	3.1	357	750	OUT	1.02K	OUT	357	750	OUT	604	OUT
5.3	3.2	511	909	OUT	1.37K	OUT	511	909	OUT	825	OUT
5.3	3.3	698	1.15K	OUT	1.74K	OUT	698	1.15K	OUT	1.10K	OUT
5.3	5	3.74K	2.67K	7.5K	7.68K	OUT	3.74K	2.67K	7.5K	3.0K	7.5K
5.4	2.9	0	287	OUT	374	OUT	0	287	OUT	100	OUT
5.4	3	182	511	OUT	750	OUT	182	511	OUT	348	OUT
5.4	3.1	357	750	OUT	1.10K	OUT	357	750	OUT	604	OUT

Table 2

5.4	3.2	562	1.00K	OUT	1.37K	OUT	562	1.00K	OUT	887	OUT
5.4	3.3	698	1.18K	OUT	1.78K	OUT	698	1.18K	OUT	1.13K	OUT
5.4	5	3.74K	2.67K	7.5K	7.68K	OUT	3.74K	2.67K	7.5K	3.16K	7.5K
5.5	2.9	0	301	OUT	383	OUT	0	301	OUT	100	OUT
5.5	3	174	511	OUT	750	OUT	174	511	OUT	357	OUT
5.5	3.1	340	750	OUT	1.10K	OUT	340	750	OUT	619	OUT
5.5	3.2	511	1.00K	OUT	1.47K	OUT	511	1.00K	OUT	909	OUT
5.5	3.3	698	1.21K	OUT	1.78K	OUT	698	1.21K	OUT	1.18K	OUT
5.5	5	3.74K	2.67K	7.5K	8.06K	OUT	3.74K	2.67K	7.5K	3.32K	7.5K

The temperature range and required performance of the application should be considered when choosing a  $V_{PC}$  power enable voltage. The higher  $V_{PC}$  values have better performance over temperature because  $I_Q$  varies less with temperature. Below is Figure 2 that shows  $I_Q$  variation over temperature for  $V_{PC}$  enable set voltages ranging from 2.9V to 5V.

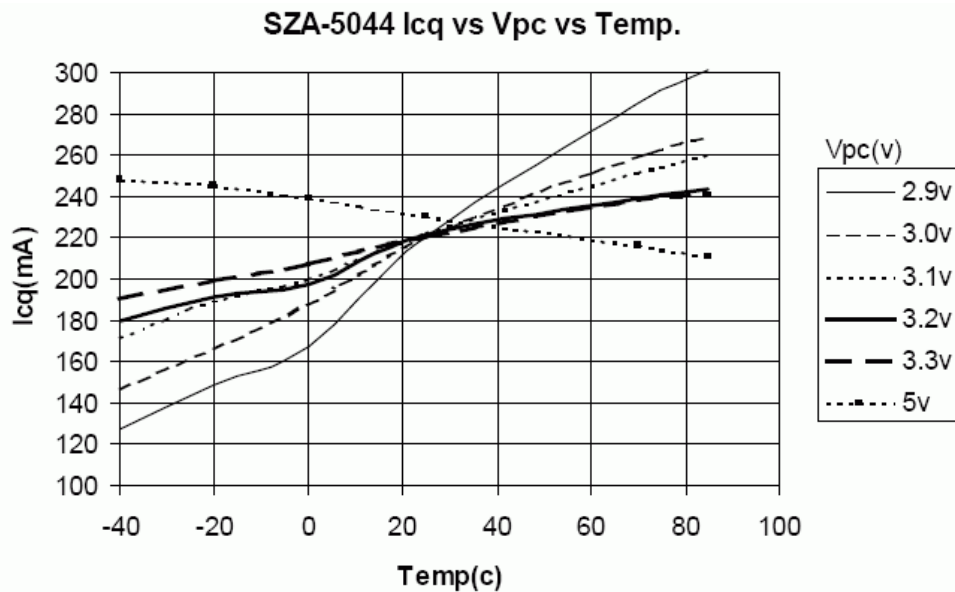


Figure 2. SZA-5044  $I_{CQ}$  versus  $V_{PC}$  versus Temperature

Another consideration is the variation in V<sub>PC</sub> enable voltage and the impact on performance. Performance is optimized when the V<sub>PC</sub> power enable is regulated and controlled. This is the case for the Atheros chip set where a regulated V<sub>PC</sub> enable=2.9V is available. Figure 3 shows I<sub>Q</sub> versus swept V<sub>PC</sub> for the nominal cases of V<sub>PC</sub> enable=2.9V to 5V at 25 °C.

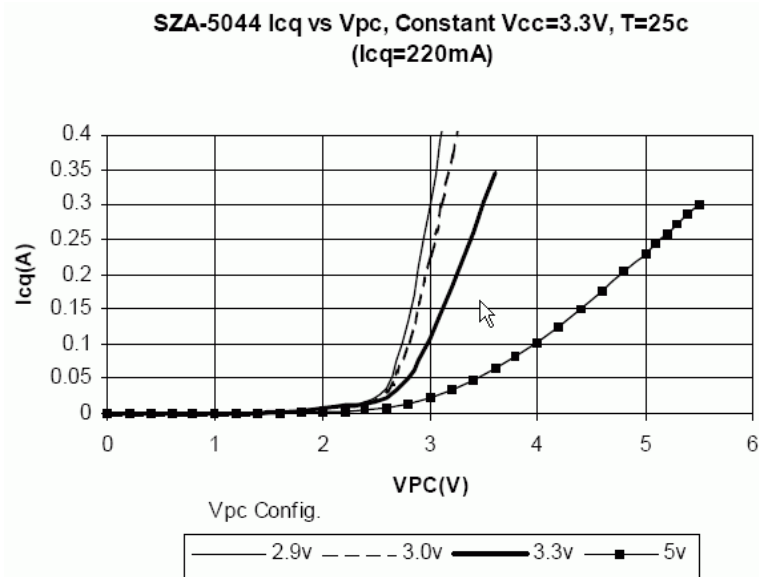


Figure 3. SZA-5044 I<sub>Q</sub> versus Swept V<sub>PC</sub>, Constant V<sub>CC</sub>=5V, T=25 °C

The variation in current over temperature has impact on EVM over temperature. Figure 4 shows the EVM at P<sub>OUT</sub>=21.5dBm versus temperature and V<sub>PC</sub> enable set voltage.

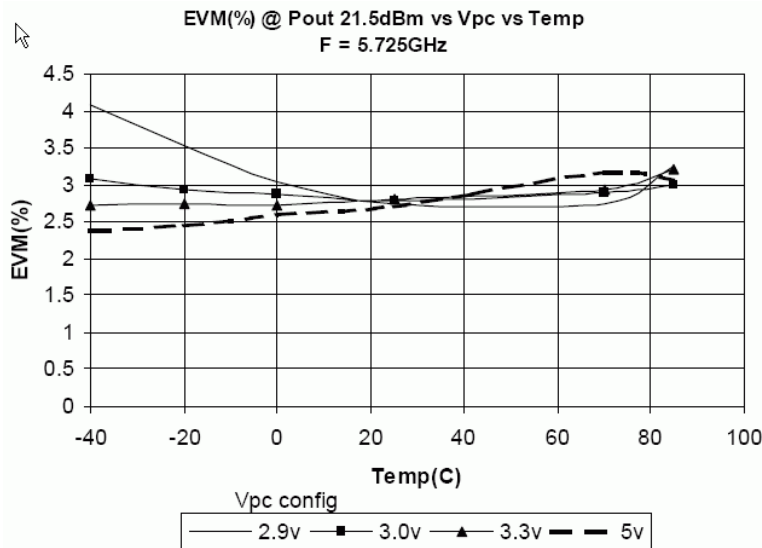


Figure 4. EVM (%) at P<sub>OUT</sub>=21.5dBm versus V<sub>PC</sub> versus Temp

The variation in  $V_{CC}$  also has an impact on EVM. Figure 5 shows the  $P_{OUT}$  at 3% EVM versus temperature and fixed  $V_{PC}$  voltage=5.0V.

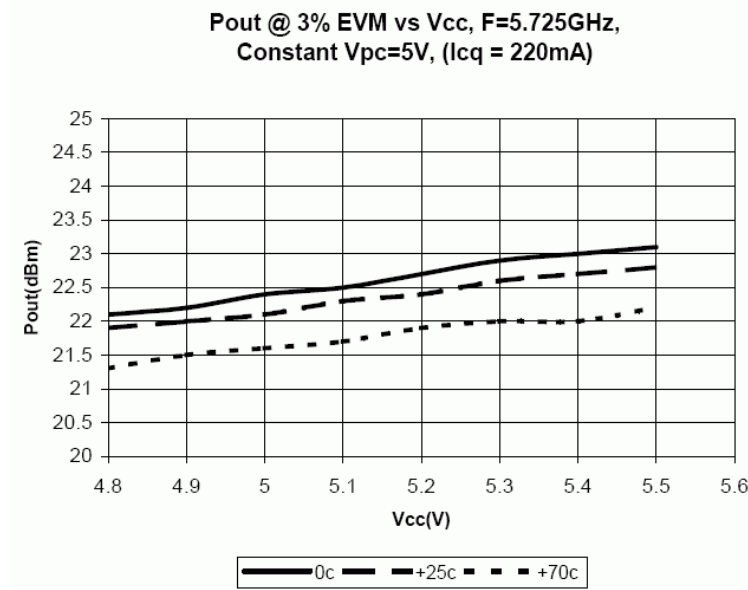


Figure 5.  $P_{OUT}$  at 3% EVM versus  $V_{CC}$ ,  $F=2.4GHz$ , Constant  $V_{PC}=5V$ ,  $ICQ=302mA$