Gain Block Active Bias Circuit

Abstract

Gain Block amplifiers (SGA,NGA,SNA,SCA series) sometimes require power supply voltages very close to the rated device voltage. This provides a challenge to stabilize current with temperature and device-to-device bias voltage variations. A cost effective and power efficient solution to this problem is discussed here.

Introduction

In order to obtain stable bias current and consistent RF performance using gain block amplifiers, RFMD recommends that customers normally use a dropping resistor in series with the power supply voltage so that a minimum 2 Volt drop is maintained across it. This circuit configuration is shown in Figure 1(a). To emphasize the temperature dependence of Vd, it is represented in the expression for device current as Vd(T). Many customers who utilize our products in battery operated or other low voltage applications find that they do not have a 2 Volt margin to spare. This problem can be addressed by utilizing a high compliance current source.

Figure 1(b) shows a high-compliance constant-current generator used as an active bias source.By appropriate component selection, this circuit will provide precise constant current bias for AR1 for maximum AR1 device voltages of 92% Vs . DC regulation power efficiency can reach 90 %.

Design / Performance Summary

The SGA-5589 was selected as the target device around which the design example shown on Page 2 was centered. The goal is to bias the SGA-5589 with a constant current at it's rated value of 60 mA over temperature (-40C to +85C) using only a single 5 Volt supply.

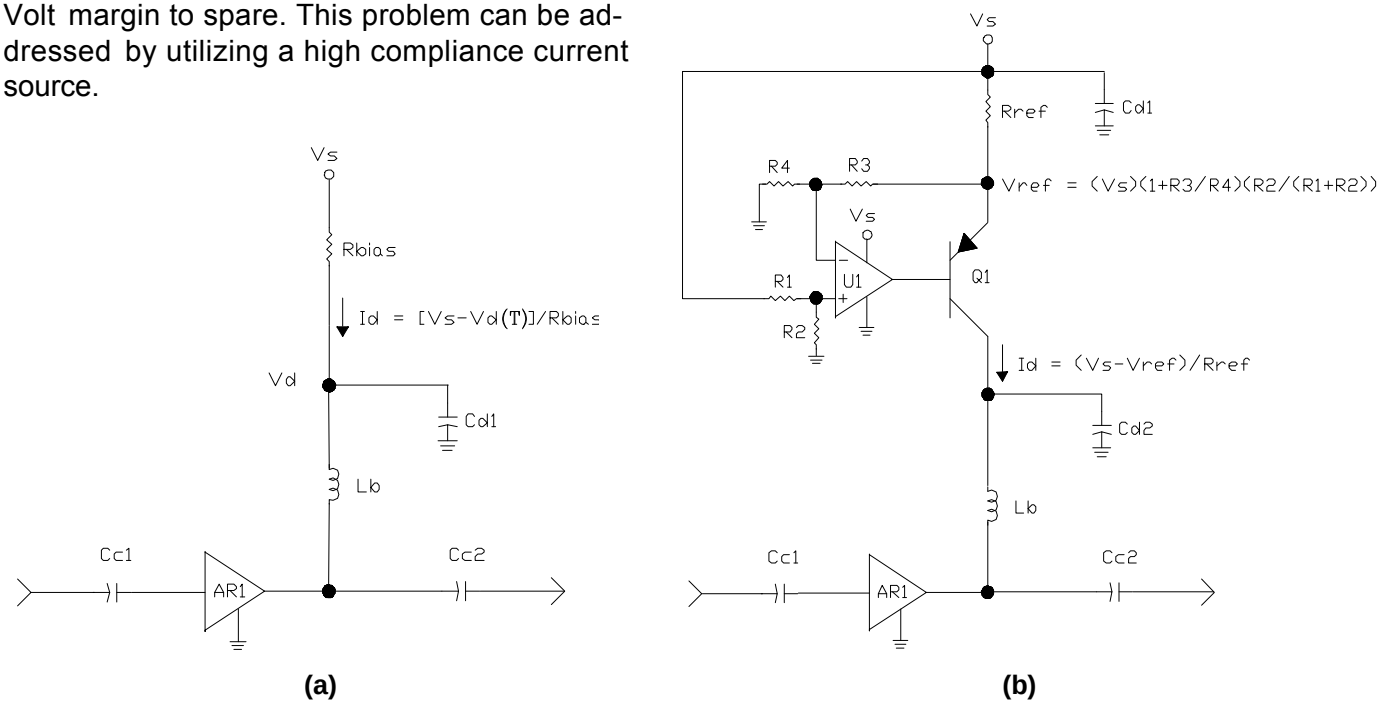


Figure 1 : (a) Standard Gain Block Passive Bias Circuit
(b) High Compliance Current Source Active Bias Circuit

Design Example

The goal in the remaining pages is to demonstrate the procedure for tailoring the circuit in Figure 1(b) to suit the needs of a particular amplifier and show the component selection techniques. In this case, the SGA-5589 has been selected and the goal is to design the high compliance current source to work from a power supply source of +5 Volts and to provide constant current bias over temperature and over a distribution of device voltage values, typical of a production lot.

Procedure

The datasheet for the SGA-5589 indicates that a nominal bias current of 60 mA is required in order to achieve the specified RF performance. We also see that the typical device voltage at room temperature required for 60 mA bias current is 3.9 Volts. On page 7, a typical histogram of device voltage for this part at room temperature is shown. The datasheet for this device states that the allowable device voltage range @25C is 3.5 to 4.3 Volts. From the sample histogram shown, a few devices in this wafer were above the 4.3 Volt upper limit and some were just barely within it. It is therefore desirable to design the active bias circuit to supply room temperature device voltages of at least the 4.3 Volt upper limit. An additional constraint on device voltage is temperature variation @ 60 mA, shown also on page 7. The graph shown was taken from a sample device and indicates an average Vd temperature coefficient of about -4.1 mV/ Deg. C. over the -40C to +85C temprature range. From +25C to -40C , we see an increase of 300 milliVolts in Vd. Since we can assume that the temperature characteristic is fairly constant from device to device, an amplifier with a Vd @+25 Deg. C which falls precisely at 4.3 Volts should rise to about 4.6 Volts at -40 Deg. C. This should be the worst case load voltage experienced by the constant current source over temperature. This means that the value for Vref (defined in Figures 1(b) and 2) needs to be 4.6 Volts plus an allowance for the VCE saturation voltage of control transistor Q1. Obviously, this number should be as low as possible. Many devices can be used here, but the device chosen

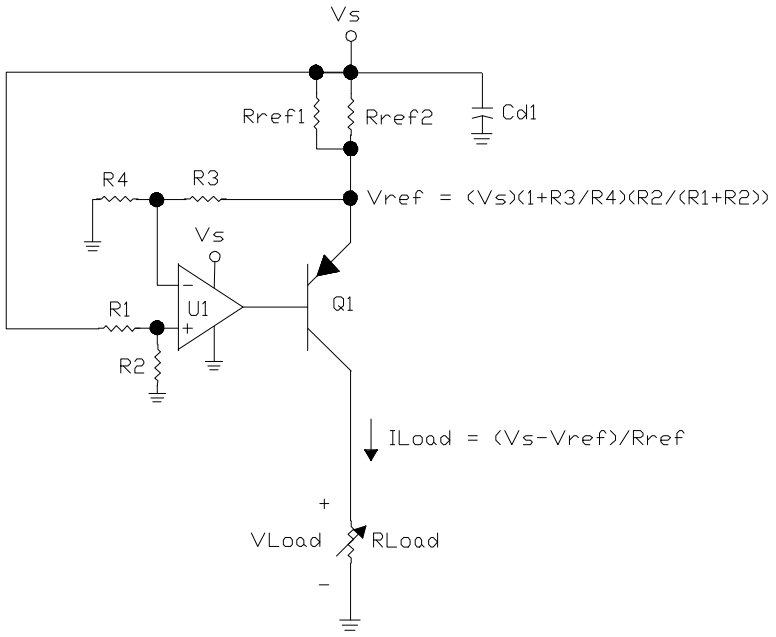


Figure 2 : Test Circuit for High Compliance Current Source

Table of Component Values

Ref. Desig.	Description	Value
R2,R4	Resistor, 1%,1/8W	1 KW
R1	Resistor, 1%,1/8W	4.99 KW
R3	Resistor, 1%,1/8W	4.64 KW
Rref1	Resistor, 5%,1/8W	5.1 W
Rref2	Resistor, 5%,1/8W	91 W
Vs	Supply Voltage	+ 5.00 Volts
U1	Operational Amplifier	LMC 7111
Q1	Transistor, PNP	FMMT-717

Design Example (continued)

for this experiment was a ZETEX FMMT-717 PNP transistor. VCEsat (max) for this device is specified at -0.17V @ 1500 mA. At a current of 60 mA., VCE sat should be about (.06 /1.5)(-.17) = -.0068 volt. The required value of Vref can therefore be estimated at 4.6 + .01 = 4.61 volts. This means that maximum load voltage will coincide with saturation of Q1 at a temperature of about -40 Deg. C. To add a little extra margin, we will select vref = 4.71 volts.

Vref = Vdmax@25C + DVd(T) + VCE(sat) + Vmargin = 4.3+0.3+0.01+0.1 = 4.71 Volts

The value of Vref will be determined by selecting the appropriate gain control resistor values for operational amplifier U1. The component value table on Page 2 shows the resistor values (R1-R4) required to set Vref at 4.71 volts with a supply voltage of 5.00 volts. U1 must be a single supply, rail-to-rail op amp with low power consumption compared to the SGA-5589 and low input offset voltage. The device used here was an LMC7111 from National Semiconductor. The accuracy of Vref is important because of the small difference between it and Vs. Any error in voltage accuracy is passed on to the generated source current.This is also why 1% resistors were used for R1-R4. The value of Rref can now be determined as :

Rref = (Vs-Vref)/Id = (5-4.71)/.06 = 4.83 Ohms.

This value was implemented by using 5.1 and 91 Ohms in parallel (Rref1 and Rref2 in Figure 2). It is acceptable to use 5% resistors in these slots. The complete list of components is shown in the table on Page 2. Note that in this design the value of Vref is directly proportional to Vs. This means that the current sourced to the load will be directly proportional to Vs also.

The results of variable load resistance testing for the circuit of Figure 2 are shown graphically on page 5. D.C. load voltage and D.C. regulation efficiency are plotted as functions of load resistance. Note that the maximum load voltage limits at above 4.6 Volts, as predicted. Also, the D.C. regulation efficiency peaks at about 90 % for the same load. Operating the current source near the high end of it's load voltage capacity therefore results in higher efficiency.
Sheet 5 shows test results of a complete SGA-5589 amplifier circuit biased with the high compliance current source. The gain vs. frequency response delivered by the circuit is shown and the circuit is performing as expected.

Conclusions

In this application note, we have presented a design for a single supply, high compliance constant current source that will allow operation of the SGA-5589 to within about 350 mV of the 5 Volt supply rail with a constant current of 60 mA. It should be recognized however that the reference voltage could be set even closer to the power supply rail, simply by proper selection of resistor values using the process described above. The limiting factor will be the saturation characteristics of the bias transistor Q1, the accuracy to which very low values of Rref can be adjusted and the degree of resolution to which resistors R1 - R4 can set the value of Vref. In addition, this basic circuit can be easily modified to supply the required bias current for any gain block amplifier offered by RFMD. Please refer to page 4 for a condensed design procedure which can be used with this circuit to provide the correct constant current bias to any of our gain blocks. RFMD is pleased to offer this application note as a design aid for our customers and we hope that they may find it beneficial.

General Design Procedure for Adaptation of Constant Current Source to any Gain Block Amplifier.

1.0 Select an amplifier and power supply voltage (Vs) such that the power supply voltage is greater than the maximum device voltage over temperature for all production lots (Vd max) of the amplifier required for nominal bias current (Ib) by at least 200 millivolts.

2.0 From the amplifier specifications, determine the nominal bias current . Select a value of Vref such that Vs - 0.1Volt => Vref >= Vd max + 0.1Volt. Calculate the required value of Rref from the following formula:

Rref = (Vs-Vref) / Ib

3.0 Calculate the values of R1 - R4 to select the gain of operational amplifier U1 so as to generate the desired value for Vref. Use the following formula:

Vref = (Vs)(1+R3 / R4)(R2 / (R1+R2))

NOTE: It is good practice to make sure that the following relationship holds approximately for R1-R4 :

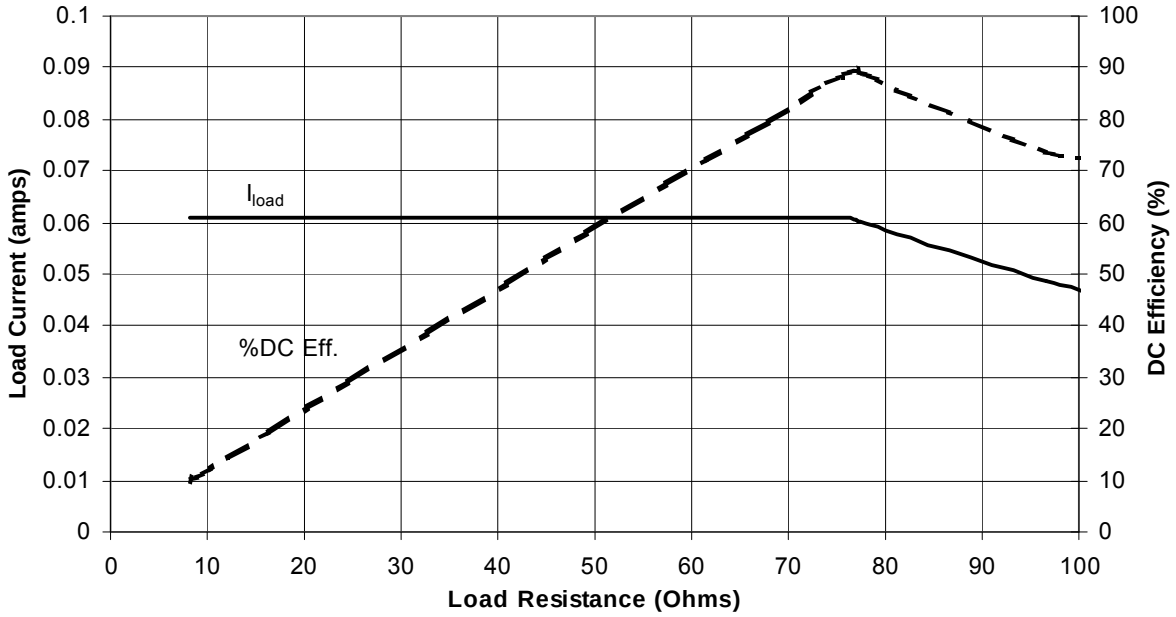
(R1)(R2)/(R1+R2) = (R3)(R4)/(R3+R4)

This will ensure minimum input offset error in op amp U1. Values for R1-R4 should also be within about the 1K to 20K range.

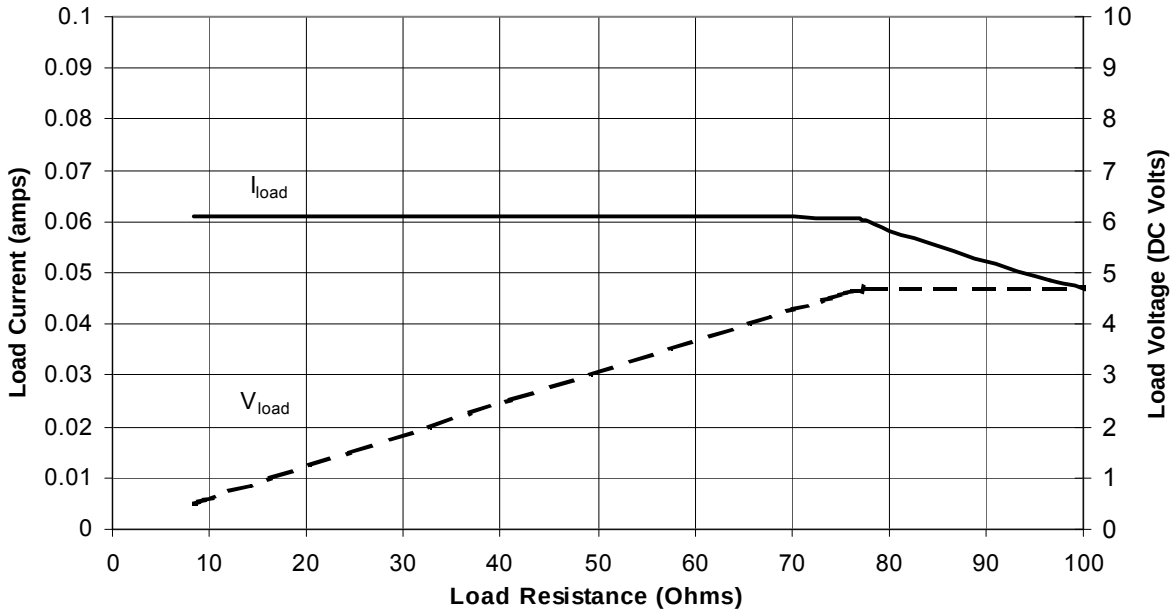
4.0 Use Cd1 and Cd2 values similar to those specified on sheet 6. WARNING: Do not connect decoupling capacitors directly between the emitter of Q1 and ground, as this may destabilize Q1. Also, avoid adding decoupling capacitors directly between the inverting input of U1 and ground.

NOTE: The above instructions presume the use of the LMC7111 for U1 and the FMMT-717 for Q1, or equivalents.

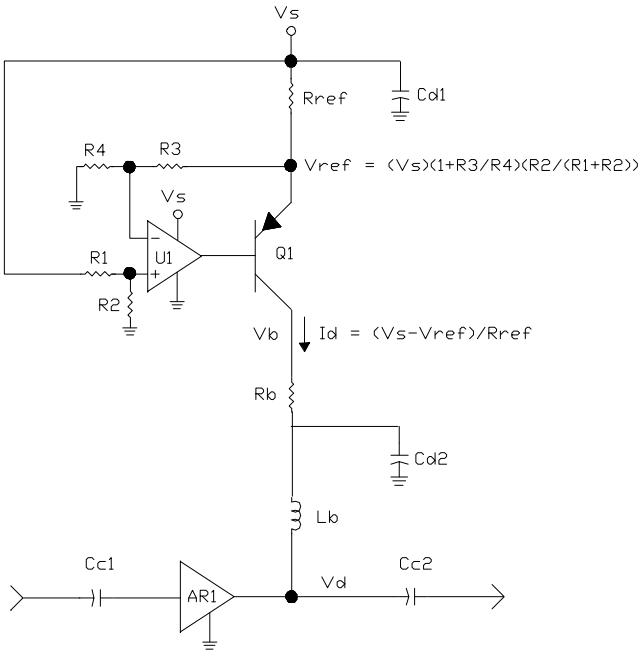
Plot of DC Load Current and % DC Efficiency vs. Load Resistance for High Compliance Current Source, Vs=+5.00 Volts, Vref = 4.71 Volts,Rref = 4.83 Ohms



Plot of DC Load Current and DC Load Voltage vs. Load Resistance for High Compliance Current Source, Vs=+5.00 Volts,Vref= 4.71 Volts, Rref = 4.83 Ohms



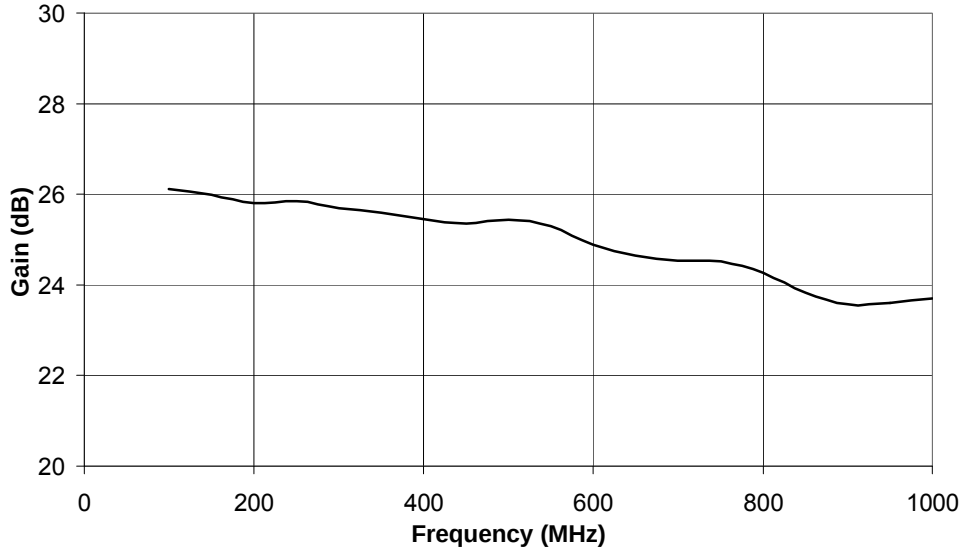
Design Example Experimental Results for CCS interface to actual SGA-5589 Amplifier Circuit



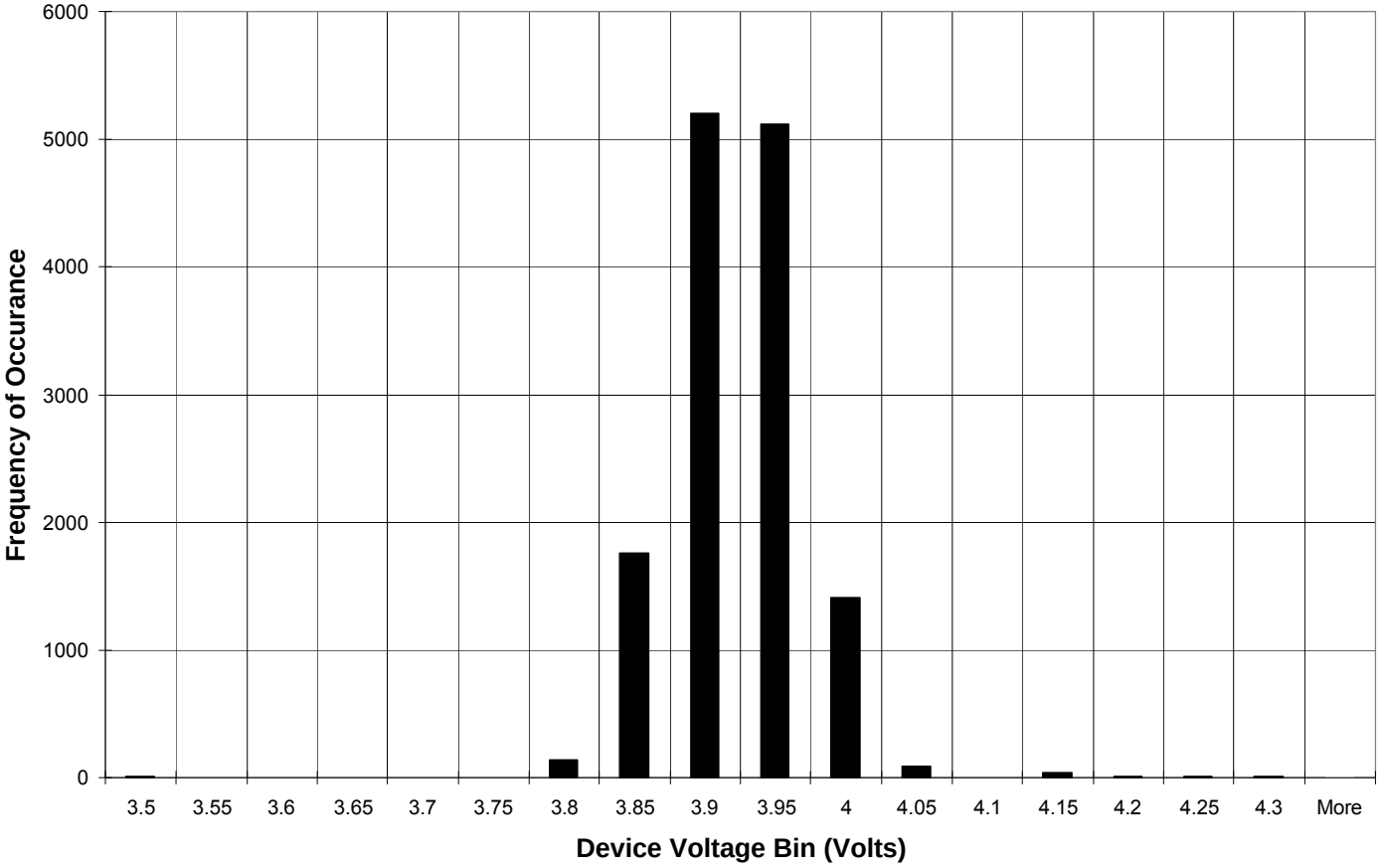
In schematic at left, Lb =1.5 uH. Cc1,2 =.01 uF. Cd1= 1 uF tantalum Cd2 = 2x .01 uF (ceramic chip) +1x22uF tantalum. The dc conditions per schematic at left were measured per the table below.

Parameter	Value
Vb (d.c. Volts)	3.948
Vd (d.c. Volts)	3.826
Id (dc mA).	60

Plot of Gain vs. Frequency SGA-5589 Amplifier biased w. High Compliance Constant Current Source.



Typical SGA-5589 Device Voltage Histogram for Id = 60 mA @ T = +25C



Sample Device Voltage vs. Temperature for SGA-5589, Id = 60 mA