

SPDT High Power UltraCMOS® RF Switch Radiation Tolerant for Space Applications

Features

- Single +3V power supply
- Low insertion loss: 0.55 dB @ 2000 MHz
- High isolation of 30 dB @ 2000 MHz
- Typical input P1dB compression point of +31 dBm
- 100 kRad(Si) total dose
- Single-pin CMOS or TTL logic control
- Low cost

Product Description

The PE9354 SPDT high power UltraCMOS® RF switch is designed to cover a broad range of applications from near DC to 3000 MHz. This single-supply reflective switch integrates on-board CMOS control logic driven by a simple, single-pin CMOS and TTL compatible control input. Using a nominal +3V power supply, a typical input P1dB compression point of +31 dBm can be achieved. The PE9354 also exhibits input-output isolation of better than 30 dB at 2000 MHz and is offered in a small 8-lead CFP.

The PE9354 is optimized for commercial space applications and is manufactured on Peregrine's UltraCMOS process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate, offering excellent RF performance and intrinsic radiation tolerance. Single event latch-up (SEL) is physically impossible and single event upset (SEU) is better than 10^{-9} errors per bit/day.

Figure 1. Functional Diagram

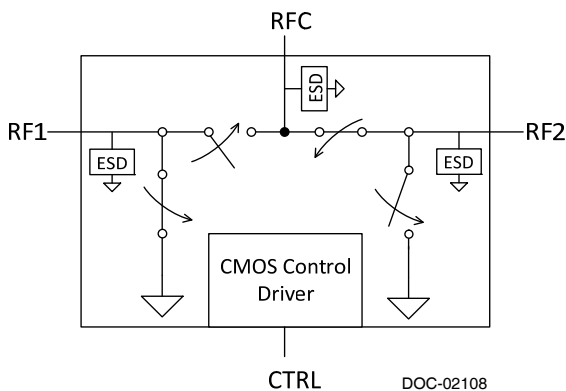


Figure 2. Package Type
8-lead CFP

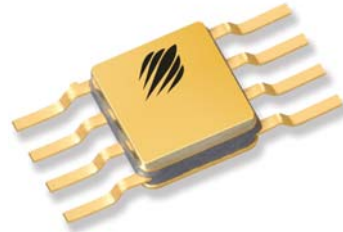


Table 1. AC Electrical Specifications @ -55 °C to +125 °C, V_{DD} = 3.0V (Z_S = Z_L = 50Ω)¹

Parameter	Condition	Min	Typ	Max	Unit
Operation frequency ²		DC		3000	MHz
Insertion loss	2000 MHz		0.55	0.80	dB
Isolation – RFC to RF1/RF2	2000 MHz	28	32		dB
Isolation – RF1 to RF2	2000 MHz	24	28		dB
Return loss ³	2000 MHz		22		dB
Input P1dB compression point	2000 MHz	28	31		dBm

Notes: 1. Parameters are tested in production at -40 °C and +85 °C. Parameters are guaranteed through characterization at -55 °C, +25 °C and +125 °C.

2. Device linearity will begin to degrade below 10 MHz.

3. Return loss not measured in production due to equipment limitations.

Figure 3. Pin Configuration

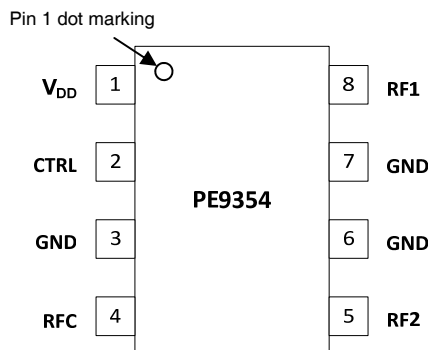


Table 2. Pin Descriptions

Pin #	Pin Name	Description
1	V _{DD}	Nominal +3V supply connection.
2	CTRL	CMOS or TTL logic level: High = RFC to RF1 signal path. Low = RFC to RF2 signal path.
3	GND	Ground connection. Traces should be physically short and connected to ground plane for best performance.
4	RFC	Common RF port for switch.*
5	RF2	RF2 port.*
6	GND	Ground connection. Traces should be physically short and connected to ground plane for best performance.
7	GND	Ground connection. Traces should be physically short and connected to ground plane for best performance.
8	RF1	RF1 port.*

Note: * All RF pins must be DC blocked with an external series capacitor or held at 0 VDC.

Table 3. DC Electrical Specifications

Parameter	Min	Typ	Max	Unit
Supply voltage, V _{DD}	2.7	3.0	3.3	V
Input leakage	-1		1	μA
Supply current, I _{DD} (V _{DD} = 3V, V _{CTRL} = 3V)		28	100	μA
Control voltage high	0.7 × V _{DD}			V
Control voltage low			0.3 × V _{DD}	V

Table 4. Absolute Maximum Ratings

Symbol	Parameter/Condition	Min	Max	Unit
V _{DD}	Power supply voltage	-0.3	4.0	V
V _I	Voltage on any input except for the CTRL input	-0.3	V _{DD} + 0.3	V
V _{CTRL}	Voltage on CTRL input		5.0	V
T _{ST}	Storage temperature range	-65	+150	°C
T _{OP}	Operating temperature range	-55	+125	°C
P _{IN}	Input power (50Ω)		32	dBm
V _{ESD}	ESD voltage (Human Body Model)		200	V
TID	Total cumulative exposure to ionizing radiation		100	kRad(Si)

Absolute maximum ratings are those values listed in the above table. Exceeding these values may cause permanent device damage. Functional operation should be restricted to the limits in the *DC Electrical Specifications* table. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified in *Table 3*.

Latch-Up Immunity

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

Table 5. Control Logic Truth Table

Control Voltage	Signal Path
CTRL = CMOS or TTL High	RFC to RF1
CTRL = CMOS or TTL Low	RFC to RF2

The control logic input pin (CTRL) is typically driven by a +3V CMOS logic level signal, and has a threshold of 50% of V_{DD}. For flexibility to support systems that have 5-volt control logic drivers, the control logic input has been designed to handle a 5-volt logic HIGH signal. (A minimal current will be sourced out of the V_{DD} pin when the control logic input voltage level exceeds V_{DD}.)

Typical Performance Data @ -55 °C to +125 °C

Figure 4. Insertion Loss – RFC to RF1

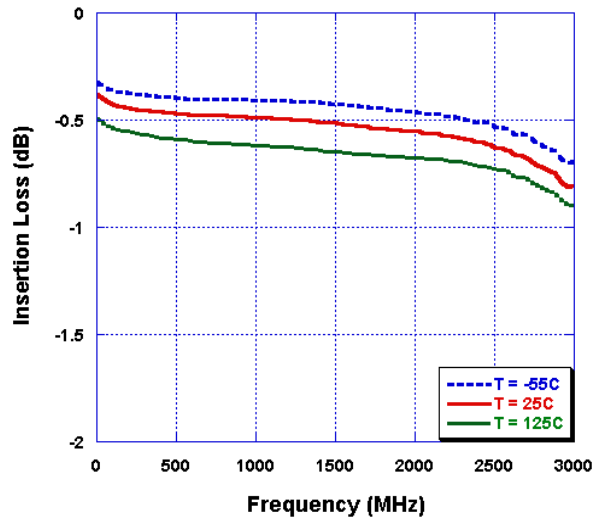


Figure 5. Input P1dB Compression Point

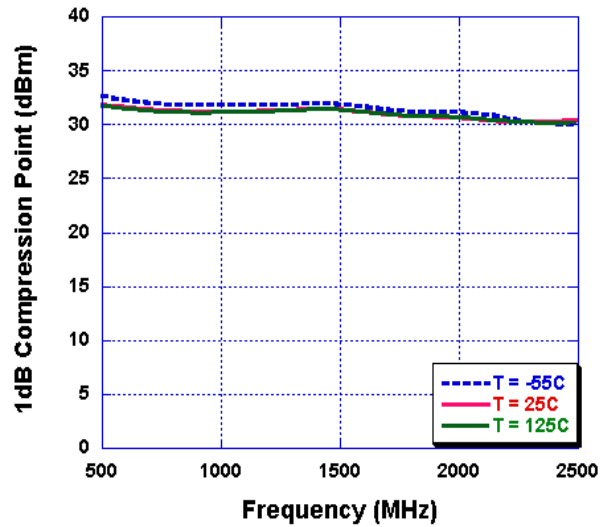


Figure 6. Insertion Loss – RFC to RF2

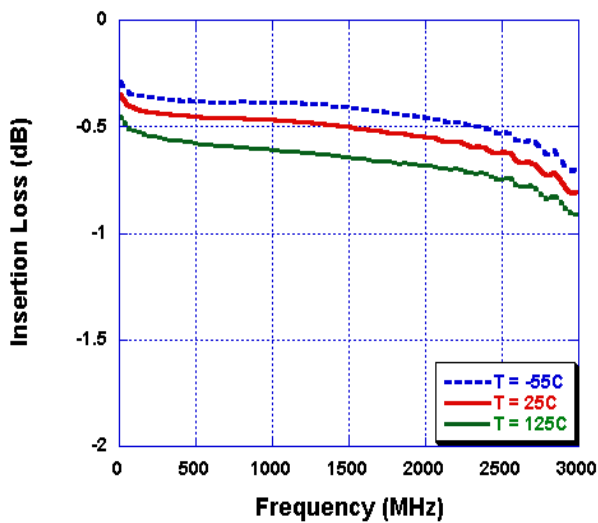
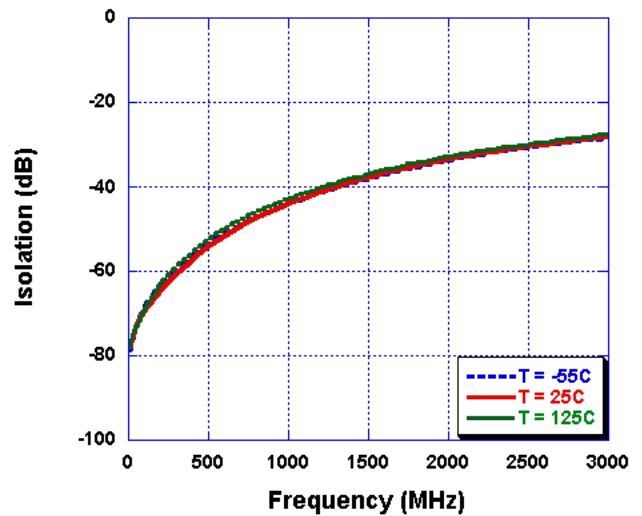


Figure 7. Isolation – RFC to RF1



Typical Performance Data @ -55 °C to +125 °C (cont.)

Figure 8. Isolation – RFC to RF2

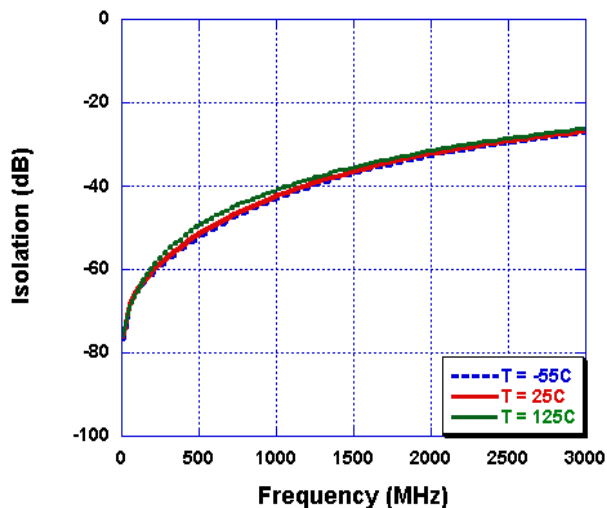


Figure 9. Isolation – RF1/RF2 to RF2/RF1

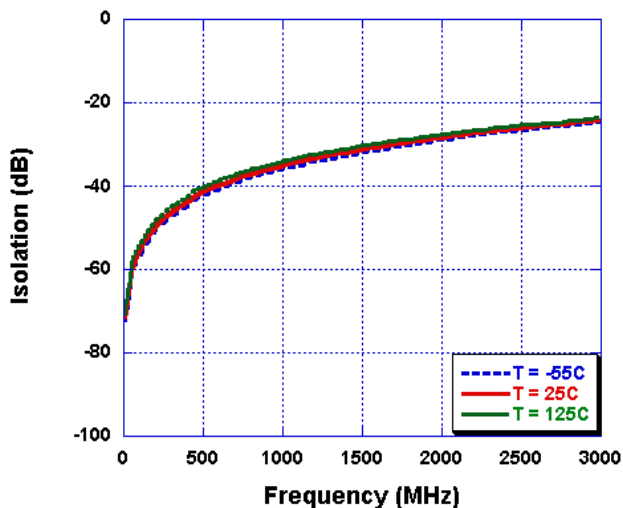


Figure 10. Return Loss – RFC

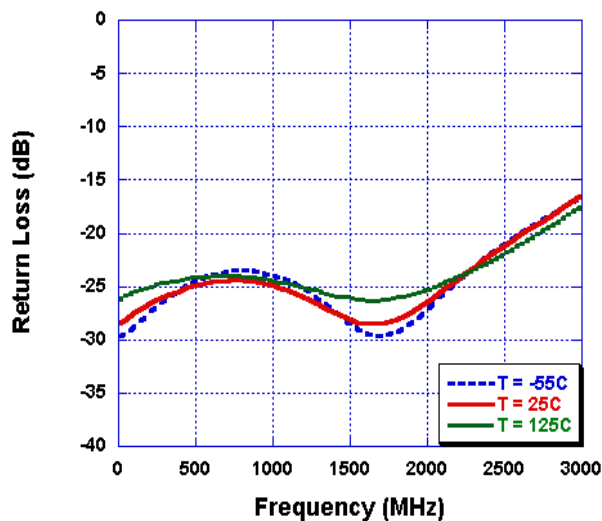
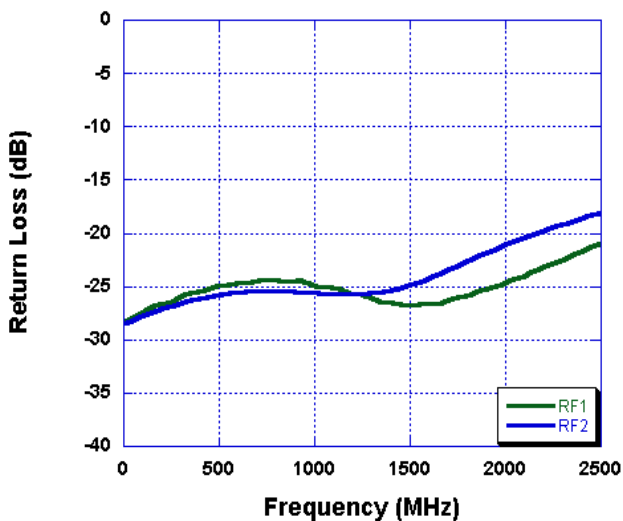


Figure 11. Return Loss – RF1, RF2



Evaluation Kit

The SPDT switch evaluation kit board was designed to ease customer evaluation of the PE9354 SPDT switch. The RF common port is connected through a 50Ω transmission line to the top left SMA connector, J1. Port 1 and Port 2 are connected through 50Ω transmission lines to the top two SMA connectors on the right side of the board, J2 and J3. A through transmission line connects SMA connectors J4 and J5. This transmission line can be used to estimate the loss of the PCB over the environmental conditions being evaluated.

The board is constructed of a two metal layer FR4 material with a total thickness of 0.031". The bottom layer provides ground for the RF transmission lines. The transmission lines were designed using a coplanar waveguide with ground plane model using a trace width of 0.030", trace gaps of 0.007", dielectric thickness of 0.028", metal thickness of 0.0014" and ϵ_r of 4.4.

J6 provides a means for controlling DC and digital inputs to the device. Starting from the lower left pin, the second pin to the right (J2–3) is connected to the device CTRL input. The fourth pin to the right (J2–7) is connected to the device V_{DD} input. A decoupling capacitor (100 pF) is provided on both CTRL and V_{DD} traces. It is the responsibility of the customer to determine proper supply decoupling for their design application. Removing these components from the evaluation board has not been shown to degrade RF performance.

The ground plane has been removed from beneath the device for performance issues. It was found that insertion loss dips (suck-outs) were experienced due to the capacitive effect of the metal package sitting insulated by the solder-mask on the ground plane. All data specified and shown on this datasheet was taken using this evaluation board configuration. For optimal performance, the package may be soldered directly to the ground plane, but the reliability issues associated with this mounting must be addressed by the customer.

Figure 12. Evaluation Board Layouts

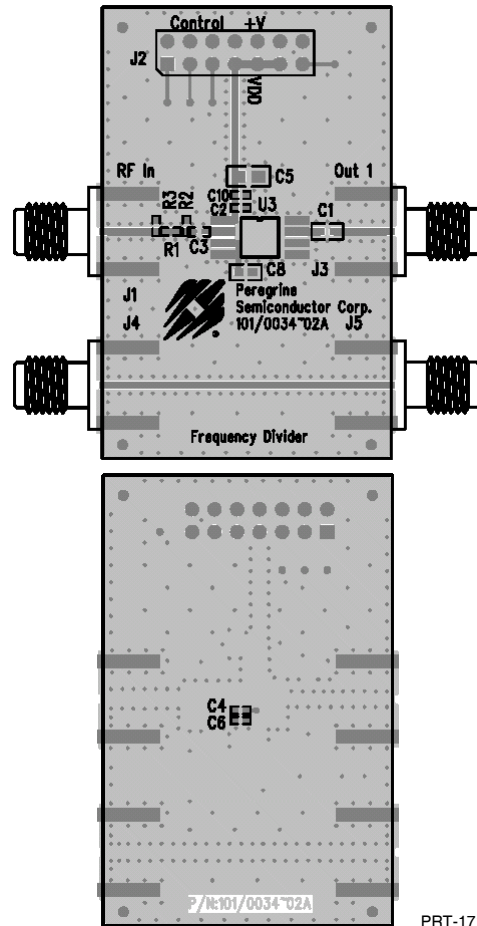


Figure 13. Evaluation Board Schematic

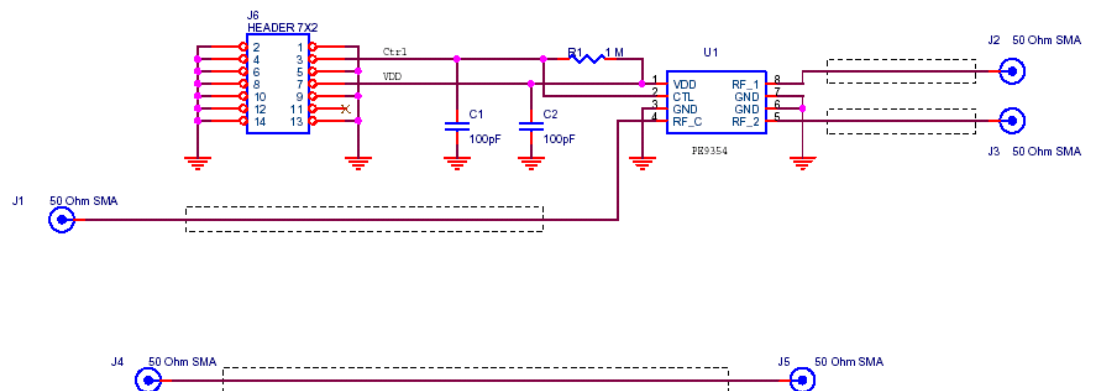


Figure 14. Package Drawing
8-lead CFP

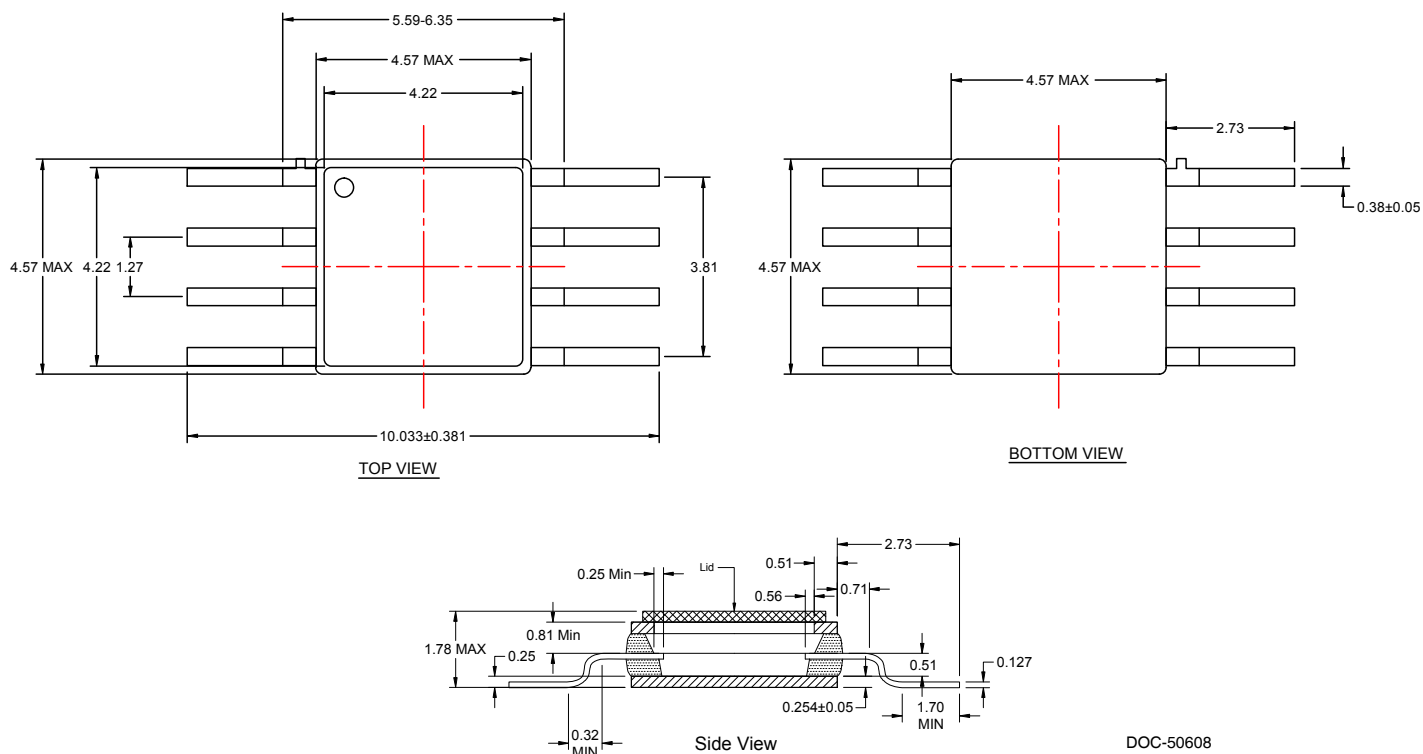
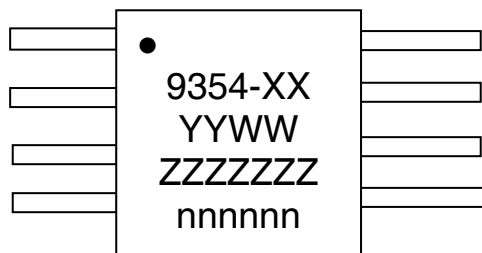


Figure 15. Top Marking Specifications



- = Pin 1 indicator
- 9354-XX = Part number (XX will be specified by the PO and/or the assembly instructions)
- YYWW = Date code, last two digits of the year and work week
- ZZZZZZZ = Lot code (up to seven digits)
- nnnnnn = Serial number of the part (up to six digits)

Table 6. Ordering Information

Order Code	Description	Package	Shipping Method
9354-01*	PE9354 Engineering samples	8-lead CFP	50 / Tray
9354-11	PE9354 Flight units	8-lead CFP	50 / Tray
9354-00	PE9354 evaluation kit	Evaluation kit	1 / Box

Note: * The PE9354-01 devices are engineering sample (ES) prototype units intended for use as initial evaluation units for customers of the PE9354-11 flight units. The PE9354-01 device provides the same functionality and footprint as the PE9354-11 space qualified device, and intended for engineering evaluation only. They are tested at +25 °C only and processed to a non-compliant flow (e.g. no burn-in, non-hermetic, etc). These units are non-hermetic and are not suitable for qualification, production, radiation testing or flight use.

Sales Contact and Information

For sales and contact information please visit www.psemi.com.

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