AN RFMD® REFERENCE MANUAL

RF205x Frequency Synthesizer User Guide

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REVISION HISTORY

Version	Date	Description of change(s)	Author(s)
Version 0.1	March 2008	Initial Draft.	CRS
Version 1.0	June 2008	Amended for RF205x family. Sections added.	CLS
Version 2.0	March 2010	Frequency corrections. Images updated.	CLS

1. INTRODUCTION

The basic philosophy behind the RF205x family of RF components offers a high-linearity broadband mixer along with frequency generation capability to support an RF frequency range of 30MHz to 2500MHz, and an IF frequency range of 30MHz to 2500MHz.

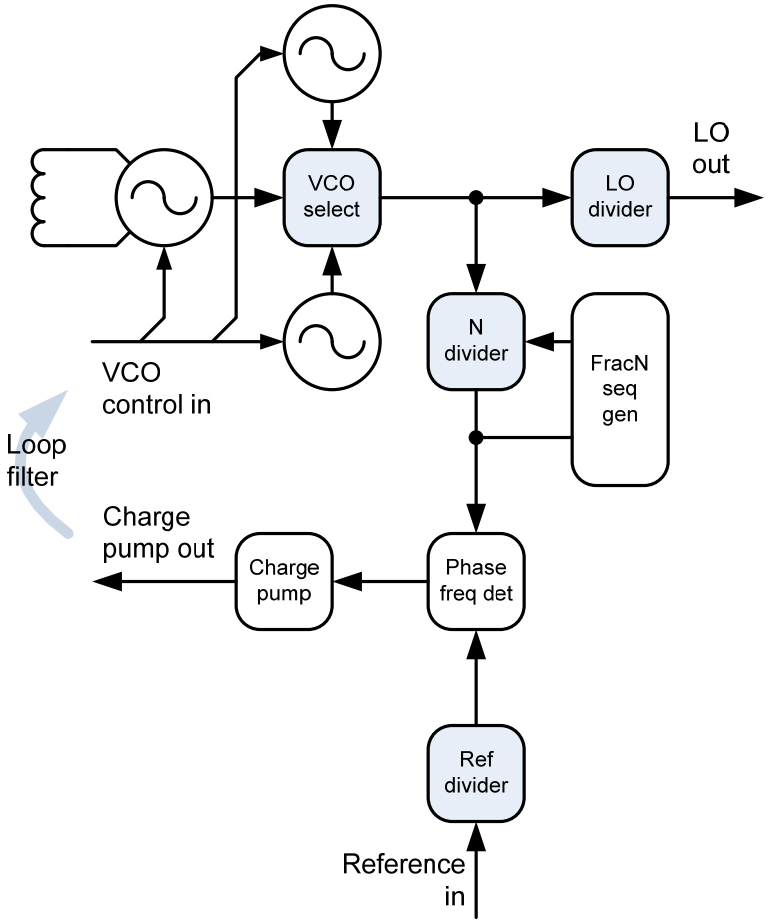
The integrated voltage controlled oscillators cover the frequency range from approximately 1200MHz to 2400MHz. A local oscillator divider divides the VCO output by 1, 2, or 4 to generate the local oscillator signal in the 300MHz to 2400MHz range.

A Fractional-N PLL operates on the VCO output to lock the signal to the reference source which can be either generated from a crystal or provided from an external source.

The RF205x synthesizer has been designed to give flexibility in device programming and hardware configuration. This document describes information for programming the RF205x synthesizer, and for optimizing the synthesizer performance for the particular application.

A number of devices are available in the RF205x family. Some of these include two mixers, some have one mixer with an internal VCO or support for an external VCO. In each case, the programming of the operating frequency is the same.

2. SYNTHESIZER PROGRAMMING



Simplified Frequency Synthesizer Block Diagram

The figure above shows a block diagram of the frequency synthesizer used on the RF205x product range. The blocks that need to be programmed are highlighted and are the subject of this section of the User Guide.

2.1 REFERENCE SIGNAL OVERVIEW

The PLL is intended for use with a reference frequency signal between 10MHz to 104MHz. A reference divider (divide by 1 to 7) is included and should be programmed to limit the frequency at the phase detector to a maximum of 52MHz.

An external reference signal can be input on the XTALIPN (or XTALIPP) pin of the device or a crystal resonator can be placed between the XTALIPP and XTALIPN pins. On-chip capacitors are used to ensure the correct load capacitance is presented to the resonator. The integrated oscillation sustaining circuit will support a crystal resonant frequency of up to 52MHz.

The phase detector frequency must be chosen with care since it will affect the spurious frequencies present in the spectrum of the LO signal, the minimum step size available in the synthesizer, and the maximum frequency of the VCO output. It will also effect the times that the VCO calibrations take.

A higher-phase detector frequency will lead to lower reference spurious since the loop filter is better able to filter them. It will also reduce the amount that reference and charge pump noise are increased by the phase locked loop, given by $20\log_{10}N$.

A lower-phase detector frequency will give a finer frequency resolution step due to the length of the fractional part of the divider ratio:

$$F_{STEP} = F_{PD} / 2^{24}$$

A lower-phase detector frequency may restrict the maximum output of the synthesizer due to restrictions on the divider ratio N:

$$F_{MAX} = MAX(2400, F_{PD} * 2^{9})$$

F_{PD} (MHz)	F_{STEP} at F_{MAX} (Hz)	F_{MAX} (MHz)
52	3.1	2400
26	1.5	2400
5	0.3	2400
2.5	0.15	1280

The minimum value of FPD at which the maximum VCO frequency of 2400MHz can be achieved:

$2400/2^9 \approx 4.69$MHz.

2.2 FRACTIONAL-N PLL OVERVIEW

The RF205x devices contain a charge pump-based, fractional-N phase locked loop (PLL) for controlling the three VCOs on the IC. The PLL includes automatic calibration systems to counteract the effects of process and environmental variations, ensuring repeatable lock time and noise performance.

The PLL will lock the VCO to the frequency F_{VCO} according to:

$$F_{VCO} = N * F_{REF} / R$$

where N is the programmed fractional N divider value, F_{REF} is the reference signal frequency at the XTALIP pin, and R is the programmed reference divider value (1 to 7).

The N divider is a fractional divider, containing a dual-modulus prescaler and a digitally spur-compensated fractional sequence generator to allow fine frequency steps of less than 3Hz. The N divider is programmed using the _N(8:0) and _NUM(23:0). First determine the desired divider value, N:

$$N = F_{VCO} * R / F_{REF}$$

_N(8:0) should be set to the integer part of N (in PLLx3).
_NUM should be set to the fractional part of N multiplied by 2^{24}, rounded as appropriate.

To program the device the _NUM value has to be broken into two parts:

_NUM_MSB is the most significant 16 bits (in PLLx1) and
_NUM_LSB is the least significant 8 bits (in PLLx2)

2.3 VCO SELECTION AND LO DIVISION

The frequency range of the local oscillator is achieved by using three integrated VCOs, each covering part of the frequency range. To ensure correct operation of the device it is important to select the appropriate VCO corresponding to the desired operating frequency range using the VCOSEL bits in the PLLx0 registers. The lowest frequency VCO requires an external printed inductor which has to have the correct dimensions to operate over the right frequency range. The approximate frequency ranges covered by the three integrated VCOs are:

VCO#	VCOSEL	Frequency Range
1	00	1900 - 2400
2	01	1500 - 2000
3	10	1200 – 1600

Note: The exact range of VCO3 is determined by the external inductor dimensions.

2.4 EXAMPLE OF RF205X SYNTHESIZER PROGRAMMING

To determine how to program the synthesizer:

1. If 2400MHz > F_{LO} ≥ 1200MHz, then the LO divider ratio = 1.
   If 1200MHz > F_{LO} ≥ 600MHz, then the LO divider ratio = 2.
   If 600MHz > F_{LO} ≥ 300MHz, then the LO divider ratio = 4.
   The LO divider ratio (_LODIV) is found in PLLx0.
2. The required VCO frequency F_{VCO} = F_{LO} * LO divider ratio.
3. The required maximum step size and/or spurious requirements are used to determine the reference divider ratio (CLK_DIV in CFG4).
4. The synthesizer division ratio is then calculated using the phase detector frequency and the calculated VCO frequency.

For example, to generate a local oscillator at 906MHz using a 42MHz crystal with a step size of less than 1Hz:

F_{LO} = 906MHz therefore the required LO divider ratio is 2, hence

F_{VCO} = 906 * 2 = 1812MHz

For a VCO frequency of 1812MHz it would be necessary to select VCO 2.

A 42MHz phase detector frequency will not meet the step size requirement, so the reference divider ratio is set to 2.

The required synthesizer division ratio is therefore:

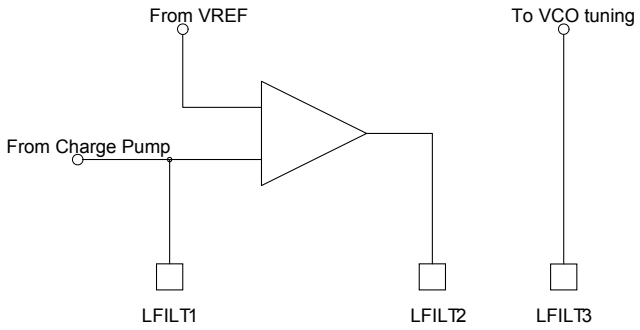
$N = F_{VCO} * R / F_{REF} = 1812 * 2 / 42 = 86.285714285714$

The _N value is set to 86, equal to the integer part of N, and the _NUM value is set to the fractional part of N multiplied by 2^{24}, rounded to the nearest integer:

$\_NUM = (N - \_N) * 2^{24} = 0.285714285714 * 2^{24} \approx 4793490$
$\_NUM\_MSB$ = integer part of ($\_NUM / 2^8$) = 18725
$\_NUM\_LSB = \_NUM - (2^8 * \_NUM\_MSB) = 0$

3. LOOP FILTER OVERVIEW

An integrated op-amp and three external loop-filter pins are provided to accommodate a variety of loop filter configurations so that loop parameters such as lock-time, phase noise at certain offsets, and integrated phase error may be optimized.



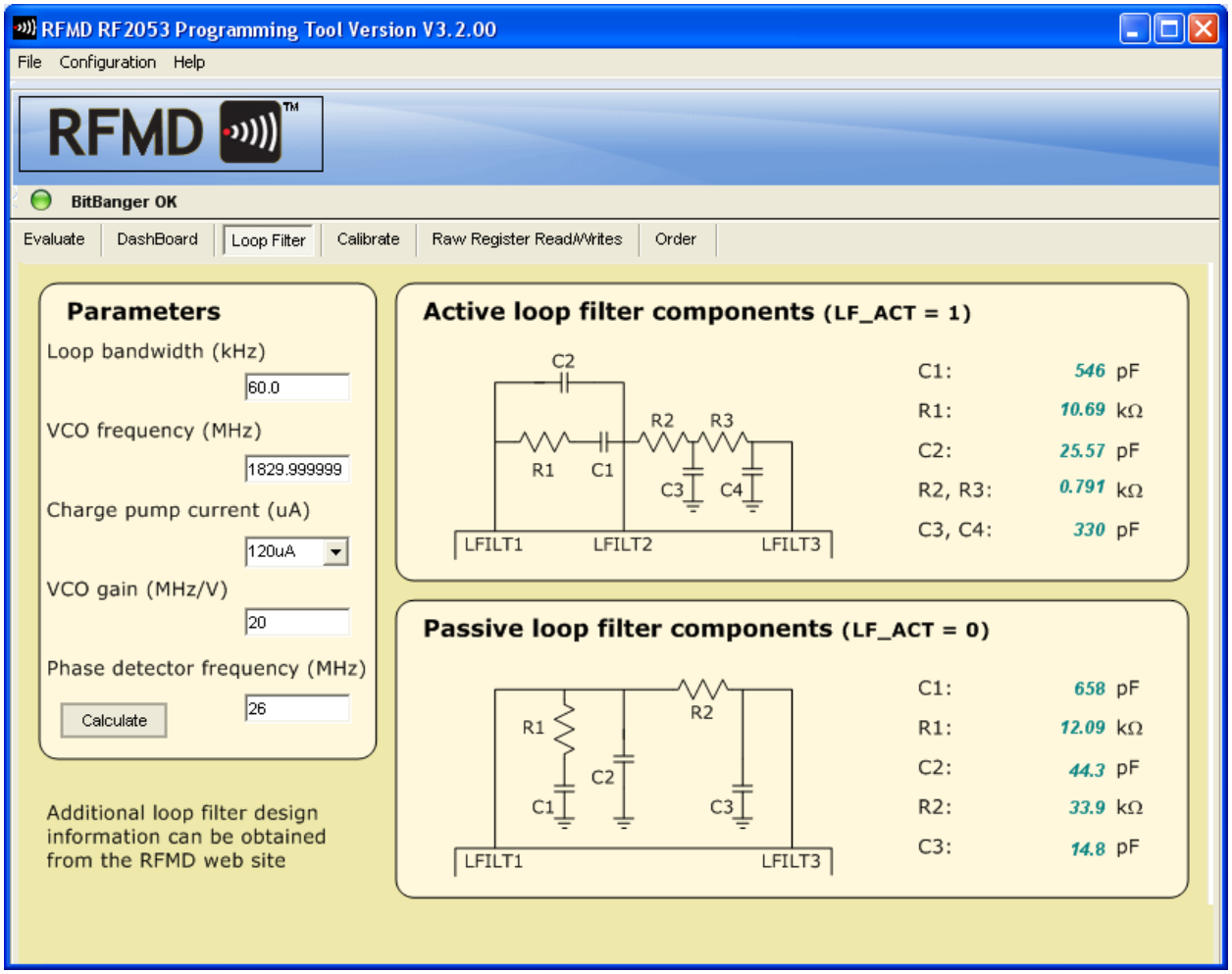
Components may be connected to LFILT1, LFILT2, and LFILT3 to construct either active or passive loop filters. The default device settings are for an active filter. Should a passive filter be required, the op-amp should be disabled by de-asserting the LFAMPEN bit in the CFG register. Note that the active filter has an inversion in the op-amp, so for a passive filter the phase detector polarity must be reversed. The PDP bit in the CFG register must be set low for a passive filter.

For passive loop filter designs, care must be taken since the charge pump output compliance voltage range is limited. With an active filter this is not a problem, since the op-amp provides gain between the charge pump output and VCO tuning input.

The charge pump output voltage compliance range is approximately +0.7V to +1.5V, so the VCO tuning voltage should be kept within this range. Outside of this range, charge pump non-linearity may cause increased phase noise. Normally the synthesizer coarse tune calibration will keep the VCO tuning voltage centered and within the compliant voltage range as the VCO frequency drifts, for example, with temperature.

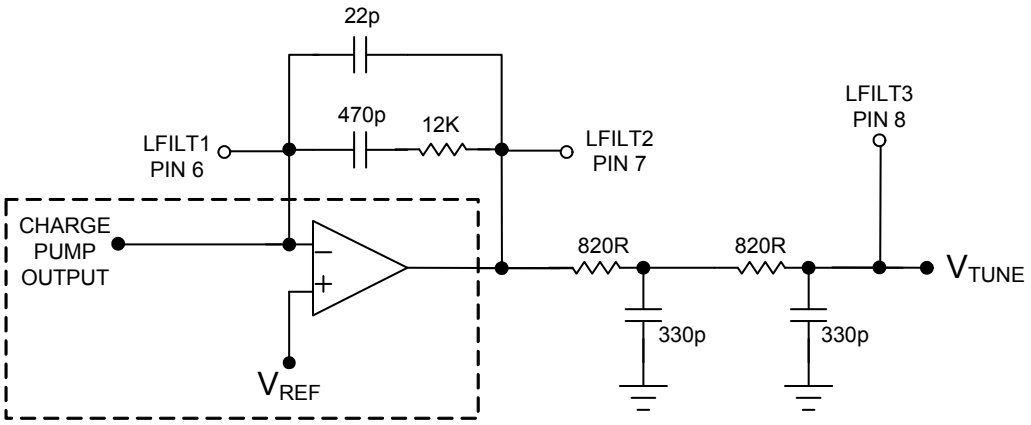
In some applications where the coarse tune calibration is disabled for fast locking, or if the device is kept enabled for long periods, then the VCO tuning voltage may vary outside the compliance range. Note that the coarse tune calibration occurs after the device is enabled. In these cases an active loop filter should always be used.

3.1 LOOP FILTER CALCULATOR



The RF205x Programming Tools GUI contains a Loop Filter Calculator tab. This basic calculator tool can be used to determine component values for active or passive loop filters. The input parameters for the synthesizer design are entered in the boxes on the left. The calculated component values are displayed on the right. The nearest standard R or C value will need to be selected.

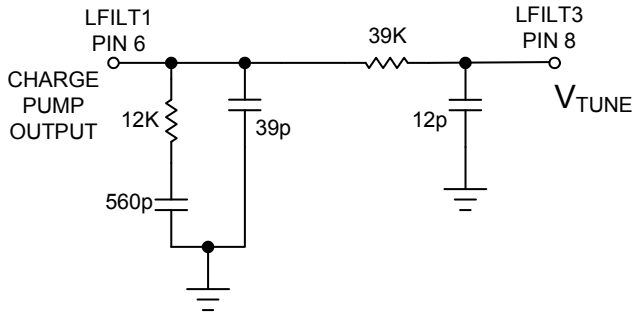
3.2 ACTIVE LOOP FILTER EXAMPLE



This is the default loop filter fitted on all of the RF205x evaluation boards (except for the RF2053 which requires a different loop bandwidth dependent on the external VCO used). The default register settings are for an active loop filter:

- 60KHz Loop Bandwidth
- Default setting, LF_ACT=1 & PDP=1

3.3 PASSIVE LOOP FILTER EXAMPLE



There are component placements on the evaluation boards enabling modification to a passive loop filter. The diagram above is an example of a passive loop filter that could be used. To use a passive loop filter requires settings in the Configuration 1 register to be changed:

- 60KHz Loop Bandwidth
- Set LF_ACT=0 & PDP=0

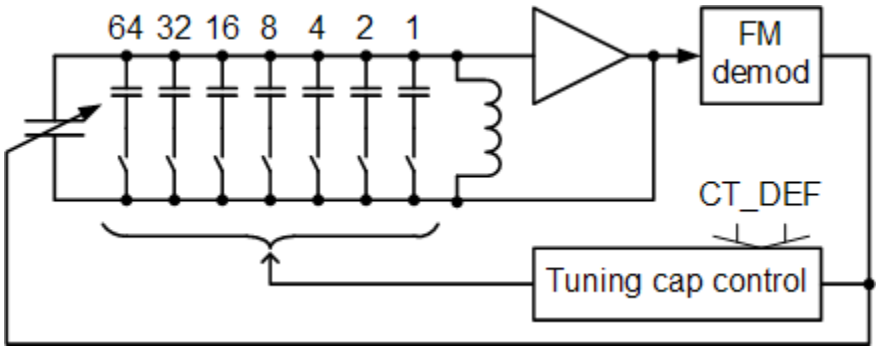
4. SYNTHESIZER CALIBRATION

The RF205x fractional-N synthesizer has two calibration systems to counteract the effects of process and environmental variations:

- The coarse tuning calibration uses a bank of switched capacitors to centre the VCO tuning range. This is activated by default and will be used in most applications.
- The VCO gain calibration is used for applications with large LO frequency ranges. The charge pump current is varied to maintain the loop filter response as VCO gain and division ratio N vary.

This section gives a brief overview of the calibration systems. For more details please refer to the *RF205x Calibration User Guide*.

4.1 COARSE TUNING CALIBRATION (CT_EN)



Coarse tuning calibration is activated by default, and occurs when the device is enabled. The diagram above shows the calibration operation; the VCO tuning capacitance is changed to set the tuning voltage to a defined value using a frequency-locked loop.

The switched tuning capacitors are automatically adjusted to bring the tuning voltage close to the value defined by CT_V. The default value of CT_V is 16 (mid-range) and gives a tuning voltage of around +1V.

Normal operation is to switch the device to standby, program it, and enable the device. The calibration is performed as part of the synthesizer settling time.

Note that for applications requiring a fast lock time the coarse tuning calibration can be disabled.

4.2 VCO GAIN CALIBRATION (KV_EN)

The VCO gain calibration works by measuring the VCO gain and correcting the charge pump current to maintain loop bandwidth. It corrects for both VCO gain and divide ratio N.

The VCO gain calibration is required only for applications with large LO frequency ranges. Here the divide ratio N and the VCO gain will vary significantly, which will change the loop response. It will be desirable to maintain a constant loop bandwidth over the whole LO operating range. The VCO gain calibration enables optimal synthesiser performance over a wide range of LO frequencies.

The VCO gain calibration will not be required for most applications where the LO frequency is fixed or only varies over a small range. An exception to this would be if the LO frequency range requires switching between VCOs, where the VCO gains will be different at the top and bottom of the two VCO ranges.

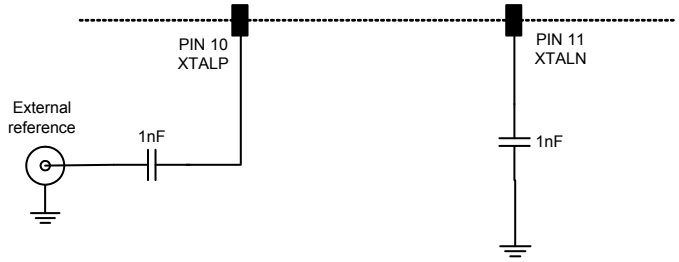
5. REFERENCE OSCILLATOR

The RF205x devices can be run from an external reference signal source, or a crystal resonator can be used with the integrated reference oscillator circuit.

5.1 EXTERNAL REFERENCE

An external reference of between 10MHz and 104MHz can be used. The reference signal is applied to the XTALP pin via suitable AC coupling. The XTALN pin must be decoupled to ground as shown in the diagram below.

Note: The recommended signal level at the XTALP pin is between 500mVp-p and 1500mVp-p.

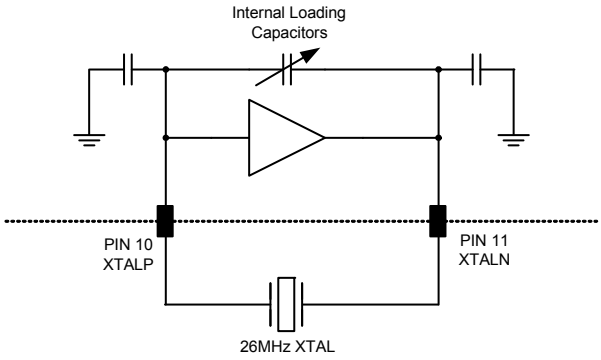


5.2 CRYSTAL OSCILLATOR

The integrated reference oscillator circuit operates with crystals of 10MHz to 52MHz center frequency.

The oscillator circuit contains internal loading capacitors. No external loading capacitors are required, depending on the crystal loading specification. The internal loading capacitors are a combination of fixed capacitors and an array of switched capacitors. The switched capacitors can be used to tune the crystal oscillator onto the required center frequency and minimize frequency error. The PCB stray capacitance, oscillator input, and output capacitance will also contribute to the crystal's total load capacitance.

A simplified block diagram of the crystal oscillator circuitry is shown below:

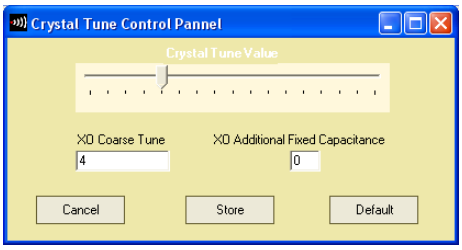


The register settings in register Configuration 4 for the switched capacitors are as follows:

- Coarse Tune XO_CT (4 bits) 15 * 0.55pF, default 0100
- Fine Step XO_CR_S (1 bit) 1 * 0.25pF, default 0

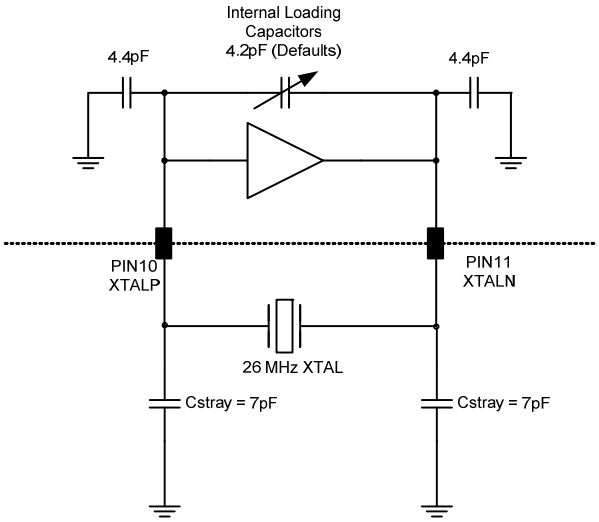
The default register settings give approximately 10pF loading, in combination with the stray capacitances mentioned.

5.2.1 Crystal Tuning



The RF205x Programming Tools GUI contains a Crystal Tune function, opened from the Dashboard tab. This allows the internal crystal loading capacitance to be varied easily.

5.2.2 Calculating Crystal Load Capacitance



PCB stray capacitance is assumed to be 2pF. Oscillator input and output capacitance are assumed to be 5pF. This gives a total stray capacitance on each pin of 7pF.

The switched capacitor array is 2.2pF in parallel with a fixed 2pF across crystal. The fixed internal shunt capacitance is 4.4pF on each pin. Summing these capacitors gives a total capacitance of 9.9pF.

5.2.3 26MHz Crystal Specification

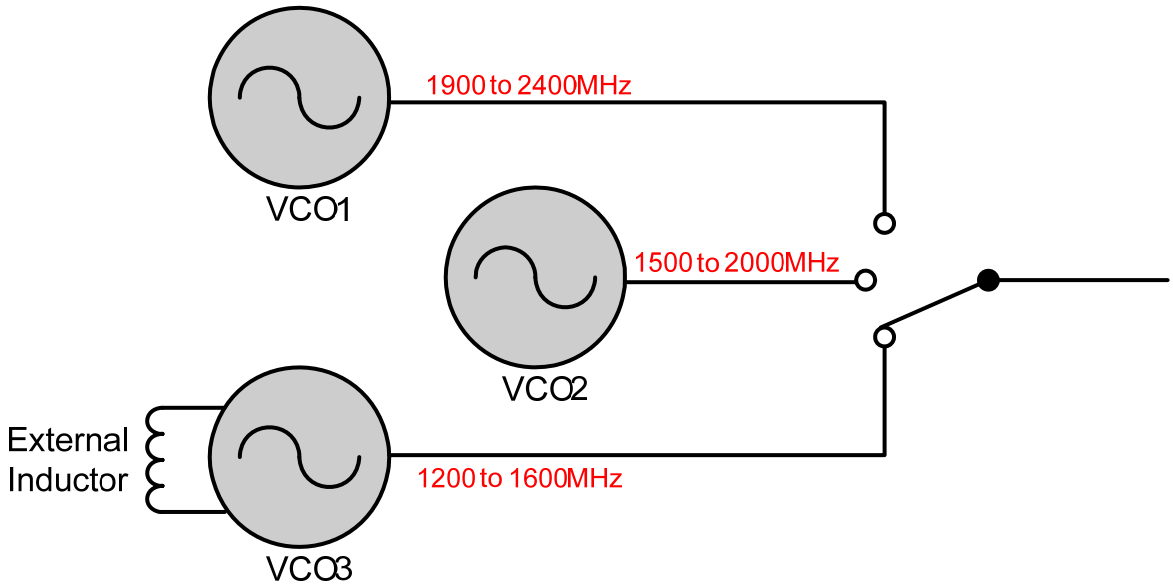
The RF205x evaluation boards are supplied with a standard 26MHz crystal fitted. Further specifications include:

- Package: 3.2*2.5
- Load capacitance: 10pF
- Accuracy: ±10ppm
- Temperature stability: ±10ppm
- Pullability: 16ppm/pF to 22ppm/pF

6. VOLTAGE CONTROLLED OSCILLATORS

There are three VCOs in both the RF2051 and RF2052, each covering a section of the 1200MHz to 2400MHz frequency range. The two high frequency VCOs (VCO1 and VCO2) are integrated entirely on the device. The low frequency VCO (VCO3) uses an external inductor, which is normally tuned to cover the 1200MHz to 1600MHz range. It can be designed to resonate the VCO at other frequencies if required, offering flexibility.

The internal VCO arrangement of the RF2051 and RF2052 is shown below, along with the approximate frequency range of each VCO.



The RF2053 has been designed to be used with an external VCO. This gives the advantage of the improved phase noise that an external VCO can offer, compared to the integrated CMOS VCOs.

There are variants of the RF2051 with a single VCO; the RF2057 (VCO1 only) and RF2059 (VCO2 only). The RF2056 also has a single VCO, which can be tuned between 200MHz and 500MHz using external inductors. These parts all have two mixers.

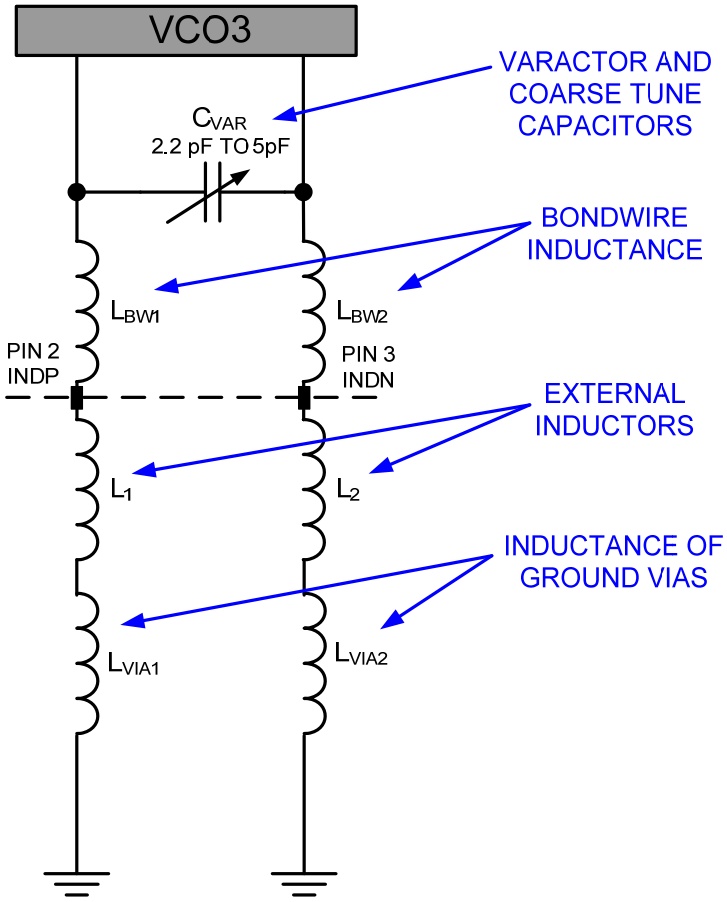
6.1 DESIGN OF VCO3 INDUCTOR ON RF2051 AND RF2052

VCO3 is a differential LC Oscillator, and uses external inductors. The inductor could be realized with:

- Discrete High Q Inductors
- Microstrip Lines

The microstrip line is the preferred choice. There is no BOM cost, and the size is compact at these frequencies taking up little board space. Since the inductor value is small then it may be difficult to implement with discrete inductors, and inductor standard values available may not give the correct frequency range. High Q inductors will also add to the BOM cost.

6.1.1 A simple model of the VCO3 differential resonator



6.1.2 Calculating the Required Inductance

Using the formula for resonant frequency:

$$Fo = \frac{1}{2\pi\sqrt{LC}}$$

Calculating for inductance gives a value of 4.0nH. This covers the required frequency range of 1200MHz to 1600MHz with the available capacitance range. The varactor and coarse tune switched capacitors give a total capacitance range of 2.2pF to 5pF.

Capacitance	Inductor	Resonant Frequency
2.2pF	4.0nH	1697MHz
3.6pF	4.0nH	1326MHz
5pF	4.0nH	1125MHz

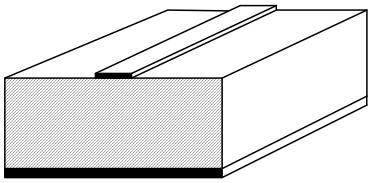
This total inductance gives the required value in each arm of 2nH. This is the combined inductance of the package bondwires, the external inductor, and the inductance of ground vias, giving:

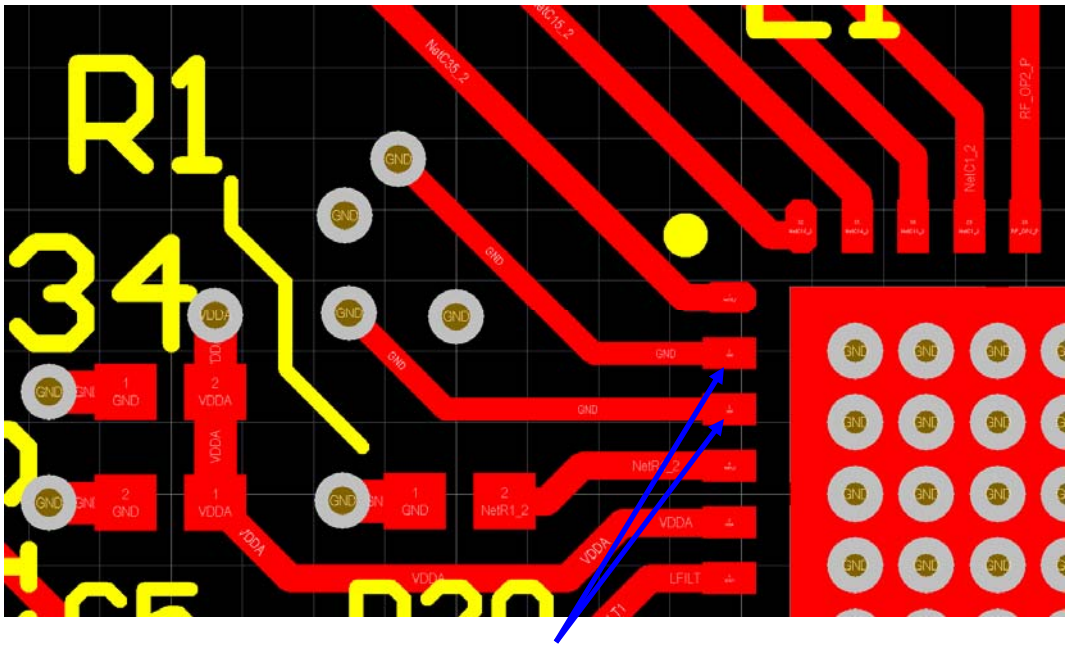
$$L_{BW1} + L_1 + L_{VIA1} = L_{BW2} + L_2 + L_{VIA2} = 2nH$$

Typically the bondwire inductance plus ground via inductance is 1nH, so the required value of each of the external inductors is 1nH.

On the RF2051/RF2052 evaluation boards the microstrip inductor dimensions are approximately:

- Length = 125mil
- Width = 8mils
- Height above ground plane = 12mil
- Substrate FR4, Ɛr = 4.6
- Zo = 77Ω



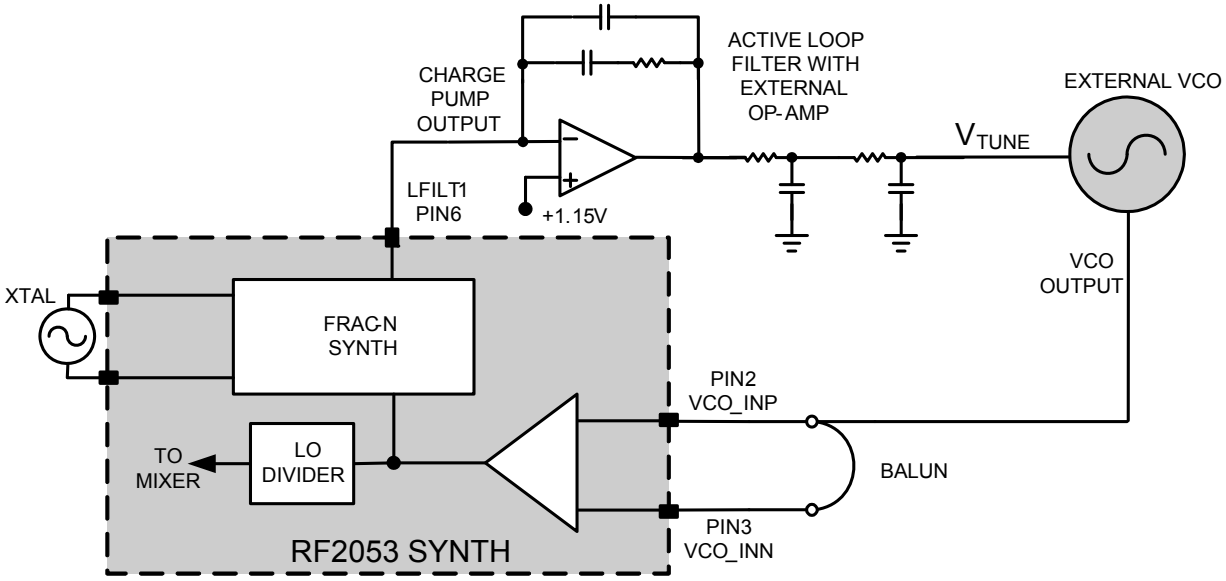


VCO3 inductor layout on the RF2051/RF2052 evaluation boards

This section has given a simple guide to the design of the VCO3 external inductors. Every PCB layout is different. For instance, the distance between PCB layers or the size of via holes may vary. The microstrip inductors should be designed and modeled for each application to ensure that the correct frequency range is achieved.

6.2 THE RF2053 WITH EXTERNAL VCO

6.2.1 Block Diagram of the RF2053 Synthesizer with External VCO and Op-Amp



For applications requiring very low phase noise, the RF2053 can be used with an external low noise VCO and op-amp. The RF2053 supports an external VCO frequency range of 30MHz to 2400MHz.

The external op-amp and its power supplies must be selected such that the op-amp can provide the full tuning voltage range required for the VCO. The positive terminal of the op-amp should be set to a reference of about +1.15V, in the center of the charge pump output voltage range. Care should be taken as any noise on this reference voltage will inject noise into the phase locked loop.

When programming the RF2053 there are two register bits that must be set to enable operation with an external VCO. The EXT_VCO bit in register CFG1 must be set to 1, and VCO3 must be selected by setting the P2_VCOSEL bits in register PLL2x0 to 10. Otherwise the programming is the same as for the RF2052, except that the frequency range must be restricted to that of the external VCO.

The LO divider can be used to divide the VCO output by 1, 2, or 4 if required. For more information, refer to the RF2053 data sheet.

7. SOME TIPS ON REDUCING PHASE NOISE

1. Frequency Plan

An important part of the synthesizer design is the frequency plan. The divide ratio N should be kept as low as possible to reduce the multiplication of phase noise within the loop bandwidth. The multiplication factor within the loop is $20\log_{10} N$. The fractional-N synthesizer gives the flexibility to minimize N, whatever the required channel step size or raster, and operate with a high phase detector frequency. The frequency plan is also important when considering spurious signals. For example reference and phase detector frequencies should be considered carefully as their harmonics may fall inside the IF and RF signal bands.

2. Passive Loop Filter

The RF205x devices can be used with a passive loop filter. This can reduce the phase noise at frequency offsets in the region of 100kHz since there is no noise contribution from the op-amp. There are disadvantages, however; the tuning range is restricted by the charge pump compliance voltage range. The active loop filter also offers a sharper cut-off.

3. Loop Filter Design

The loop filter is a critical component of the synthesizer, and can be optimized for a number of parameters including settling time and phase noise. For some applications phase noise at certain offsets will be critical, whereas for others the integrated phase error is more important. Generally lowering the loop bandwidth will reduce the phase noise, which is not always simple. The loop bandwidth tends to be set by the point at which the synthesizer noise floor meets the VCO phase noise. Lowering the loop bandwidth will cause peaking of the phase noise, since outside the loop bandwidth the phase noise is dominated by the VCO noise which will be higher than the noise floor within the loop. Lowering the loop bandwidth will also increase settling time.

A rough approximation of the relationship between settling time and loop bandwidth is given below. This gives a rough guideline, however the loop response should be modeled to give a more accurate indication:

$$T_{settle} = \frac{2.5}{F_{loop\_bw}}$$

As an example, a settling time of 42µsec should be achievable with a loop bandwidth of 60KHz. The startup and calibration times of the device need to be considered as well as the PLL settling time.

Loop filter design is the focus of many references and textbooks, so it will not be covered further here. The RF205x Programming Tools GUI contains a simple loop filter tool for calculating component values for both passive and active loop filter configurations.

4. Layout

The layout of the PCB is obviously important at these frequencies. Good layout is required to achieve the optimal phase noise of the RF205x device. Areas of particular concern are the external inductor for VCO3, the loop filter, and the reference crystal or oscillator.

5. Supply Decoupling

High frequency decoupling capacitors are required close to the analog and digital supply pins, and to the analog decoupling pin of the RF205x device. The best decoupling value will depend on the application frequency and the impedance of the capacitor at that frequency. Decoupling capacitors in the region of 10nF to 100nF are also recommended to attenuate noise in the 10 to 100MHz range.

Power supply noise is a major cause of high-phase noise and spurious on synthesizer designs. In particular, low frequency noise, which could be from a switching regulator, is problematic. Depending on the noise level on the 3V power supply to the device, low frequency decoupling may be required, typically 10uF. In worst case conditions some series filtering may also be needed.

The RF2053 of course requires an external VCO. It is critical that the supply to the VCO is decoupled and filtered adequately. Low frequency noise is again problematic and can pull the VCO or cause spurious.

6. Control Line Filtering

The control lines to the RF205x device need to be decoupled to attenuate any noise from the micro-controller and digital circuitry. Digital noise can affect the synthesizer, particularly if the control lines are routed close to sensitive circuitry such as the loop filter. Low pass filtering in the form of an RC network could be employed to further reduce noise on the control lines.

7. LDO Bypass

The RF205x devices contain several low drop-out (LDO) regulators that power the internal circuit blocks. If you are running the device from a low noise 3V power supply, then the phase noise may be improved by using the LDO bypass function. This bypasses the on-chip LDO regulators, so the internal circuits run off the incoming supply.

LDO_BYP is bit 8 of the Test register (not listed in data sheet). The default setting is 0 to enable the on chip LDOs. Set test register bit 8 to LDO_BYP = 1 to disable and bypass the LDOs. Bear in mind that if the supply is noisy, this may make the phase noise worse.

8. Charge Pump Leakage Setting

The default charge pump leakage setting is CPL = 10 (leakage setting 2). Setting CPL=01 (leakage setting 1) should reduce phase noise within the loop bandwidth by about 1dB. The CPL bits are in the Config 1 register, bits 5 and 6.

This is only recommended in certain conditions as this setting will reduce the linearity of the charge pump. This could cause the fractional divider noise to mix with the reference frequency and increase phase noise close to the synthesizer centre frequency. The Fractional-N synthesizer contains a sigma delta modulator that pushes the fractional divider noise out to offsets where it is attenuated by the loop filter.

9. VCO Selection

Certain LO frequencies lie within the frequency range of two of the VCOs, for example at 2000MHz. At 2000MHz, the RF205x GUI will automatically select VCO2. The VCOSEL bits in PLL1x0 or PLL2x0 registers will be set to 01; however, 2000MHz also lies within the range of VCO1. The bottom end of VCO1's range gives a lower Kvco to VCO2, narrowing the loop bandwidth. The VCO phase noise also improves at the lower end of the VCO's frequency range.

It is always better to select the lower end of one VCO's frequency range, rather then the higher end of the next VCO, as the phase noise is lower. When using a frequency near to the end of a VCO's range, the variations due to environment (temperature) and process must be considered.

10. Charge Pump Current

Varying the charge pump current will change the loop response. Reducing the charge pump current will reduce loop bandwidth for a given loop filter design. This parameter can be used to optimize the loop response and improve phase noise at a particular LO frequency. The loop response will vary with LO frequency since Kvco and N change as mentioned in section 4.

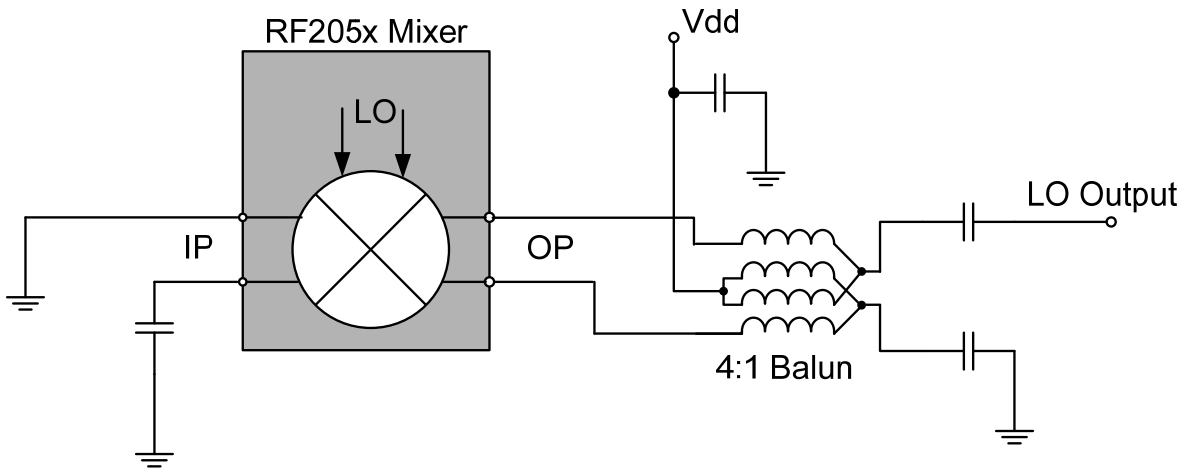
The charge pump current can be changed using charge pump setting CP_DEF, bits 0 to 5 in PLL1x0 or PLL2x0 registers. Default setting is 011111. Setting to maximum will give the lowest charge pump noise.

8. ACCESSING THE RF205X LO SIGNAL

The LO signal is routed from the LO dividers via buffers direct to the mixer's LO input port, so the LO signal is not accessible on any device output pin. The LO leakage can be measured on the mixer output, but the level will be too low for phase noise measurements or for other applications. The low level of LO leakage will also mean that the LO phase noise at high offsets >1MHz will be obscured by the device noise floor.

The double balanced mixer will by nature suppress the LO signal at the mixer output. Unbalancing the mixer by applying a DC offset or ground to one of the input pins means that the LO signal will be routed directly to the mixer output and not suppressed.

If the mixer of the RF205x device has one of the input pins grounded, then the LO signal will be available at the mixer output. The LO level will be +3dBm ± 3dBm at the mixer output, depending on LO frequency. The supply current will also increase by around 15mA.



8.1 LO MEASUREMENTS ON THE RF205X EVALUATION BOARDS

The following shows the modifications required to the RF205x evaluation board to apply an offset to the mixer input. A 0Ω resistor replaces the 100pF AC coupling capacitor. A convenient method is to connect a 50Ω SMA load to the RF input connector to give a ground connection, via 50Ω. Then the LO signal can be measured at the RF output connector. The load can be removed to revert back to normal measurements, but the test equipment connected to the input must be AC-coupled.