Product Specification

PE97042

3.5 GHz UltraCMOS® Integer-N PLL Radiation Tolerant for Space Applications

Features

- Low power @ 45 mA typical
- ÷10/11 dual modulus prescaler
- Phase detector output
- Serial or direct hardwired mode
- Phase noise figure of merit: –216 dBc/Hz
- SEU < 10^{-9} errors / bit-day
- 100 kRad (Si) total dose
- Easily modified to be pin compatible with the PE9704, packaged in a 44-lead CQFJ *(reference application note AN23 at www.psemi.com)*

Product Description

Peregrine's PE97042 is a high-performance integer-N PLL capable of frequency synthesis up to 3.5 GHz. The device is designed for superior phase noise performance while providing an order of magnitude reduction in current consumption, when compared with existing commercial space PLLs.

The PE97042 features a ÷10/11 dual modulus prescaler, counters, and a phase comparator as shown in *Figure 1*. Counter values are programmable through a serial or direct hardwired mode.

The PE97042 is optimized for commercial space applications. Single event latch up (SEL) is physically impossible and single event upset (SEU) is better than 10^{-9} errors per bit / day.

The PE97042 is manufactured on Peregrine's UltraCMOS® process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate, offering excellent RF performance and intrinsic radiation tolerance.

Figure 1. Block Diagram

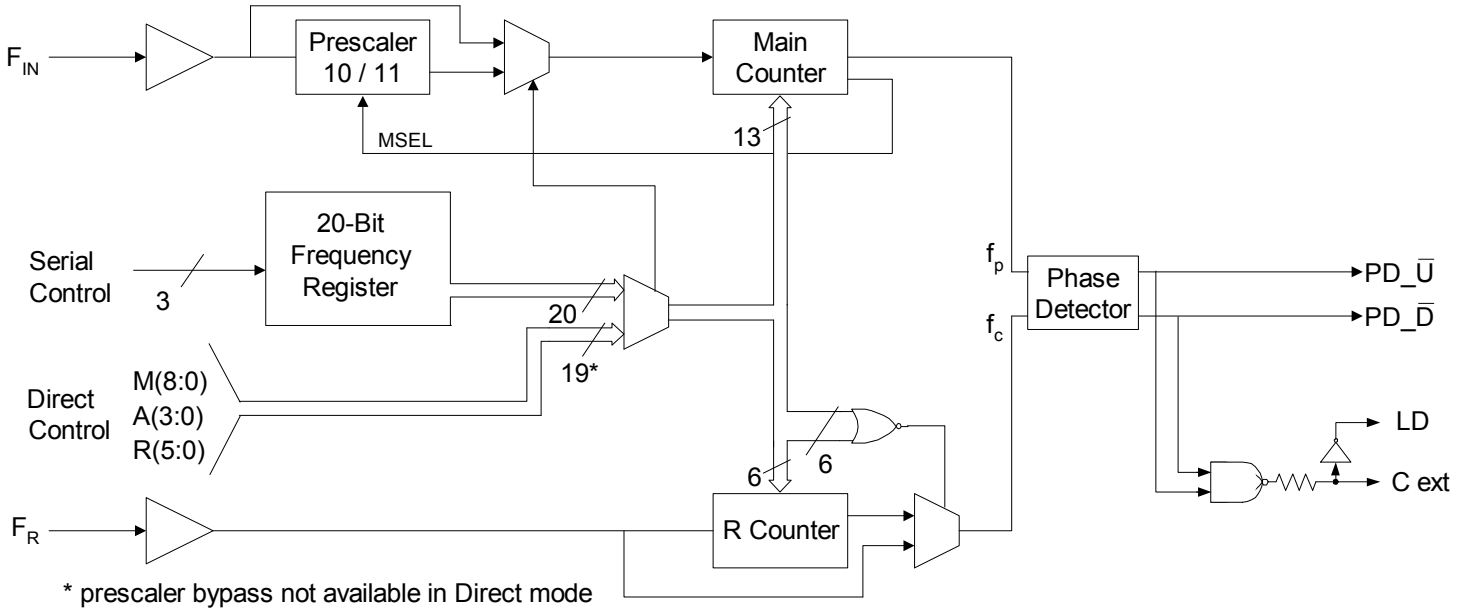


Figure 2. Pin Configurations (Top View)

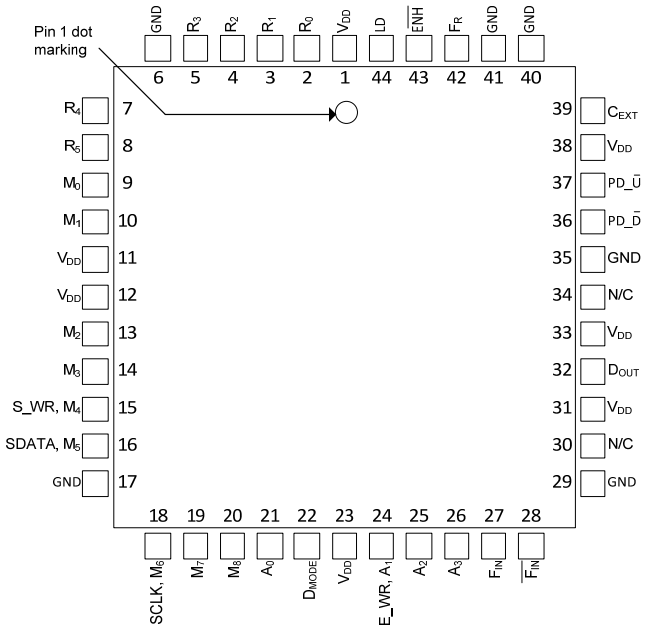


Figure 3. Package Type

44-lead CQFJ

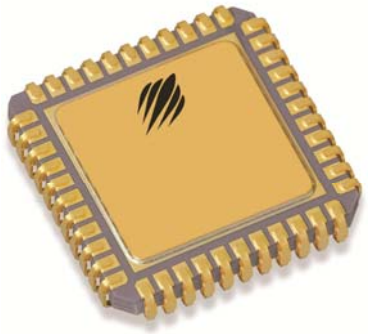


Table 1. Pin Descriptions

Pin #	Pin Name	Interface Mode	Type	Description
1	V_{DD}	Both	Note 1	Power supply input. Input may range from 2.85V to 3.45V. Bypassing recommended.
2	R_0	Direct	Input	R counter bit0
3	R_1	Direct	Input	R counter bit1
4	R_2	Direct	Input	R counter bit2
5	R_3	Direct	Input	R counter bit3
6	GND	Both		Ground
7	R_4	Direct	Input	R counter bit4
8	R_5	Direct	Input	R counter bit5 (MSB)
9	M_0	Direct	Input	M counter bit0
10	M_1	Direct	Input	M counter bit1
11	V_{DD}	Both	Note 1	Power supply input. Input may range from 2.85V to 3.45V. Bypassing recommended.
12	V_{DD}	Both	Note 1	Power supply input. Input may range from 2.85V to 3.45V. Bypassing recommended.
13	M_2	Direct	Input	M counter bit2
14	M_3	Direct	Input	M counter bit3
15	S_WR	Serial	Input	Frequency register load enable input. Buffered data is transferred to the frequency register on S_WR rising edge.
	M_4	Direct	Input	M counter bit4
16	SDATA	Serial	Input	Binary serial data input. Data is entered LSB first, and is clocked serially into the 20-bit frequency control register (E_WR “low”) or the 8-bit enhancement register (E_WR “high”) on the rising edge of SCLK.
	M_5	Direct	Input	M counter bit5
17	GND	Both		Ground

Table 1. Pin Descriptions (cont.)

Pin #	Pin Name	Interface Mode	Type	Description
18	SCLK	Serial	Input	Serial clock input. SDATA is clocked serially into either the 20-bit primary register (E_WR "low") or the 8-bit enhancement register (E_WR "high") on the rising edge of SCLK.
	M_6	Direct	Input	M counter bit6
19	M_7	Direct	Input	M counter bit7
20	M_8	Direct	Input	M counter bit8 (MSB)
21	A_0	Direct	Input	A counter bit0
22	D_{MODE}	Both	Input	Selects direct interface mode (D_{MODE} = 1) or serial interface mode (D_{MODE} = 0)
23	V_{DD}	Both	Note 1	Power supply input. Input may range from 2.85V to 3.45V. Bypassing recommended.
24	E_WR	Serial	Input	Enhancement register write enable. While E_WR is "high", SDATA can be serially clocked into the enhancement register on the rising edge of SCLK.
	A_1	Direct	Input	A counter bit1
25	A_2	Direct	Input	A counter bit2
26	A_3	Direct	Input	A counter bit3 (MSB)
27	F_{IN}	Both	Input	Prescaler input from the VCO, 3.5 GHz max frequency. A 22 pF coupling capacitor should be placed as close as possible to this pin and terminated with a 50Ω resistor to ground.
28	$\overline{F_{IN}}$	Both	Input	Prescaler complementary input. A 22 pF bypass capacitor should be placed as close as possible to this pin and be connected in series with a 50Ω resistor to ground.
29	GND	Both		Ground
30	N/C		Note 3	No connect
31	V_{DD}	Both	Note 1	Power supply input. Input may range from 2.85V to 3.45V. Bypassing recommended.
32	D_{OUT}	Serial	Output	Data Out. The Main Counter output, R counter output, or dual modulus prescaler select (MSEL) can be routed to D_{OUT} through enhancement register programming.
33	V_{DD}	Both	Note 1	Power supply input. Input may range from 2.85V to 3.45V. Bypassing recommended.
34	N/C		Note 3	No connect
35	GND	Both		Ground
36	PD_$\overline{D}$	Both	Output	PD_$\overline{D}$ pulses down when f_p leads f_c
37	PD_$\overline{U}$	Both		PD_$\overline{U}$ pulses down when f_c leads f_p
38	V_{DD}	Both	Note 1	Power supply input. Input may range from 2.85V to 3.45V. Bypassing recommended.
39	C_{EXT}	Both	Output	Logical "NAND" of PD_$\overline{U}$ and PD_$\overline{D}$, passed through an on-chip, 2 kΩ series resistor. Connecting C_{EXT} to an external capacitor will low pass filter the input to the inverting amplifier used for driving LD.
40	GND	Both		Ground
41	GND	Both		Ground
42	F_R	Both	Input	Reference frequency input
43	$\overline{ENH}$	Both	Output	Enhancement mode. When asserted low ("0"), enhancement register bits are functional..
44	LD	Serial	Output	Lock detect output, the open-drain logical inversion of C_{EXT}. When the loop is locked, LD is high impedance; otherwise LD is a logic low ("0").

Notes: 1.V_{DD} pins 1, 11, 12, 23, 31, 33, 35, and 38 are connected by diodes and must be supplied with the same positive voltage level.
2. All digital input pins have 70 kΩ pull-up resistors to V_{DD}.
3. No connect pins can be left open or floating.

Table 2. Absolute Maximum Ratings

Symbol	Parameter/Condition	Min	Max	Unit
V_{DD}	Supply voltage	–0.3	4.0	V
V_I	Voltage on any input	–0.3	V_{DD} + 0.3	V
I_I	DC into any input	–10	+10	mA
I_O	DC into any output	–10	+10	mA
T_{STG}	Storage temperature range	–65	+150	°C
V_{ESD}	ESD voltage HBM*		1000	V

Note: * Human Body Model (MIL-STD 883 Method 3015 C2)

Table 3. Operating Ratings

Symbol	Parameter/Condition	Min	Max	Unit
V_{DD}	Supply voltage	2.85	3.45	V
T_A	Operating ambient temperature range	–40	+85	°C

Exceeding absolute maximum ratings may cause permanent damage. Operation should be restricted to the limits in the Operating Ratings table. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the specified rating specified in *Table 2*.

Latch-Up Immunity

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

ELDRS

UltraCMOS devices do not include bipolar minority carrier elements and therefore do not exhibit enhanced low dose rate sensitivity.

Table 4. DC Characteristics @ V_{DD} = 3.3V, –40 °C < T_A < +85 °C, unless otherwise specified

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{DD}	Operational supply current;	V_{DD} = 2.85–3.45V				
		Prescaler disabled		15	20	mA
		Prescaler enabled		45	50	mA
Digital inputs: all except F_R, $\overline{F_{IN}}$ (all digital inputs have 70 kΩ pull-up resistors)						
V_{IH}	High level input voltage	V_{DD} = 2.85–3.45V	0.7 x V_{DD}			V
V_{IL}	Low level input voltage	V_{DD} = 2.85–3.45V			0.3 x V_{DD}	V
I_{IH}	High level input current	V_{IH} = V_{DD} = 3.45V			1	µA
I_{IL}	Low level input current	V_{IL} = 0, V_{DD} = 3.45V	–70			µA
Reference divider input: F_R						
I_{IHR}	High level input current	V_{IH} = V_{DD} = 3.45V			100	µA
I_{ILR}	Low level input current	V_{IL} = 0, V_{DD} = 3.45V	–100			µA
Counter and phase detector outputs: f_c, f_p						
V_{OLD}	Output voltage LOW	I_{out} = 6 mA			0.4	V
V_{OHD}	Output voltage HIGH	I_{out} = –3 mA	V_{DD} – 0.4			V
Lock detect outputs: C_{EXT}, LD						
V_{OLC}	Output voltage LOW, C_{EXT}	I_{out} = 100 µA			0.4	V
V_{OHC}	Output voltage HIGH, C_{EXT}	I_{out} = –100 µA	V_{DD} – 0.4			V
V_{OLLD}	Output voltage LOW, LD	I_{out} = 1 mA			0.4	V

Table 5. AC Characteristics @ V_{DD} = 3.3V, –40 °C < T_A < +85 °C, unless otherwise specified

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Control interface and latches (see *Figures 1* and *9*)						
f_{Clk}	Serial data clock frequency[1]				10	MHz
t_{ClkH}	Serial clock HIGH time		30			ns
t_{ClkL}	Serial clock LOW time		30			ns
t_{DSU}	SDATA set-up time after SCLK rising edge		10			ns
t_{DHLD}	SDATA hold time after SCLK rising edge		10			ns
t_{PW}	S_WR pulse width		30			ns
t_{CWR}	SCLK rising edge to S_WR rising edge		30			ns
t_{CE}	SCLK falling edge to E_WR transition		30			ns
t_{WRC}	S_WR falling edge to SCLK rising edge		30			ns
t_{EC}	E_WR transition to SCLK rising edge		30			ns
t_{MDO}	MSEL data out delay after F_{IN} rising edge	C_L = 12 pf			8	ns
Main divider (including prescaler)						
P_{F_IN}	Input level range	External AC coupling 275 MHz ≤ Freq ≤ 3.2 GHz	–5		5	dBm
		External AC coupling 3.2 GHz < Freq ≤ 3.5 GHz 3.15V ≤ V_{DD} ≤ 3.45V	0		5	dBm
Main divider (prescaler bypassed)						
F_{IN}	Operating frequency		50		300	MHz
P_{F_IN}	Input level range	External AC coupling	–5		5	dBm
Reference divider						
F_R	Operating frequency[3]				100	MHz
P_{F_R}	Reference input power[2]	Single-ended input	–2		10	dBm
Phase detector						
f_c	Comparison frequency[3]				50	MHz
SSB phase noise (F_{IN} = 1.9 GHz, F_R = 20 MHz, f_c = 20 MHz, LBW = 50 kHz, V_{DD} = 3.3V, temp = +25 °C)						
Φ_N	Phase noise	100 Hz offset		–89	–83	dBc/Hz
Φ_N	Phase noise	1 kHz offset		–95	–91	dBc/Hz
Φ_N	Phase noise	10 kHz offset		–102	–96	dBc/Hz
SSB phase noise (F_{IN} = 1.9 GHz, F_R = 20 MHz, f_c = 20 MHz, LBW = 50 kHz, V_{DD} = 3.0V, temp = +25 °C)						
Φ_N	Phase noise	100 Hz offset		–87	–70	dBc/Hz
Φ_N	Phase noise	1 kHz offset		–94	–81	dBc/Hz
Φ_N	Phase noise	10 kHz offset		–101	–89	dBc/Hz

Notes: 1. f_{clk} is verified during the functional pattern test. Serial programming sections of the functional pattern are clocked at 10 MHz to verify f_{clk} specification.
2. CMOS logic levels can be used to drive the reference input. If the V_{DD} of the CMOS driver matches the V_{DD} of PLL IC, then the reference input can be DC coupled. Otherwise, the reference input should be AC coupled.
3. Parameter is guaranteed through characterization only and is not tested.

Figure 4. RF Sensitivity vs Frequency (Typical Device at Temperature = +25 °C)

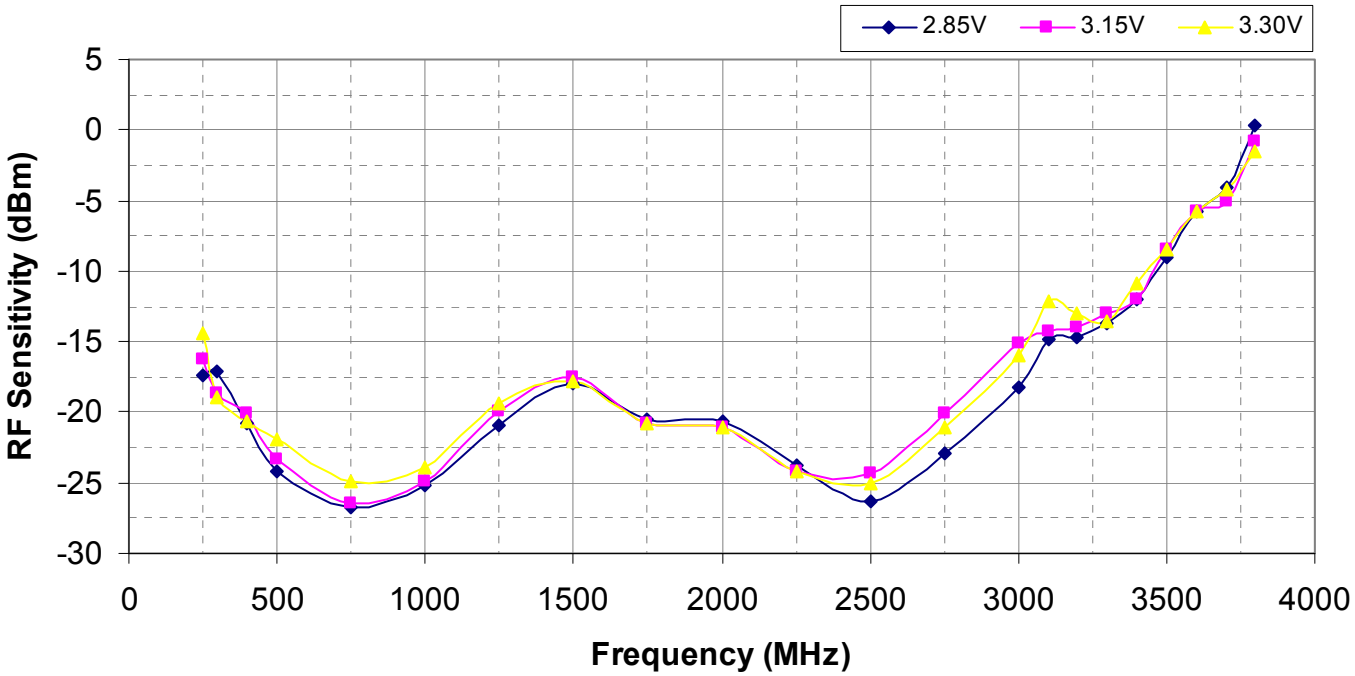


Figure 5. Typical Phase Noise for PE97042, V_{DD} = 3.3V, Temp = +25 °C, Fvco = 1.92 GHz, Fcomp = 20 MHz, Loop Bandwidth = 50 kHz

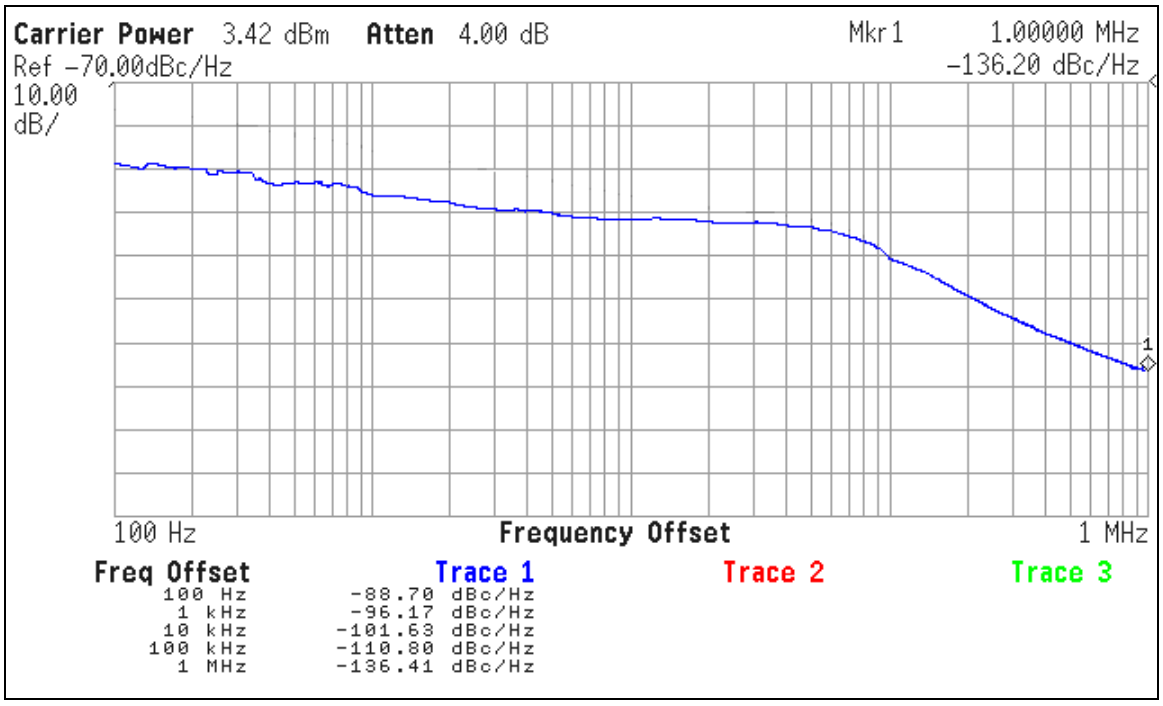


Figure 6. Equivalent Input Diagram: Reference Input

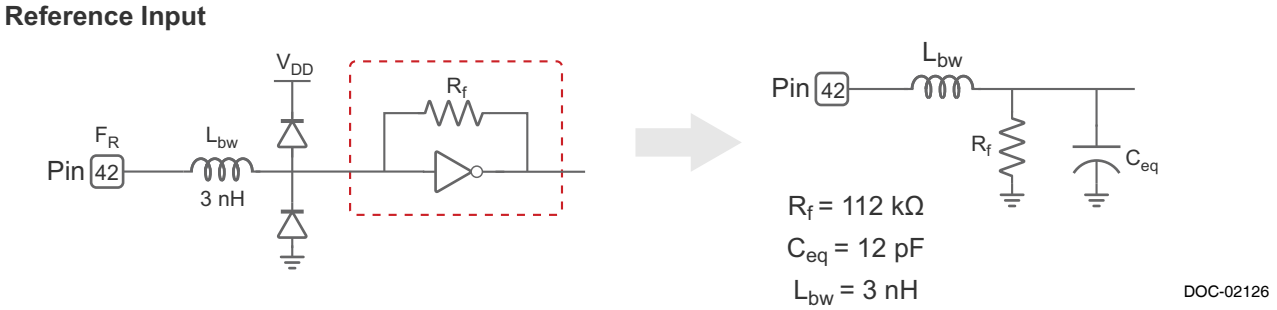


Figure 7. Equivalent Input Diagram: Main Input

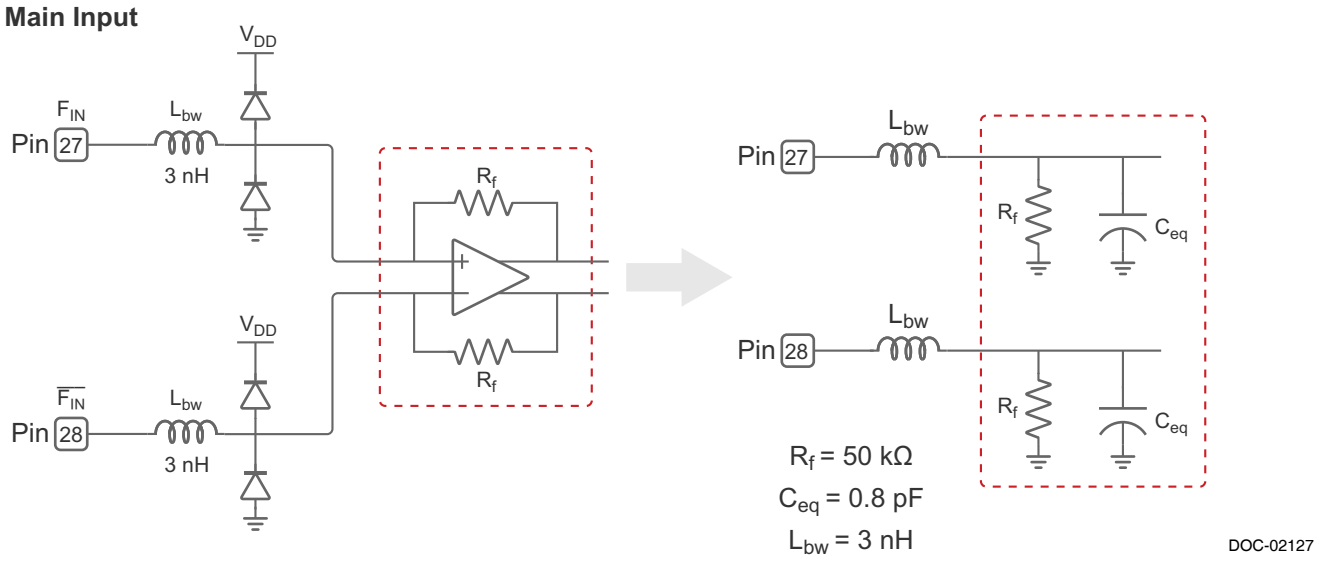
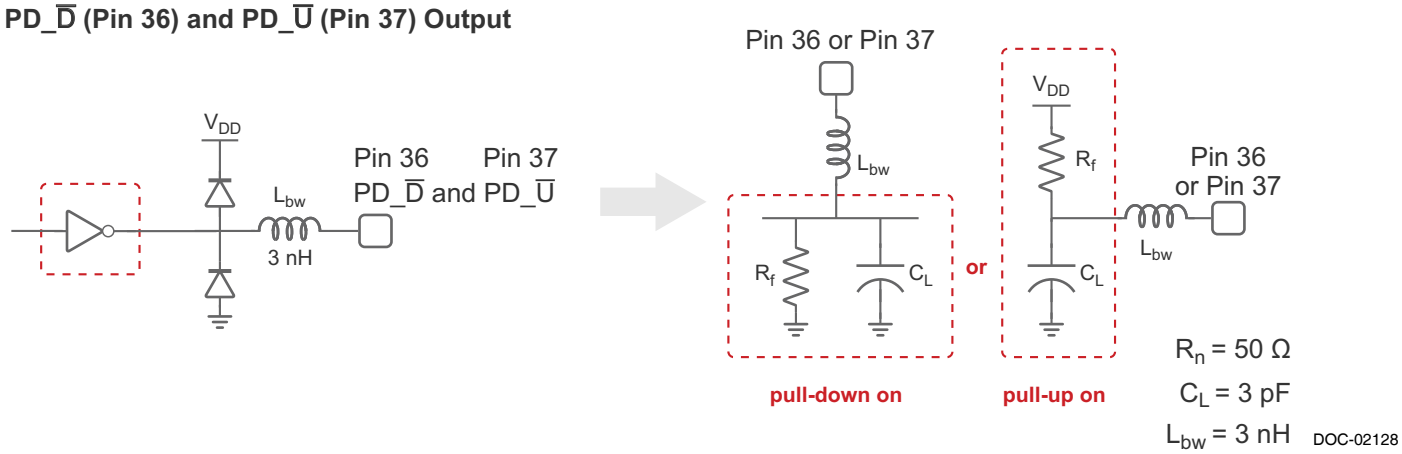


Figure 8. Equivalent Output Diagram: PD_$\overline{D}$ & PD_$\overline{U}$ Outputs



Functional Description

The PE97042 consists of a prescaler, counters, a phase detector, and control logic. The dual modulus prescaler divides the VCO frequency by either 10 or 11, depending on the value of the modulus select. Counters R and M divide the reference and prescaler output, respectively, by integer values stored in a 20-bit register. An additional counter (A) is used in the modulus select logic. The phase-frequency detector generates up and down frequency control signals. The control logic includes a selectable chip interface. Data can be written via a serial bus or hardwired directly to the pins. There are also various operational and test modes and a lock detect output.

Main Counter Chain

Normal Operating Mode

Setting the PB control bit "low" enables the ÷10/11 prescaler. The main counter chain then divides the RF input frequency (F_{IN}) by an integer derived from the values in the M and A counters.

In this mode, the output from the main counter chain (f_p) is related to the VCO frequency (F_{IN}) by the following equation:

$$f_p = F_{IN} / 10 \times (M + 1) + A \qquad (1)$$

where

$$A \leq M + 1,\ 1 \leq M \leq 511$$

When the loop is locked, F_{IN} is related to the reference frequency (F_R) by the following equation:

$$F_{IN} = [10 \times (M + 1) + A] \times [F_R / (R + 1)] \qquad (2)$$

where

$$A \leq M + 1,\ 1 \leq M \leq 511$$

A consequence of the upper limit on A is that F_{IN} must be greater than or equal to 90 x [F_R / (R + 1)] to obtain contiguous channels. The A counter can accept values as high as 15, but in typical operation it will cycle from 0 to 9 between increments in M.

Programming the M counter with the minimum allowed value of "1" will result in a minimum M counter divide ratio of "2".

Prescaler Bypass Mode

Setting the enhancement register bit PB "high" allows F_{IN} to bypass the ÷10/11 prescaler. In this mode, the prescaler and A counter are powered down, and the input VCO frequency is divided by the M counter directly. This mode is only available when using the serial port to set the frequency control bits.

The following equation relates F_{IN} to the reference frequency F_R:

$$F_{IN} = (M + 1) \times [F_R / (R+1)] \qquad (3)$$

where

$$1 \leq M \leq 511$$

Reference Counter

The reference counter chain divides the reference frequency F_R down to the phase detector comparison frequency f_c.

The output frequency of the 6-bit R counter is related to the reference frequency by the following equation:

$$f_c = F_R / (R + 1) \qquad (4)$$

where

$$0 \leq R \leq 63$$

Note that programming R with "0" will pass the reference frequency (F_R) directly to the phase detector.

Register Programming

Serial Interface Mode

Serial Interface mode is selected by setting the D_{MODE} input "low".

While the E_WR input is "low", serial data (SDATA input), B_0 to B_{19}, is clocked into a buffer register on the rising edge of SCLK, LSB (B_0) first. The contents from this buffer register are transferred into the frequency control register on the rising edge of S_WR according to the timing diagram shown in *Figure 9*. This data controls the counters as shown in *Table 6*.

While the E_WR input is "high", serial data (SDATA input), B_0 to B_7, is clocked into a buffer register on the rising edge of SCLK, LSB (B_0) first. The contents from this buffer register are transferred into the enhancement register on the falling edge of E_WR according to the timing diagram shown in *Figure 9*. After the falling edge of E_WR, the data provides control bits as shown in *Table 7*. These bits are active when the $\overline{ENH}$ input is "low".

Direct Interface Mode

Direct Interface mode is selected by setting the D_{MODE} input "high". In this mode, the counter values are set directly at external pins as shown in *Table 6*. All frequency control register bits are addressable except PB (it is not possible to bypass the ÷10/11 dual modulus prescaler in Direct mode).

Table 6. Frequency Register Programming

Interface Mode	$\overline{ENH}$	D_{MODE}	R_5	R_4	M_8	M_7	X	M_6	M_5	M_4	M_3	M_2	M_1	M_0	R_3	R_2	R_1	R_0	A_3	A_2	A_1	A_0
Serial*	1	0	B_0	B_1	B_2	B_3	B_4	B_5	B_6	B_7	B_8	B_9	B_{10}	B_{11}	B_{12}	B_{13}	B_{14}	B_{15}	B_{16}	B_{17}	B_{18}	B_{19}
Direct	1	1	R_5	R_4	M_8	M_7	$\overline{0}$	M_6	M_5	M_4	M_3	M_2	M_1	M_0	R_3	R_2	R_1	R_0	A_3	A_2	A_1	A_0

Note: * Data is clocked serially on SCLK rising edge while E_WR is "low" and transferred to frequency register on S_WR rising edge.

MSB (first in) (last in) LSB

Table 7. Enhancement Register Programming

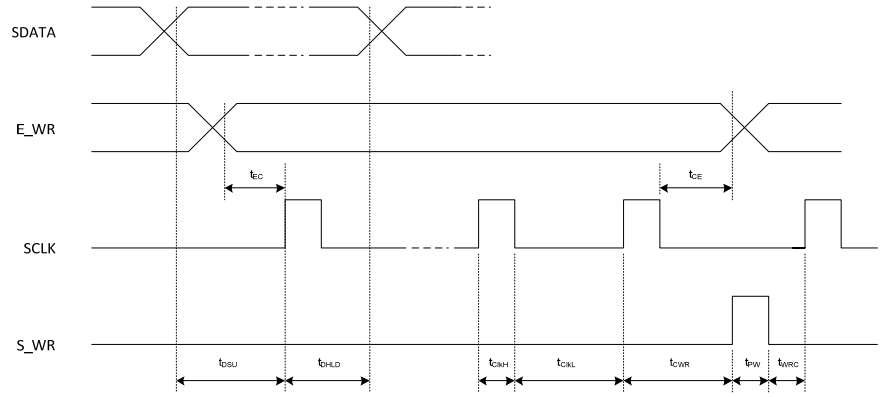
Interface Mode	$\overline{ENH}$	D_{MODE}	Reserved[1]	Reserved[1]	f_p output	Power down	Counter load	MSEL output	f_c output	PB
Serial[2]	0	X	B_0	B_1	B_2	B_3	B_4	B_5	B_6	B_7

Notes: 1. Program to 0.

2. Data is clocked serially on SCLK rising edge while E_WR is "low" and transferred to frequency register on S_WR rising edge.

MSB (first in) (last in) LSB

Figure 9. Serial Interface Mode Timing Diagram



Enhancement Register

The functions of the enhancement register bits are shown below. All bits are active high. Operation is undefined if more than one output is sent to D_{OUT}.

Table 8. Enhancement Register Bit Functionality

Bit Function		Description
Bit 0	Reserved*	
Bit 1	Reserved*	
Bit 2	f_p output	Drives the M counter output onto the D_{OUT} output.
Bit 3	Power down	Power down of all functions except programming interface.
Bit 4	Counter load	Immediate and continuous load of counter programming.
Bit 5	MSEL output	Drives the internal dual modulus prescaler modulus select (MSEL) onto the D_{OUT} output.
Bit 6	f_c output	Drives the R counter output onto the D_{OUT} output.
Bit 7	PB	Allows Fin to bypass the 10/11 prescaler.

Note: * Program to 0.

Phase Detector Outputs

The phase detector is triggered by rising edges from the main counter (f_p) and the reference counter (f_c). It has two outputs, PD_$\overline{U}$, and PD_$\overline{D}$. If the divided VCO leads the divided reference in phase or frequency (f_p leads f_c), PD_$\overline{D}$ pulses "low". If the divided reference leads the divided VCO in phase or frequency (f_c leads f_p), PD_$\overline{U}$ pulses "low". The width of either pulse is directly proportional to phase offset between the two input signals, f_p and f_c. The phase detector gain is 430 mV / radian.

PD_$\overline{U}$ and PD_$\overline{D}$ are designed to drive an active loop filter which controls the VCO tune voltage. PD_$\overline{U}$ pulses result in an increase in VCO frequency and PD_$\overline{D}$ results in a decrease in VCO frequency.

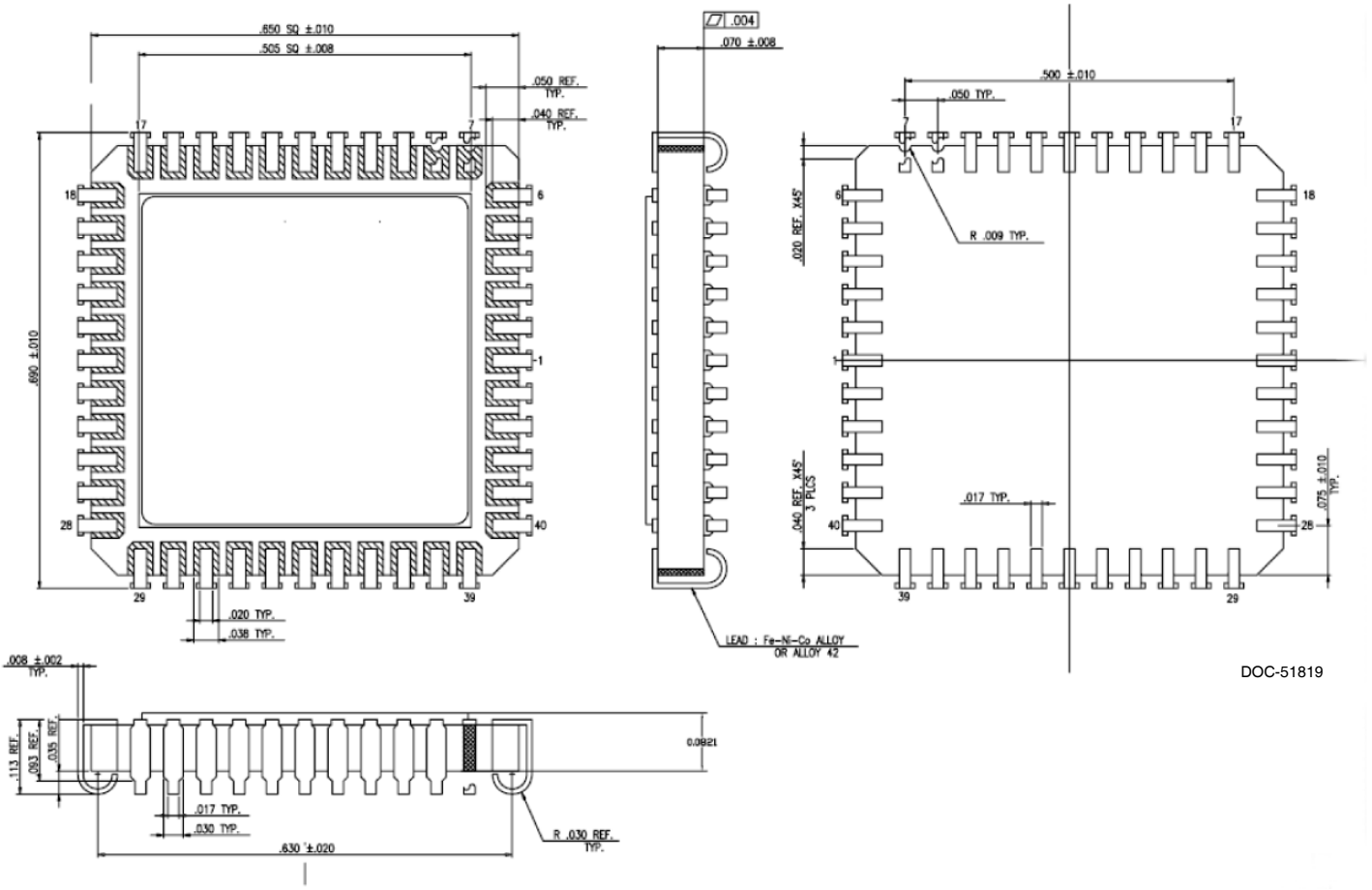
Software tools for designing the active loop filter can be found at Peregrine's web site: www.psemi.com.

Lock Detect Output

A lock detect signal is provided at pin LD, via the pin C_{EXT} (see *Figure 1*). C_{EXT} is the logical "NAND" of PD_$\overline{U}$ and PD_$\overline{D}$ waveforms, driven through a series 2 kΩ resistor. Connecting C_{EXT} to an external shunt capacitor provides integration of this signal.

The C_{EXT} signal is then sent to the LD pin through an internal inverting comparator with an open drain output. Thus LD is an "AND" function of PD_$\overline{U}$ and PD_$\overline{D}$.

Figure 10. Package Drawing
44-lead CQFJ



All dimensions are in inches

Figure 11. Top Marking Specifications

PRT-25129

△ = Pin 1 indicator

97042-XX = Part number (XX will be specified by the PO and/or the assembly instructions)

YYWW = Date Code, last two digits of the year and work week

ZZZZZZZ = Lot Code (up to seven digits)

nnnnnn = Serial number of the part (up to six digits)

Table 9. Ordering Information

Order Code	Description	Package	Shipping Method
97042-01*	Engineering samples	44-lead CQFJ	40 units / tray
97042-11	Flight units	44-lead CQFJ	40 units / tray
97042-00	Evaluation kit		1 / box

Note: * The PE97042-01 devices are ES (engineering sample) prototype units intended for use as initial evaluation units for customers of the PE97042-11 flight units. The PE97042-01 device provides the same functionality and footprint as the PE97042-11 space qualified device, and intended for engineering evaluation only. They are tested at +25 °C only and processed to a non-compliant flow (e.g. No burn-in, non-hermetic, etc). These units are non-hermetic and are not suitable for qualification, production, radiation testing or flight use.

Sales Contact and Information

For sales and contact information please visit www.psemi.com.