

Migrating from PE9763 to PE97632

Introduction

A new generation of low phase noise frequency synthesizers has been released to address the need of the space application requirements for low phase noise. Three new products – PE97022, PE97042 and PE97632, are based on the existing products – PE9702, PE9704 and PE9763 respectively. Careful planning and attention have been made during design to minimize the effort and changes required for the migration from the existing products to the new products. There are trade-offs between design constraint and extent of phase noise improvement. The priority is always given first to produce a solution with the lowest phase noise possible and then with minimum effort for the migration. This application note describes in detail the necessary steps that are needed to migrate from an existing design that uses PE9763 to PE97632 to achieve improved phase noise.

Migrating From PE9763 to PE97632

Going from PE9763 to PE97632 is a direct migration if the charge pump pin (pin 56) is not being used in the existing PE9763 design. If the existing PE9763 design is utilizing “CP” pin, the design needs first be converted to use pin 55 (PD_D) and pin 57 (PD_U) to drive an active loop filter.

Table 1. PE9763 Operational Specifications

Symbol	Parameter/Conditions	Min	Max	Units
V _{DD}	Supply voltage	2.85	3.15	V

Symbol	Parameter	Conditions	Typ	Units
I _{DD}	Operational supply current; Prescaler disabled* Prescaler enabled*	V _{DD} = 2.85 to 3.15 V	10 25	mA mA
Φ _N	Normalized Phase Noise	V _{DD} = 2.85 to 3.15 V	-210	dBc/ Hz

*Charge pump disabled

Summary:

- Details of low phase noise availability in new PLL products
- Migration from PE9763 to PE97632
 - PE97632 pin 55 and pin 57 connection difference if charge pump is used in current PE9763 design
 - Phase Noise greatly improved by raising V_{DD} to 3.3 V on PE97632
- Operational Specification Comparison chart between PE9763 and PE97632
- Phase Noise graph comparison between PE9763 and PE97632

For a PE9763 design that already uses pin 55 (PD_D) and pin 57 (PD_U) for the loop filter, PE97632 can drop-in to the existing PE9763 socket without any design change. If additional phase noise improvement is desired, the supply voltage (V_{DD}) can be raised from 3.0 V to 3.3 V.

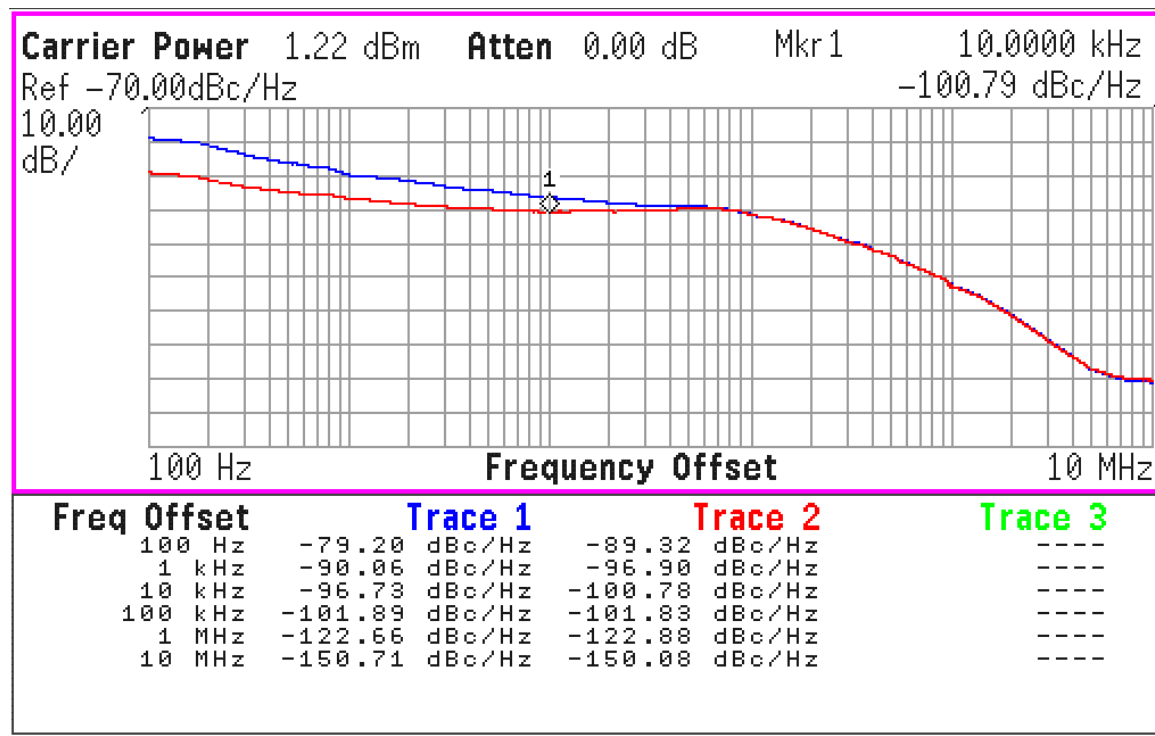
The typical operation I_{DD} for PE97632 is about 15 mA higher than for PE9763. The existing design needs to be capable of sourcing the extra current without lowering the voltage level on V_{DD} pins of PE97632. Please see *Tables 1&2* for a comparison of operational specifications.

Table 2. PE97632 Operational Specifications

Symbol	Parameter/Conditions	Min	Max	Units
V _{DD}	Supply voltage	2.85	3.45	V

Symbol	Parameter	Conditions	Typ	Units
I _{DD}	Operational supply current; Prescaler disabled Prescaler enabled	V _{DD} = 3.3 V	15 40	mA mA
Φ _N	Normalized Phase Noise	V _{DD} = 3.3 V	-216	dBc/ Hz

Figure 1. Typical Phase Noise for PE9763 (Trace 1) and PE97632 (Trace 2), Fvco = 1.9204 GHz, Fcomp = 20 MHz, Loop Bandwidth =50 kHz



Conclusion

This application note has described the steps necessary to convert any existing design that uses PE9763 to the newer, lower phase noise PE97632. For help or more information about this report, please contact Peregrine Applications Support at help@psemi.com.

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Sales Offices

The Americas

Peregrine Semiconductor Corporation

9380 Carroll Park Drive
San Diego, CA 92121
Tel: 858-731-9400
Fax: 858-731-9499

Europe

Peregrine Semiconductor Europe

Bâtiment Maine
13-15 rue des Quatre Vents
F-92380 Garches, France
Tel: +33-1-4741-9173
Fax : +33-1-4741-9173

Space and Defense Products

Americas:

Tel: 858-731-9453

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180 Rue Jean de Guiramand
13852 Aix-En-Provence Cedex 3, France
Tel: +33-4-4239-3361
Fax: +33-4-4239-7227

Peregrine Semiconductor, Asia Pacific (APAC)

Shanghai, 200040, P.R. China
Tel: +86-21-5836-8276
Fax: +86-21-5836-7652

Peregrine Semiconductor, Korea

#B-2607, Kolon Tripolis, 210
Geumgok-dong, Bundang-gu, Seongnam-si
Gyeonggi-do, 463-943 South Korea
Tel: +82-31-728-3939
Fax: +82-31-728-3940

Peregrine Semiconductor K.K., Japan

Teikoku Hotel Tower 10B-6
1-1-1 Uchisaiwai-cho, Chiyoda-ku
Tokyo 100-0011 Japan
Tel: +81-3-3502-5211
Fax: +81-3-3502-5213

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