

## PE94302

**50Ω RF Digital Step Attenuator  
Radiation Tolerant for Space  
Applications, 6-bit, 31.5 dB, 4.0 GHz**

### Product Description

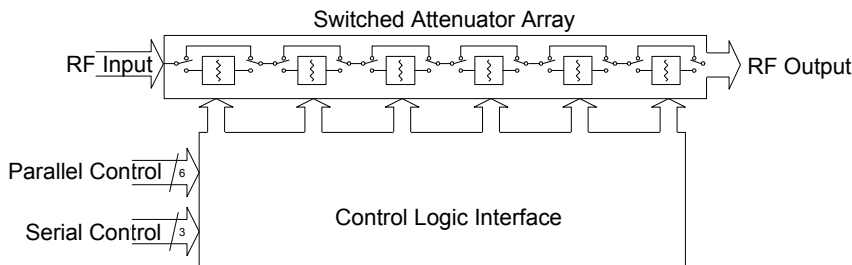
Peregrine's PE94302 is a high linearity, 6-bit UltraCMOS® RF digital step attenuator (DSA). This 50Ω RF DSA covers a 31.5 dB attenuation range in 0.5 dB steps. It provides both parallel and serial CMOS control interface. The PE94302 maintains high attenuation accuracy over frequency and temperature and exhibits very low insertion loss and power consumption.

The PE94302 is optimized for commercial space applications. Single event latch-up (SEL) is physically impossible and single event upset (SEU) is better than 10/9 errors per bit/day. Fabricated in Peregrine's UltraCMOS technology, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate, the PE94302 offers excellent RF performance and intrinsic radiation tolerance.

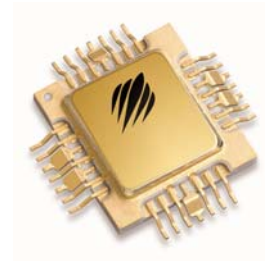
### Features

- Attenuation: 0.5 dB steps to 31.5 dB
- Flexible parallel and serial programming interfaces
- 100 kRad (Si) total dose
- Positive CMOS control logic
- High attenuation accuracy and linearity over temperature and frequency
- Low power: 100 μA @ 3.0V
- 50Ω impedance

**Figure 1. Functional Diagram**



**Figure 2. Package Type  
28-lead CQFP**



**Table 1. Electrical Specifications @ -40 °C ≤ Temp ≤ +85 °C, 2.7V ≤ V<sub>DD</sub> ≤ 3.30V**

Parameter	Test Conditions	Frequency	Min	Typ	Max	Unit
Operation frequency		250 kHz–4000 MHz				MHz
Insertion loss		250 kHz–2.2 GHz		1.5	2.75	dB
Attenuation accuracy	0.5–8.0 dB atten	250 kHz–1.0 GHz	-(0.55 + 3.7% of atten setting)		+(0.55 + 3.7% of atten setting)	dB
	8.5–31.5 dB atten				+ 0.9	
	0.5–4.0 dB atten	1.0–2.2 GHz			+(0.70 + 3.0% of atten setting)	
	4.5–31.5 dB atten				+ 0.9	
	0.5–23.0 dB atten				-(0.7 + 3.0% of atten setting)	
	23.5–31.5 dB atten		-(0.6 + 9.0% of atten setting)			
1dB compression		1 MHz–2.2 GHz		33		dBm
Input IP3	Two-tone inputs			52		dBm
Return loss		250 kHz–2.2 GHz		15		dB
Switching speed	Min to max atten state				1	μs

Notes: 1. Device linearity will begin to degrade below 1 MHz.  
2. Electrical specifications guaranteed at maximum input power = +12 dBm.  
3. Specs are guaranteed to 2.2 GHz, characterized to 4.0 GHz.

Figure 3. Pin Configuration (Top View)

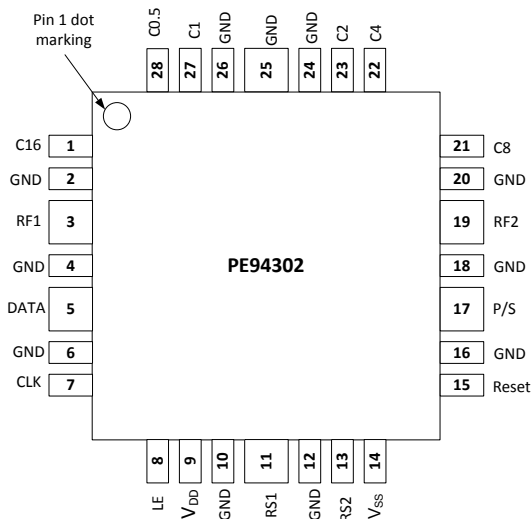


Table 2. Pin Descriptions

Pin #	Pin Name	Description
1	C16	Attenuation control bit, 16 dB.
2	GND	Ground.
3	RF1	RF port (Note 1).
4	GND	Ground.
5	DATA	Serial interface data input.
6	GND	Ground.
7	CLK	Serial interface clock input.
8	LE	Latch enable input (Note 2).
9	V <sub>DD</sub>	Power supply pin.
10	GND	Ground.
11	RS1	Redundant signal (Note 3).
12	GND	Ground.
13	RS2	Redundant signal (Note 3).
14	V <sub>SS</sub>	Negative supply voltage (Note 4).
15	Reset	Reset (Note 5).
16	GND	Ground.
17	P/S	Parallel/serial mode select.
18	GND	Ground.
19	RF2	RF port (Note 1).
20	GND	Ground.
21	C8	Attenuation control bit, 8 dB.
22	C4	Attenuation control bit, 4 dB.
23	C2	Attenuation control bit, 2 dB.
24	GND	Ground.
25	GND	Ground.
26	GND	Ground.
27	C1	Attenuation control bit, 1 dB.
28	C0.5	Attenuation control bit, 0.5 dB.
Pad	GND	Exposed pad: Ground for proper operation.

- Notes:
- Both RF ports must be held at 0 VDC or DC blocked with an external series capacitor.
  - Latch enable (LE) has an internal 100 kΩ resistor to V<sub>DD</sub>.
  - Must be tied to V<sub>DD</sub> or GND under normal operation.
  - Must be tied to external supply with V<sub>SS</sub> = -V<sub>DD</sub>.
  - Must be tied to GND under normal operation.

Table 3. Absolute Maximum Ratings

Symbol	Parameter/Conditions	Min	Max	Unit
V <sub>DD</sub>	Power supply voltage	-0.3	4.0	V
V <sub>SS</sub>	Negative power supply voltage (-V <sub>DD</sub> )	-4.0	0.3	V
V <sub>I</sub>	Voltage on any DC input	-0.3	V <sub>DD</sub> + 0.3	V
T <sub>ST</sub>	Storage temperature range	-65	+150	°C
P <sub>IN</sub>	Input power (50Ω) 5 MHz-<100 MHz 100 MHz		22 24	 dBm dBm
V <sub>ESD</sub>	ESD voltage (human body model)		500	V

Exceeding absolute maximum ratings may cause permanent damage. Operation should be restricted to the limits in the Operating Ranges table. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

Table 4. Operating Ranges

Parameter	Min	Typ	Max	Unit
V <sub>DD</sub> power supply voltage	2.7	3.0	3.3	V
V <sub>SS</sub> power supply voltage	-3.3	-3.0	-2.7	V
I <sub>DD</sub> power supply current			250	μA
I <sub>SS</sub> power supply current	-500			μA
RF input power (50Ω) ≥5 MHz			17	dBm
T <sub>OP</sub> operating temperature range	-40		+85	°C
Digital input high	0.7 × V <sub>DD</sub>			V
Digital input low			0.3 × V <sub>DD</sub>	V
Digital input leakage			1	μA

**Electrostatic Discharge (ESD) Precautions**

When handling this UltraCMOS device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified.

**Latch-Up Immunity**

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

**ELDRS**

The UltraCMOS process does not exhibit enhanced low-dose-rate sensitivity (ELDRS) since bipolar minority carrier elements are not used.

## Programming Options

### Parallel/Serial Selection

Either a Parallel or Serial interface can be used to control the PE94302. The P/S bit provides this selection, with P/S = LOW selecting the Parallel interface and P/S = HIGH selecting the Serial interface.

### Parallel Mode Interface

The Parallel interface consists of six CMOS-compatible control lines that select the desired attenuation state, as shown in *Table 5*.

The Parallel interface timing requirements are defined by *Figure 5* (Parallel Interface Timing Diagram), *Table 8* (Parallel Interface AC Characteristics) and switching speed (*Table 1*).

For Latched Parallel programming the latch enable (LE) should be held LOW while changing attenuation state control values, then pulse LE HIGH to LOW (per *Figure 5*) to latch new attenuation state into device.

For Direct Parallel programming, the LE should be either pulled high or floated (see *Table 2, Note 2*). Changing attenuation state control values will change device state to new attenuation. Direct mode is ideal for manual control of the device (using hardware, switches or jumpers).

### Serial Interface

The Serial interface is a 6-bit serial-in, parallel-out shift register buffered by a transparent latch. It is controlled by three CMOS-compatible signals: DATA, CLK and LE. The DATA and CLK inputs allow data to be serially entered into the shift register, a process that is independent of the state of the LE input.

The LE input controls the latch. When LE is HIGH, the latch is transparent and the contents of the serial shift register control the attenuator. When LE is brought LOW, data in the shift register is latched.

The shift register should be loaded while LE is held LOW to prevent the attenuator value from changing as data is entered. The LE input should then be toggled HIGH and brought LOW again, latching the new data. The timing for this operation is defined by *Figure 4* (Serial Interface Timing Diagram) and *Table 7* (Serial Interface AC Characteristics).

**Table 5. Truth Table\***

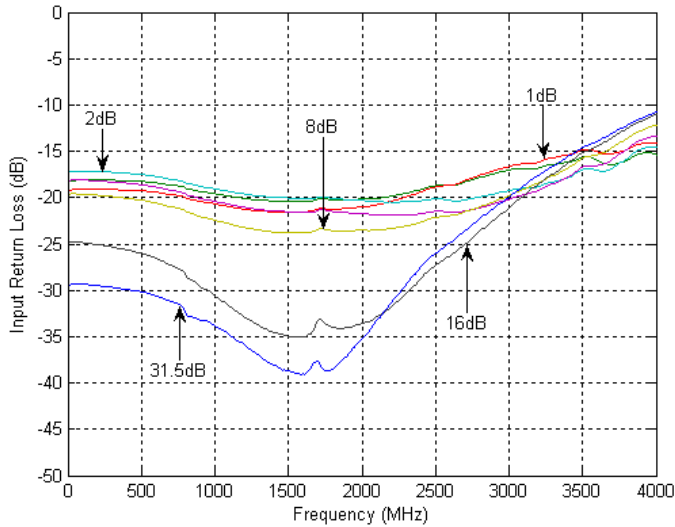
P/S	C16	C8	C4	C2	C1	C0.5	Attenuation State
0	0	0	0	0	0	0	Reference loss
0	0	0	0	0	0	1	0.5 dB
0	0	0	0	0	1	0	1 dB
0	0	0	0	1	0	0	2 dB
0	0	0	1	0	0	0	4 dB
0	0	1	0	0	0	0	8 dB
0	1	0	0	0	0	0	16 dB
0	1	1	1	1	1	1	31.5 dB

Note: \* Not all 64 possible combinations of C0.5–C16 are shown in table.

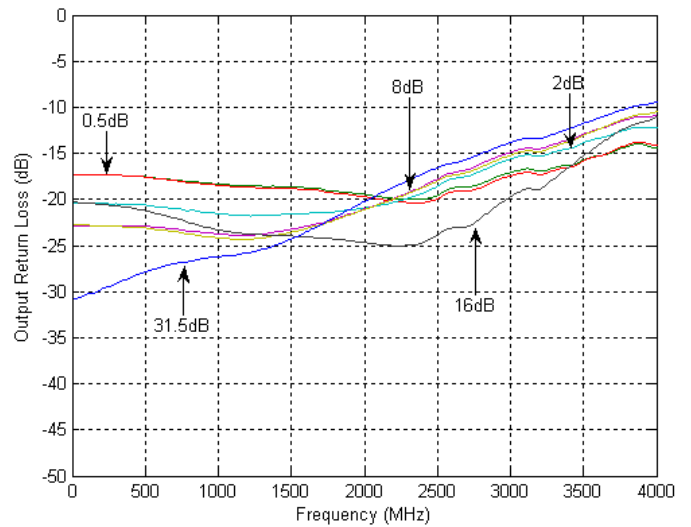


Typical Performance Data @ +25 °C,  $V_{DD} = -V_{SS} = 3.0V$ , unless otherwise specified

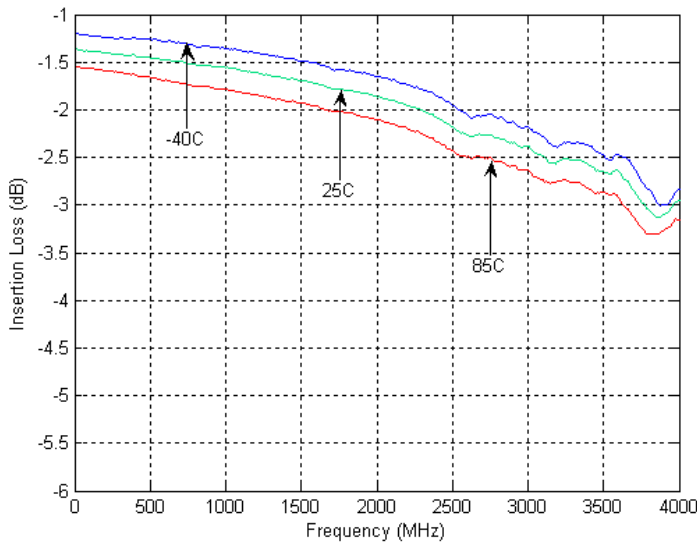
**Figure 6. Input Return Loss vs Frequency**



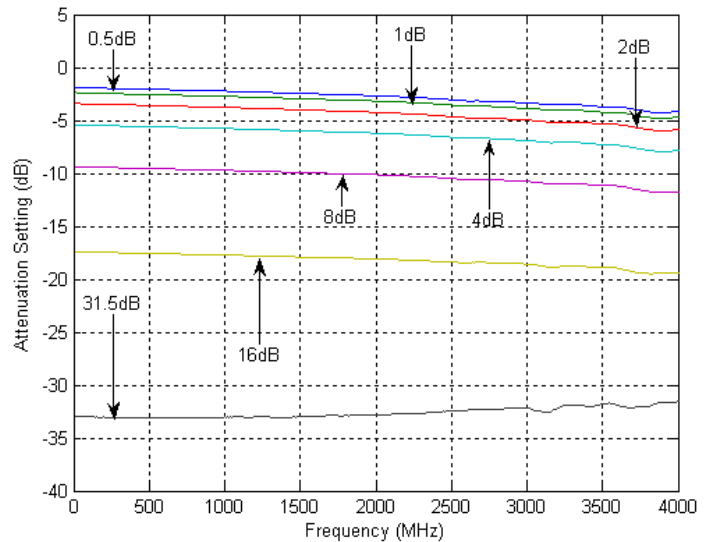
**Figure 7. Output Return Loss vs Frequency**



**Figure 8. Insertion Loss**



**Figure 9. Attenuation Setting vs Frequency**



Typical Performance Data @ +25 °C,  $V_{DD} = -V_{SS} = 3.0V$ , unless otherwise specified (cont.)

Figure 10. Attenuation Error vs Frequency

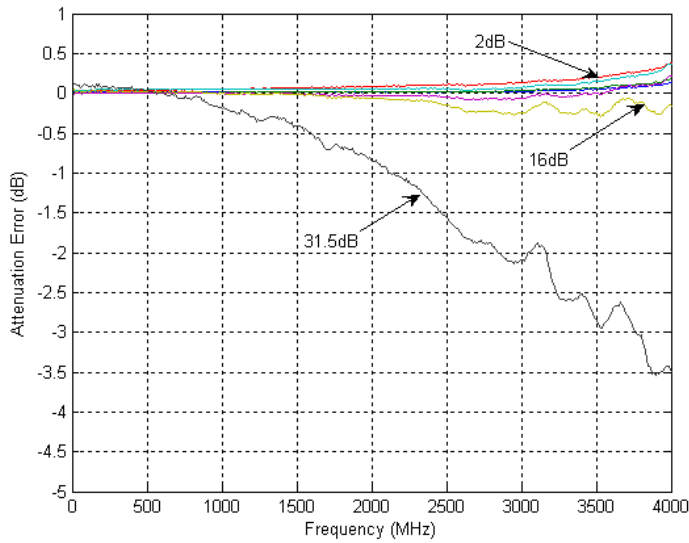


Figure 11. Attenuation Error vs Setting

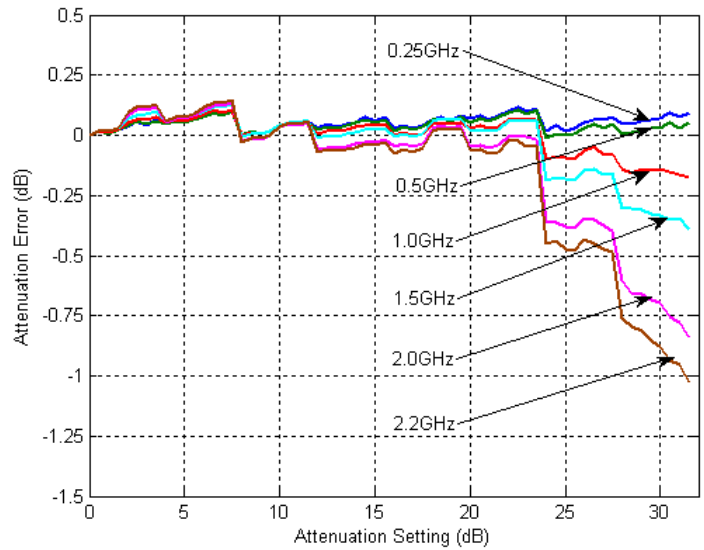


Figure 12. IIP3 vs Frequency

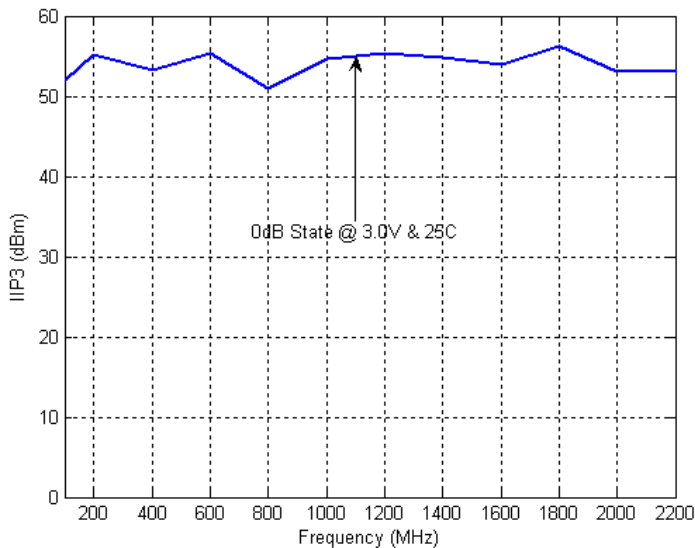
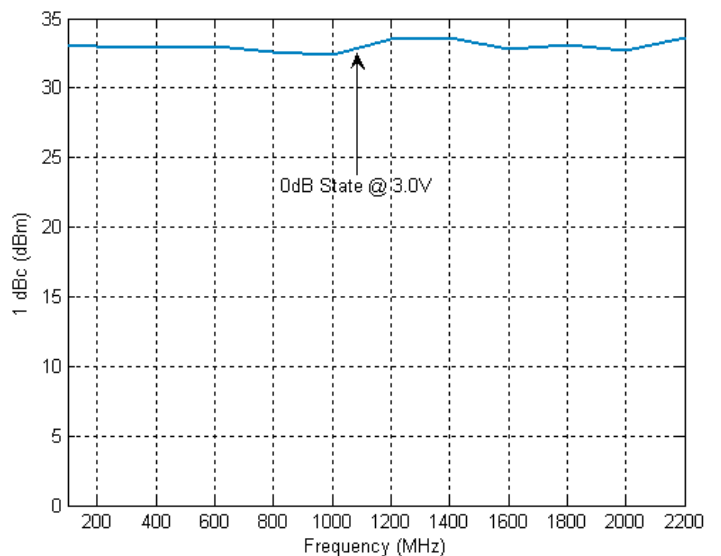


Figure 13. 1dB Compression vs Frequency



**Figure 14. Package Drawing (dimensions in millimeters)**  
28-lead CQFP

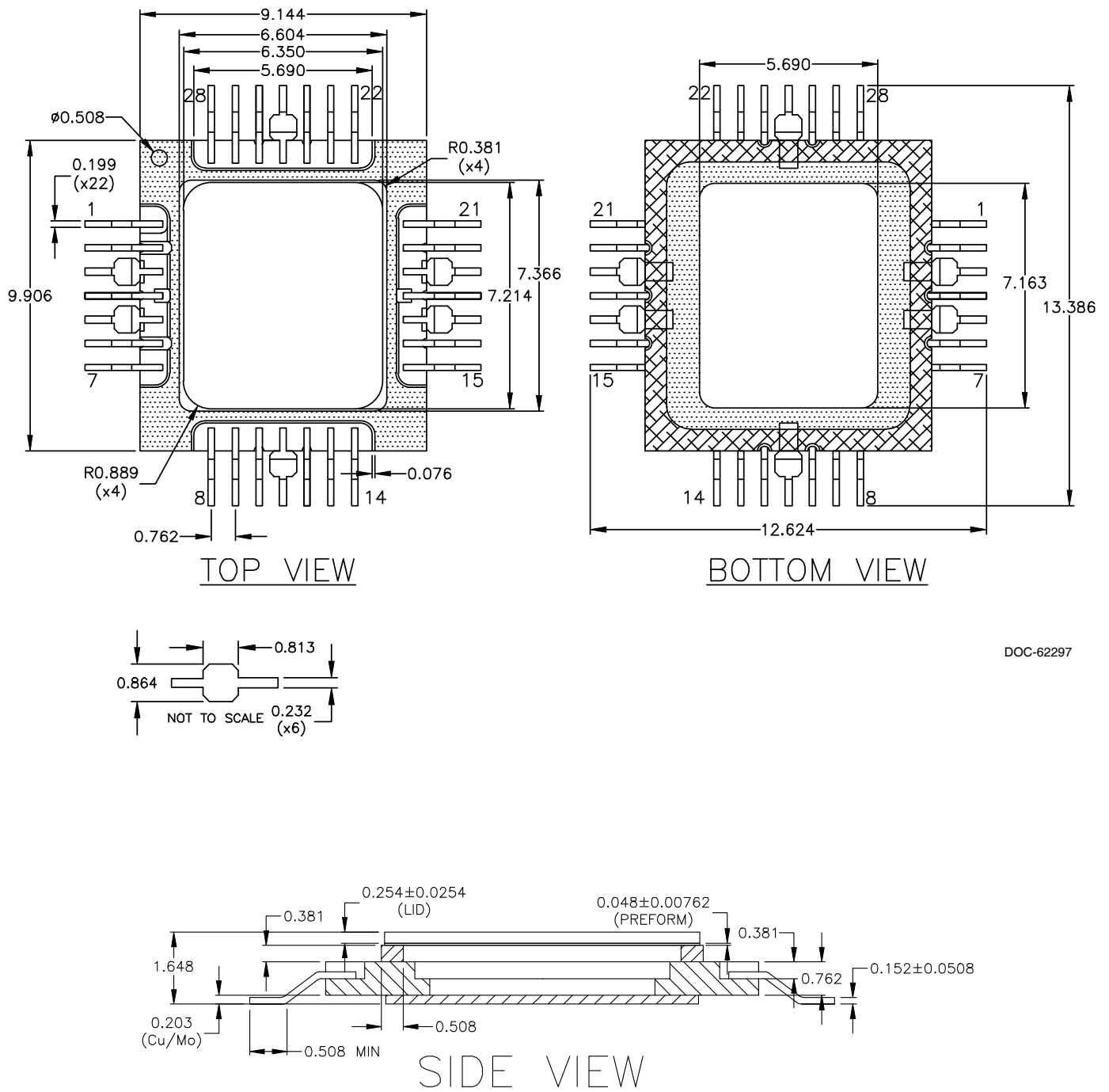
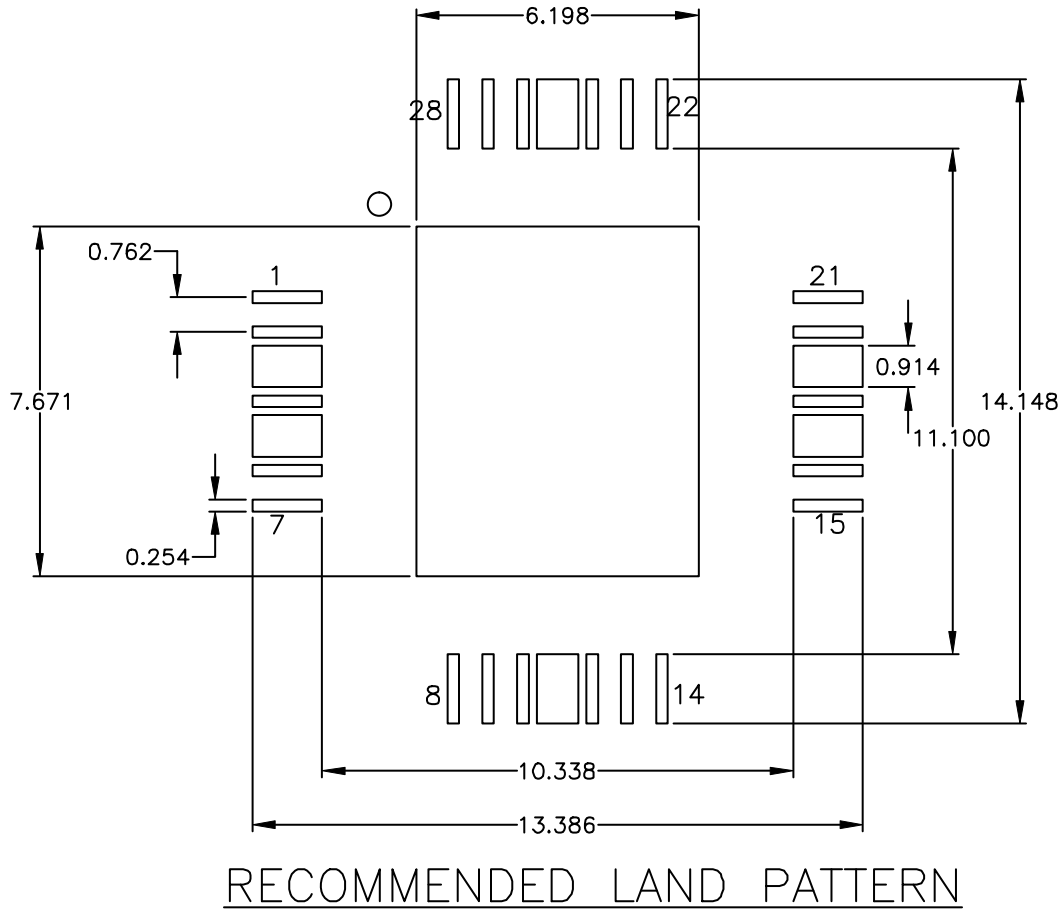
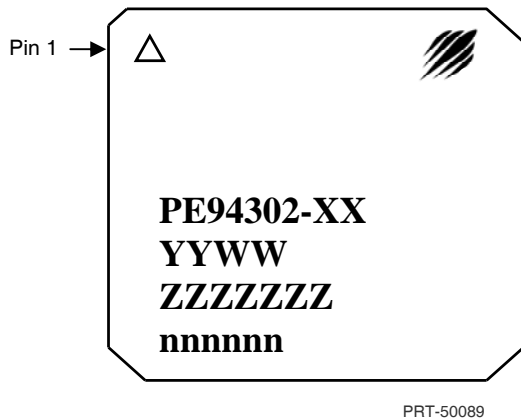


Figure 14. Package Drawing (dimensions in millimeters) (cont.)





**Figure 15. Top Marking Specifications**



△ = Pin 1 indicator  
 94302-XX = Part number (XX will be specified by the PO and/or the assembly instructions)  
 YYWW = Date Code, last two digits of the year and work week  
 ZZZZZZZ = Lot Code (up to seven digits)  
 nnnnnn = Serial number of the part (up to six digits)

**Table 9. Ordering Information**

Order Code	Description	Package	Shipping Method
94302-01*	Engineering samples	28-lead CQFP	24 units / JEDEC tray
94302-11	Production units	28-lead CQFP	24 units / JEDEC tray
94302-00	Evaluation kit	Evaluation board	1 / box

Note: \* The PE94302-01 devices are engineering sample (ES) prototype units intended for use as initial evaluation units for customers of the PE94302-11 flight units. The PE94302-01 device provides the same functionality and footprint as the PE94302-11 space qualified device, and intended for engineering evaluation only. They are tested at +25 °C only and processed to a non-compliant flow (e.g. no burn-in, non-hermetic, etc). These units are non-hermetic and are not suitable for qualification, production, radiation testing or flight use.

## Sales Contact and Information

For sales and contact information please visit [www.psemi.com](http://www.psemi.com).

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