AN33: Application Note

5 bit & 6 bit RF Digital Step Attenuator Compatibility

Features

- 5 & 6 bit models
- Common flexible parallel and serial programming interfaces
- Unique power-up state selection
- Positive CMOS control logic
- High attenuation accuracy and Linearity over temperature and frequency
- Very low power consumption
- Single-supply operation
- 50Ω impedance
- Packaged in a 20 Lead 4x4mm QFN

Summary

Peregrine Semiconductor Application Note AN33 demonstrates socket and software compatibility of the 5 bit and 6 bit digital step attenuators products. This family offers high performance attenuation accuracy and linearity using only a single 3 volt supply.

1. Introduction

Typical digital step attenuators (DSA) in GaAs technology require either a single or bipolar 5 Volt supply, and either a +5 or -5 Volt control interface. Peregrine DSA's require only one +3 volt supply to deliver extremely high linearity and high accuracy. Other features include default power-up attenuation state, user selectable serial , parallel, and direct mode programming,, 3 volt CMOS interface, 50 and 75 ohm variations, and very low power consumption. This document describes forward / backward compatibility of the 5 bit and 6 bit models.

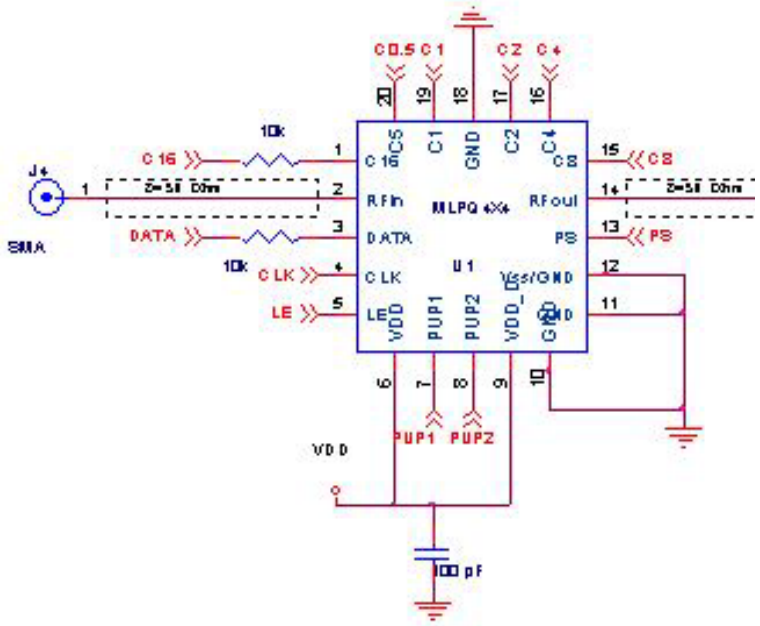


Figure 1. Typical 6 bit evaluation schematic

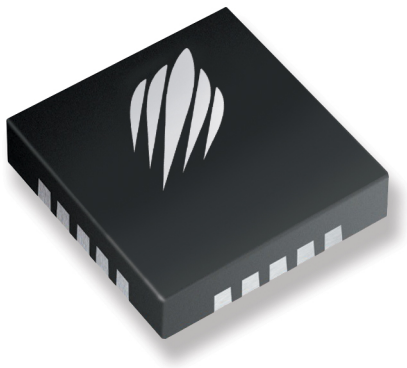
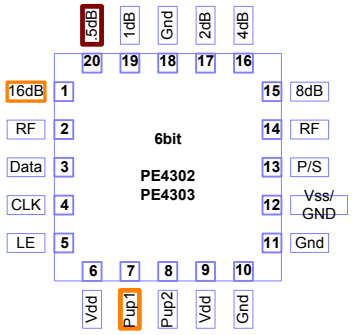


Figure 2. 20 pin / 4x4 QFN

P/S	C16	C8	C4	C2	C1	C0.5	Attenuation State
0	0	0	0	0	0	0	Reference Loss
0	0	0	0	0	0	1	0.5 dB
0	0	0	0	0	1	0	1 dB
0	0	0	0	1	0	0	2 dB
0	0	0	1	0	0	0	4 dB
0	0	1	0	0	0	0	8 dB
0	1	0	0	0	0	0	16 dB
0	1	1	1	1	1	1	31.5 dB

Note: Not all 64 possible combinations of C0.5-C16 are shown in



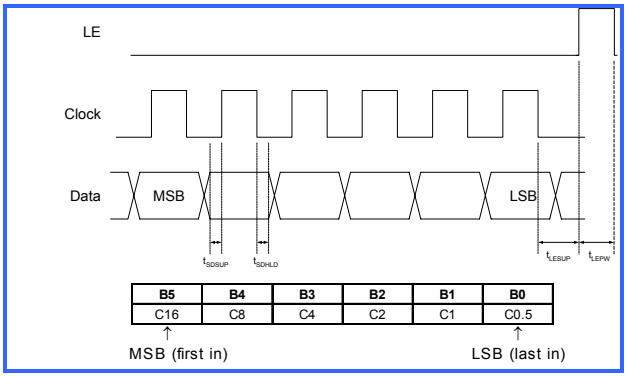
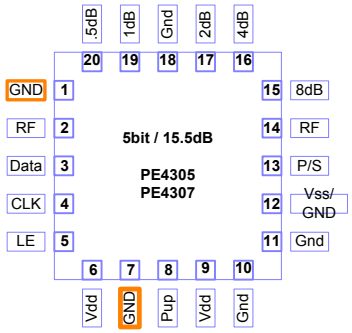


Figure 3. 6-bit 31.5 dB Serial Timing

A 6 bit attenuator can be installed in a 5 bit design. The highlighted pins are different for 5 bit users as explained below.

P/S	Pin 1	C8	C4	C2	C1	C0.5	Attenuation State
0	0	0	0	0	0	0	Reference Loss
0	0	0	0	0	0	1	0.5 dB
0	0	0	0	0	1	0	1 dB
0	0	0	0	1	0	0	2 dB
0	0	0	1	0	0	0	4 dB
0	0	1	0	0	0	0	8 dB
0	0	1	1	1	1	1	15.5 dB

Note: Not all possible combinations of C0.5-C8 are shown



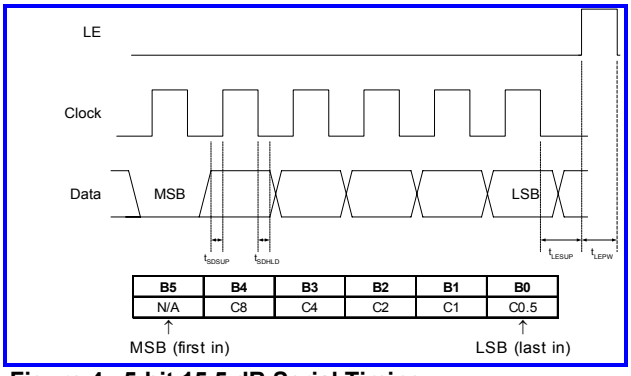
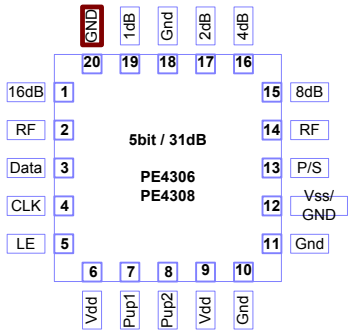


Figure 4. 5-bit 15.5 dB Serial Timing

P/S	C16	C8	C4	C2	C1	Pin 20	Attenuation State
0	0	0	0	0	0	0	Reference Loss
0	0	0	0	0	1	0	1 dB
0	0	0	0	1	0	0	2 dB
0	0	0	1	0	0	0	4 dB
0	0	1	0	0	0	0	8 dB
0	1	0	0	0	0	0	16 dB
0	1	1	1	1	1	0	31.5 dB

Note: Not all possible combinations of C1-C16 are shown



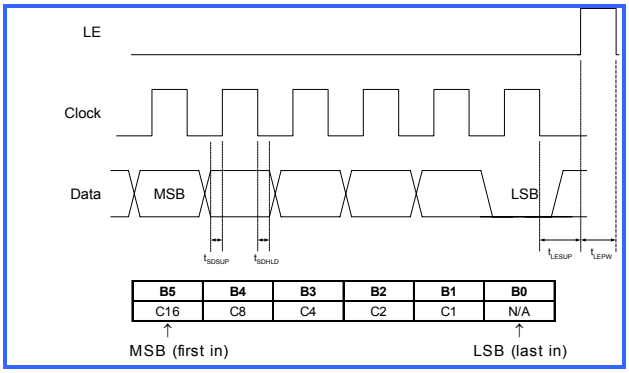


Figure 5. 5 bit 31 dB Serial Timing

2. Generic Hardware Design Consideration

The 5 bit and 6 bit parts share a common pinout. The only differences between the 5 and 6 bit parts are the two specific pins associated with the Direct Mode 0.5dB and 16 dB steps.

Direct Mode
In Direct Mode the pin assigned to an unavailable step becomes a Don't Care.

5 Bit, 0.5 dB LSB Pin 1, C16 on the 6 bit device, becomes inactive or Don't Care.
5 Bit, 1 dB LSB Pin 20, C0.5 on the 6 bit device, becomes inactive or Don't Care.

***For the 6-bit part to emulate the 5-bit part, the "Don't Care" pin should be held Lo.
***For designs that may upgrade from 5-bit to 6-bit, the "Don't Care" pins can be routed to zero ohm resistor initially hooked to ground, with provision to connect to controller.

Serial Mode
The 5 and 6 bit parts use a common 6 bit serial word format. The first bit, the MSB, corresponds to the 16 dB step and the LSB corresponds to the 0.5 dB step.

5 Bit, 0.5 dB LSB Device operates on either a 5 or 6 bit word. Optional 6th MSB is ignored and the state is set by the last 5 bits sent. If the designer anticipates a possible upgrade to a 6 bit, 31.5 dB part, then a 6 bit word preserves full software compatibility.

5 Bit, 1 dB LSB Device requires 6 bit word. The 0.5 dB bit is received but ignored.

1. The 5-bit *31* dB part in **serial** mode uses a similar clock/data string. Use Figure 4, noting 6 clocks are required, and five data bits position as shown.

2. The 5-bit *31* dB part in **parallel** mode uses the table in Figure 4. Note data bit pin C0.5 is unused.

3. The 5-bit *15.5* dB part in **serial** mode uses a similar clock/data string. Use Figure 5, noting 6 clocks are required, and five data bits position as shown.

4. The 5-bit *15.5* dB part in **parallel** mode uses the table in Figure 5. Note data bit pin C16 is unused.

***** NOTE:** Controlling the 6th bit position in a 5-bit attenuator will put the part into an unknown state.

Sales Offices

United States

Peregrine Semiconductor Corp.
6175 Nancy Ridge Drive
San Diego, CA 92121
Tel 1-858-455-0660
Fax 1-858-455-0770

Japan

Peregrine Semiconductor K.K.
The Imperial Tower, 15th floor
1-1-1 Uchisaiawaicho, Chiyoda-ku
Tokyo 100-0011 Japan
Tel: 03-3507-5755
Fax: 03-3507-5601

Europe

Peregrine Semiconductor Europe
Bâtiment Maine
15, Rue des Quatre Vents
92380 Garches, France
Tel 33-1-4741-9173
Fax 33-1-4741-9173

For a list of representatives in your area, please refer to our Web site at: ***http://www.peregrine-semi.com***

Data Sheet Identification

Advance Information

The product is in a formative or design stage. The data sheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification

The data sheet contains preliminary data. Additional data may be added at a later date. Peregrine reserves the right to change specifications at any time without notice in order to supply the best possible product.

Product Specification

The data sheet contains final data. In the event Peregrine decides to change the specifications, Peregrine will notify customers of the intended changes by issuing a PCN (Product Change Notice).