Document Number: MC1320xRFCUG
Rev. 1.2, 03/2010

MC1320x RF Daughter Card

User's Guide

1 Introduction

The MC1320x RF Daughter Card (1320xRFD-A00) is used in conjunction with a microcontroller development board for RFIC evaluation, code development, and system evaluation. The RF Daughter Card interfaces directly to the M68EVB908GB60, RG60 and QG60 HCS08 family Microcontroller Development Boards and to the M52235 EVB Microcontroller Development Board, but it can be adapted to other boards that offer access to the MCU input/output ports.

The RF Daughter Card is configured with all the off-chip circuitry required for functional performance of the MC1320x RF data modem except the MCU. The MCU interface required by the RFIC is pinned out at the edge of the card using standard header pins. The RF interface is accomplished through an onboard PCB antenna. Also, there is an SMT jumper that can be relocated, which will redirect the RF interface to an on-board 50 ohm connector. The SMA connector can be used with standard coax cables for testing purposes. Figure 1-1 shows the RF Daughter Card.

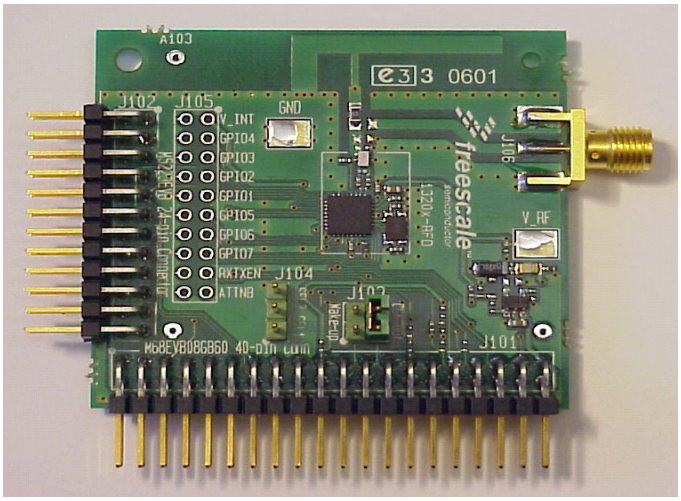

Figure 1-1. MC1320x RF Daughter Card

Figure 1-2 shows the RF Daughter Card installed in a GB60 development board.

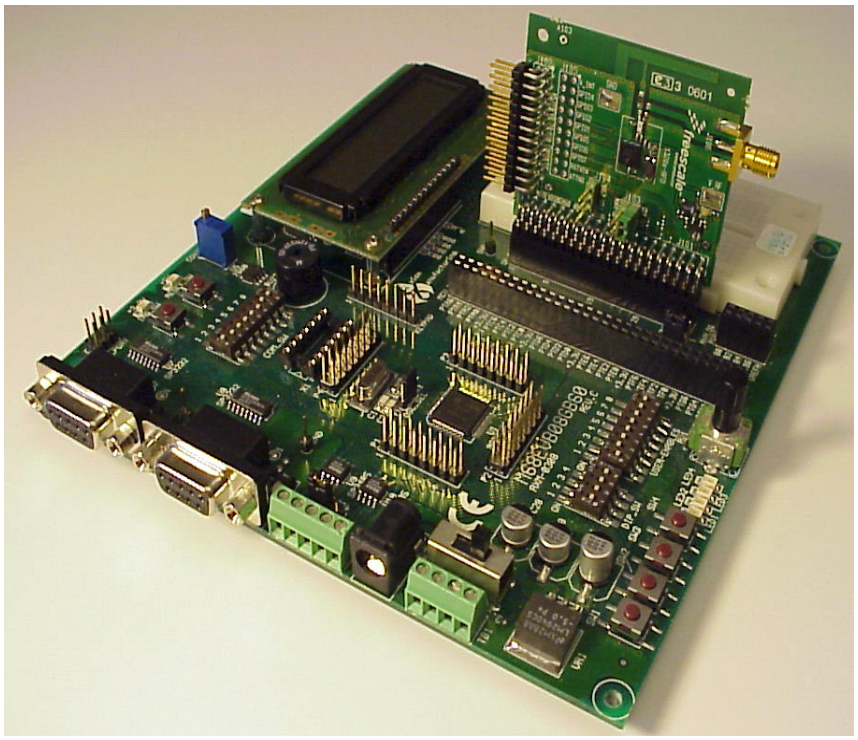

Figure 1-2. MC1320xRF Daughter Card In GB60 Development Board

Figure 1-3 shows the M52235 EVB development board.

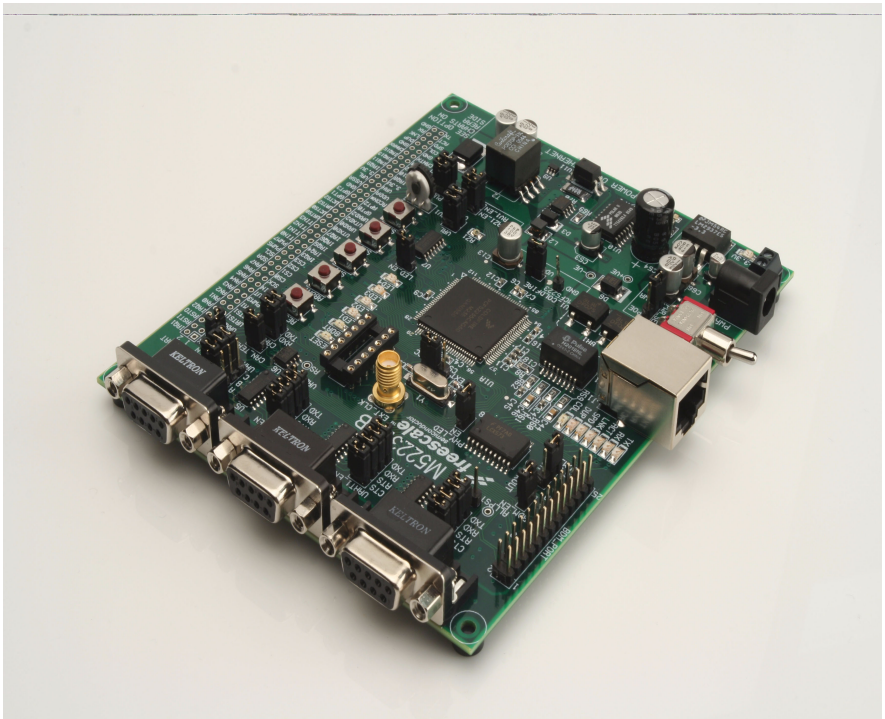

Figure 1-3. M52235 EVB Development Board

2 Safety Information

Any modifications to this product may violate the rules of the Federal Communications Commission and make operation of the product unlawful.

47 C.F.R. Sec. 15.21

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

47 C.F.R. Sec.15.105(b)

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. The antenna(s) used for this equipment must be installed to provide a separation distance of at least 8 inches (20cm) from all persons.

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

- This device may not cause harmful interference.
- This device must accept any interference received, including interference that may cause undesired operation.

3 Revision History

The following table summarizes revisions to this document since the previous release (Rev 1.1).

Revision History

Location	Revision
Section 6	Updated document cross reference.

4 MC1320x MCU Interface

Figure 4-1 shows the typical connections between the MC1320x transceiver and a microcontroller unit (MCU). See the *MC13202/203 Reference Manual*, document MC13202RM, for interface considerations. Details about the interconnects for both the GB60 and M52235 Development boards are described in Section 5.1, “Development Board Interconnects”.

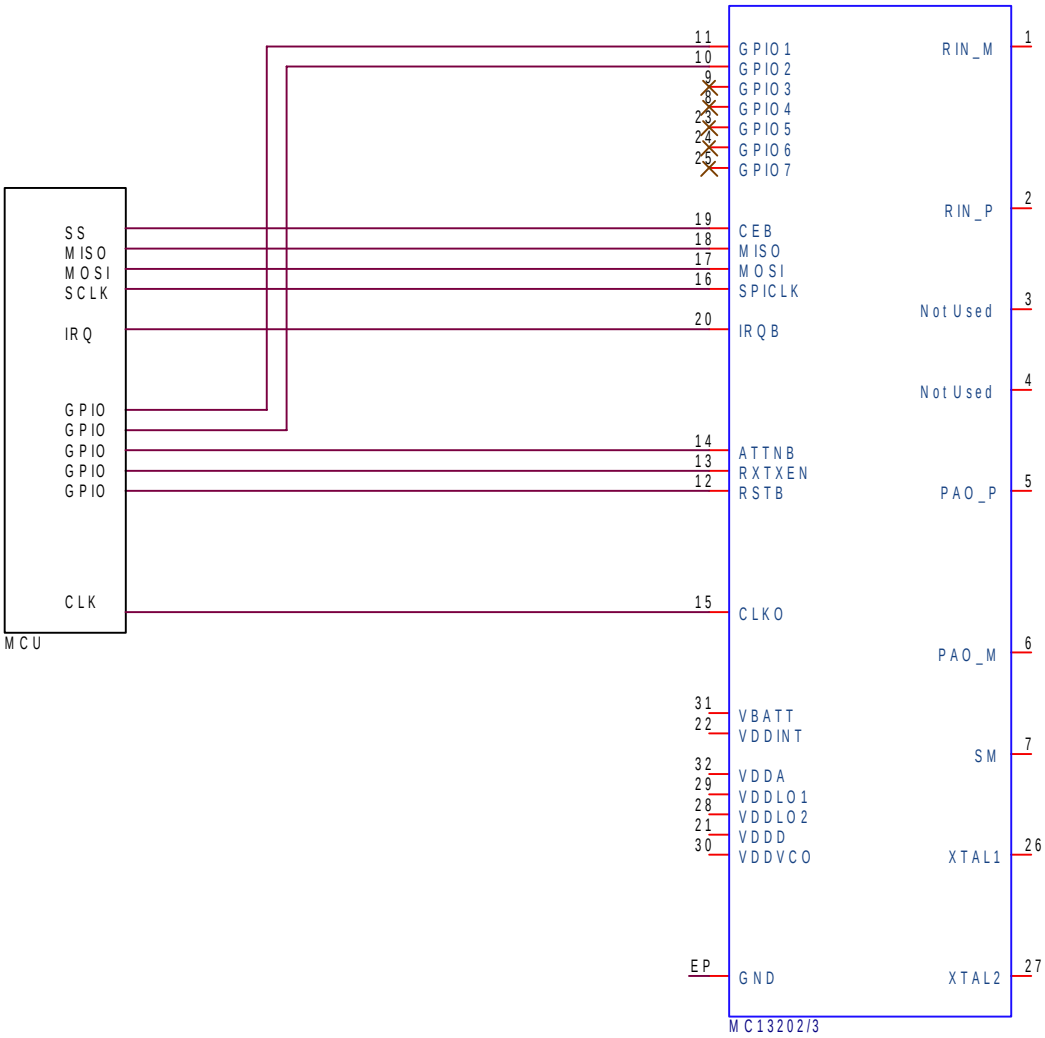

Figure 4-1. MCU Interface Pinout

5 Daughter Card Description

As shown in Figure 5-1 and Figure 8-1, connector J101 is the main interface to the GB60 Development Board. The interface connections described in Section 5.1, “Development Board Interconnects”, fall under the following three broad categories:

1. Serial Peripheral Interface (SPI)
2. Control
3. Power

Figure 1-2 shows how the RF Daughter Card is mounted on the GB60 Development Board.

NOTE

Ensure that zero ohm resistor R104 is in place on the MC1320x Daughter Card. As of this release, previous versions of the MC1320x Daughter Card may not have R104 inserted.

NOTE

J101 Pin 1 of the MC1320x must to be connected to GB_PORT Pin 1 of the GB60 Development Board.

As shown in Figure 5-1 and Figure 8-1, connector J102 is the main interface to the M52235 Development Board. Figure 1-3 shows how the RF Daughter Card is mounted on the M52235 Development Board.

NOTE

J102 Pin 1 of the MC1320x must be connected to MCU_PORT Pin 1 on the M52235 Development Board.

Figure 5-1 shows the top side of the RF Daughter Card PCB with component placement.

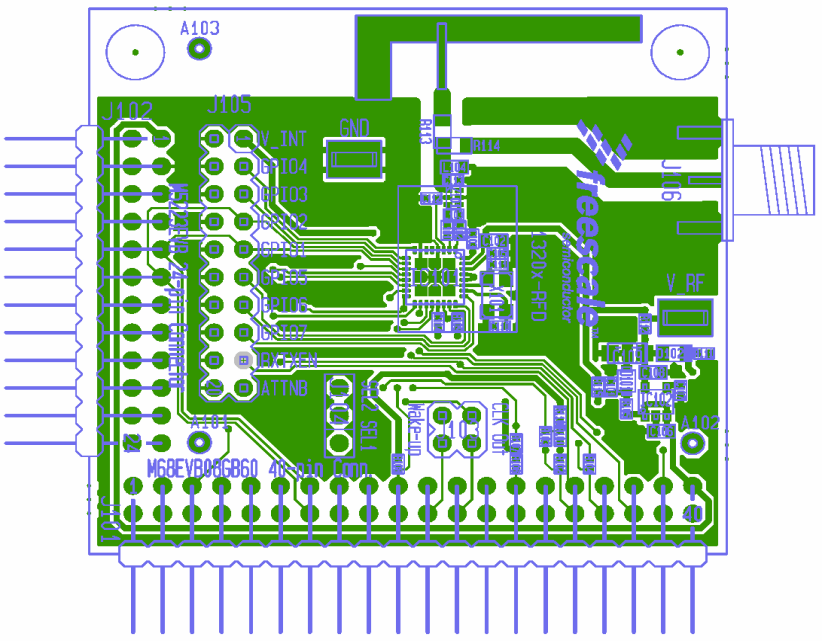

Figure 5-1. MC1320x Daughter Card (Top View)

Figure 5-2 shows the shows the bottom side of the RF Daughter Card PCB.

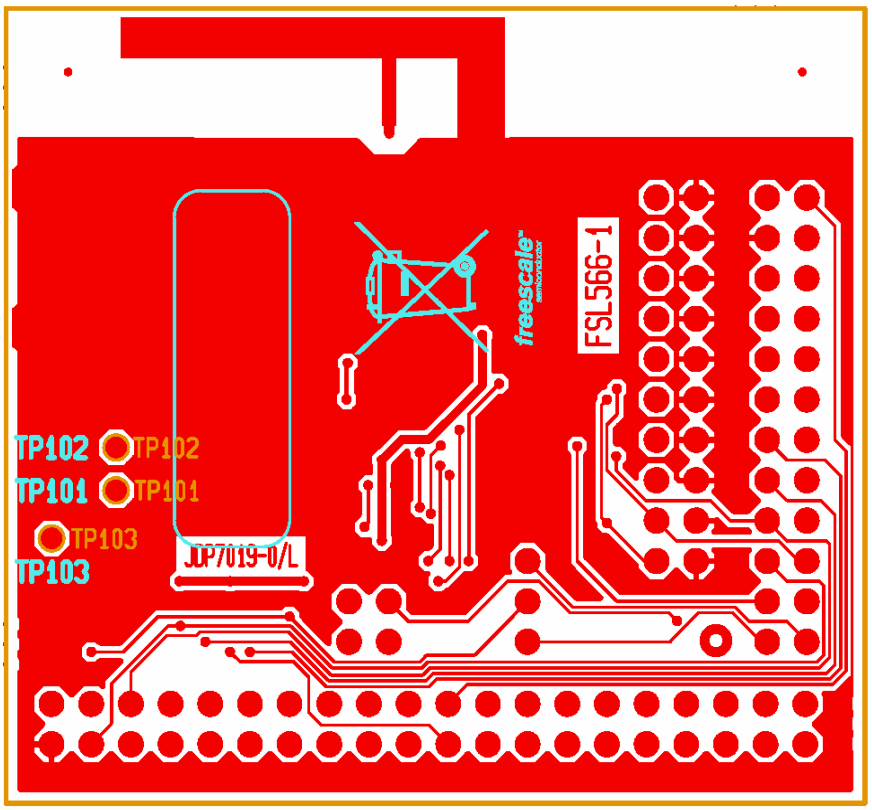

Figure 5-2. MC1320x Daughter Card (Bottom View)

5.1 Development Board Interconnects

The following sections describe the interconnects for both the GB60 and M52235 Development boards. Table 5-1 lists the pin connections for J101 and Table 5-2 lists the pin connections for J102.

Table 5-1. J101 Pin Connections

Pin Number	Pin Name	Description	Functionality
1,2,3,4, 6,7,8,9, 10,11,12, 15,16,17 18,21,23, 25,26,28, 29, 30,33	N/C		No connection.
5	PTA2	Connects to PTA2 on GB60.	Provides a wakeup function to the MCU via Pin 22 when jumper is installed between J103 pins 1 and 2.
13	GPIO1	Connects to General Purpose Input/Output 1 of MC1320X.	When gpio_alt_en, Register 9, Bit 7 = 1, GPIO1 functions as an “Out of Idle” Indicator.
14	GPOI2	Connects to General Purpose Input/Output 2 of MC1320X.	When gpio_alt_en, Register 9, Bit 7 = 1, GPIO2 functions as a “CRC Valid” Indicator.

Table 5-1. J101 Pin Connections (continued)

Pin Number	Pin Name	Description	Functionality
19	$\overline{\text{IRQ}}$	Connects to $\overline{\text{IRQ}}$ pin of MC1320X.	Allows the MC1320X to issue an $\overline{\text{IRQ}}$ to the MCU.
20	$\overline{\text{RESET}}$	Optionally connects to $\overline{\text{RESET}}$ of MC1320X when R101 or R102 are installed.	Allows the MCU to reset the MC1320X.
22	PTE1/RXD1	Connects to PTE1/RXD1 of GB60.	Provides a wakeup function to the MCU via Pin 5 when jumper is installed between J103 pins 1 and 2.
24	XCLK/16MHz	Connects to CLKO of MC1320X when jumper is installed between J103 pins 3 and 4.	Provides reference based on MC1320X 16 MHz reference oscillator to the MCU.
27	PTC2/BAUD SEL	Connect to PTC2/BAUD SEL of GB60.	
31	$\overline{\text{RXTXEN}}$	Connect to $\overline{\text{RXTXEN}}$ of MC1320X.	Allows the MCU to control the $\overline{\text{RXTXEN}}$ line of the MC1320X.
32	$\overline{\text{RESET}}$	Connects to $\overline{\text{RESET}}$ of MC1320X.	Allows the MCU to reset the MC1320X.
34	PTD5/CESI/$\overline{\text{ATTN}}$	Connects to PTD5/CESI of GB60 when R104 is installed. Connect directly to Pin 15 of J102.	Allows the MCU to wake up the MC1320X from Doze or Hibernate.
35	MOSI	Connect to MOSI of MC1320x.	SPI
36	SPSCK	Connect to SPICLK of the MC13201.	SPI
37	CE	Connect to CE of MC1320X.	SPI
38	MISO	Connects to MISO of MC1320X.	SPI
39	V_IN	Connects the Daughter Card to the supply voltage output of the GB60 board.	Provides supply voltage to the Daughter Card. Voltage must not exceed 16 Vdc. See Section 5.1.0.3, “Power Connections”.
40	GND	Connect ground on GB60 board to ground on Daughter Card.	

Table 5-2. J102 Pin Connections

Pin Number	Pin Names	Description	Functionality
4, 5, 6, 7, 8, 11, 12, 14, 16, 18, 22	N/C		No connection
1	V_IN	Connects the Daughter Card to the supply voltage output on the M52235EVB.	Provides supply voltage to the Daughter Card. Voltage must not exceed 16 Vdc. See Section 5.1.0.3, “Power Connections”.
2	$\overline{\text{IRQ}}$	Connects to $\overline{\text{IRQ}}$ pin of MC1320X.	Allows the MC1320X to issue an $\overline{\text{IRQ}}$ to the MCU.
3	GND	Connects the ground of the RF Daughter Card to the ground of the M52235EVB	
9	GPIO1	Connects to General Purpose Input/Output 1 of MC1320X.	When gpio_alt_en, Register 9, Bit 7 = 1, GPIO1 functions as an “Out of Idle” Indicator.
10	GPOI2	Connects to General Purpose Input/Output 2 of MC1320X.	When gpio_alt_en, Register 9, Bit 7 =1, GPIO2 functions as a “CRC Valid” Indicator.
13	$\overline{\text{RESET}}$	Connects to $\overline{\text{RESET}}$ of MC1320X and Pin 32 of J101.	Allows the MCU to reset the MC1320X.
15	PTD5/CESI	Connects to $\overline{\text{ATTN}}$ of MC1320X and Pin 34 of J101.	Allows the MCU to wake up the MC1320X from Doze or Hibernate.
17	MOSI	Connects to MOSI of MC1320X.	SPI
19	MISO	Connects to MISO of MC1320X.	SPI
20	$\overline{\text{RXTXEN}}$	Connect to $\overline{\text{RXTXEN}}$ of MC1320X.	Allows the MCUntrol the $\overline{\text{RXTXEN}}$ line of the MC1320X.
21	SPICLK	Connect to SPICLK of the MC1320X	SPI
23	PTE2/CE-QSPI-CSO	Connects to Pin 1 of J104	Allows Chip Enable (CE) selection. See Section 5.1.0.1, “SPI Connections”.
24	PTE2/CE-AN7	Connects to Pin 3 of J104	Allows Chip Enable (CE) selection. See Section 5.1.0.1, “SPI Connections”.

NOTE

In the following sections, pin numbers not in parenthesis reference the GB60 Development Board. Pin numbers in parenthesis reference the M52235 Development Board.

5.1.0.1 SPI Connections

J101 pins 35 through 38 (J102 pin 17, 19, 21 and 23) provide the following four wire SPI interface:

- MOSI
- SPICLK
- $\overline{\text{CE}}$
- MISO

The MC1320x always functions as a slave device. SPI operation is described in detail in the appropriate *MC1320x Data Sheet* and/or *MC1320x Reference Manual*.

NOTE

As it applies to the M52235 Development Board, the $\overline{\text{CE}}$ signal on (J102 Pin 23 and Pin 24) are hard wired to header J104. These pins control the functionality of $\overline{\text{CE}}$.
When Pin 2 and Pin 3 of J104 are shorted, $\overline{\text{CE}}$ is wired to (J102 Pin 24) (PTE2/CE-AN7).
When Pin 1 and Pin 2 of J104 are shorted, $\overline{\text{CE}}$ is wired to (J102 Pin 23) (PTE2/CE-QSPI_CS0).

5.1.0.2 Control Connections

- J101 Pin 19 (J102 Pin 2) is the $\overline{\text{IRQ}}$ line from the MC1320x. Connection to the MCU depends on how the MCU services interrupts.
- J101 Pin 31 (J102 Pin 20), $\overline{\text{RXTXEN}}$, allows the MCU to initiate transceiver functions.
- J101 Pin 34 (J102 Pin 15), $\overline{\text{ATTN}}$, allows the MCU to wake up the MC1320x from Doze or Hibernate low power modes.

NOTE

$\overline{\text{RXTXEN}}$ and $\overline{\text{ATTN}}$ are also available at header J105 for manual control.

- J101 Pin 24 provides the MC1320x CLKO to the MCU when a jumper is installed at J103.
- J101 Pin 32 (J102 Pin13) interfaces with the MCU to provide a Reset to the MC1320x.
- J101 Pin 5 and Pin 22 provide a wake up function to the MCU when a jumper is installed at J103.
- J101 Pin 13 and Pin 14 (J102 Pin 9 and Pin 11) provide access to the MC1320x GPIO1 and GPIO2 ports.

5.1.0.3 Power Connections

J101 Pin 39 (J102 pin 1) provides the supply voltage to the RF Daughter Card. Voltage on this line should never exceed 16.0 VDC and the nominal voltage supply should not exceed 16.0 VDC. J101 Pin 40 (J102 pin 3) is ground.

NOTE

MCU connection signals are dependent on the on-board voltage regulator. If R105, D101, and C101 are mounted and R115 is removed, J101 Pin 39 will provide the interface supply voltage which must never exceed 3.6 V. Nominal supply voltage should never exceed 3.4 V.

5.1.0.4 Non-MCU Connections

Header J105 provides connections to a number of MC1320x contacts for non-MCU connections. As already stated, the $\overline{\text{RXTXEN}}$ and $\overline{\text{ATTN}}$ lines are available at J105 for external control using switches or other hardware. The MC1320x GPIO is also available for connection to external hardware.

6 RF Circuit

The MC1320x has an internal TX/RX switch. This feature allows for an external RF circuit that has a very low component count. The MC1320x requires only a few passive components and a balun to provide an interface to an antenna or a 50 ohm circuit. Figure 6-1 shows a schematic for only the RF portion of the MC1320x Daughter Card.

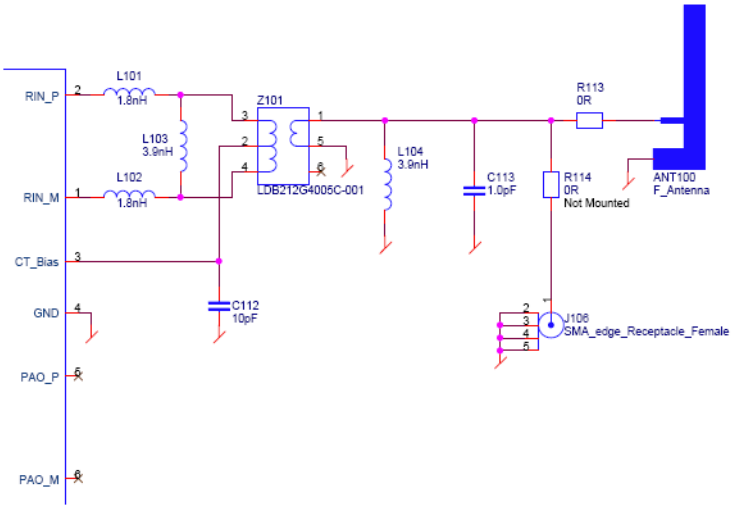

Figure 6-1. RF Portion of 20x Daughter Card

To provide a design that is of the lowest possible cost to produce, this reference design was built on a printed circuit board consisting of only two layers and with a printed circuit board antenna. The antenna is an Inverted F design widely used in the 2.4 GHz band. This antenna provides good performance while minimizing Bill of Material (BOM) cost.

For more information on a low cost design approach, see the *ZigBee Hardware Design Considerations Reference Manual* (ZHDCRM)

7 Software Configuration

As shown in Figure 8-1, the legend in the schematic shows the recommended jumper settings for Wake, ClkOut, and Chip Enable.

NOTE

The Wake and ClkOut signals are only for interface to the GB60 Development Board. The Chip Enable signal is only for interface to the M52235 Development Board.

For software development, Freescale recommends users obtain the most recent software development tools and documentation from the following web pages:

- For ZigBee related software and documentation go to www.freescale.com/zigbee
- For microcontroller software and documentation go to www.codewarrior.com

8 Bill of Materials (BOM) and Schematic

This section contains the RF Daughter Card BOM and schematic.

Table 8-1. Bill of Materials

Qty	Part Number	Value	Rating Tolerance	Manufacturer	Part Number	Reference
1	96000310100	Label 21*6mm Test BarCode		96000310100	BARCODE101	
3	50610710001	100nF	16V ±10% X7R	Murata	GRM155R71C104KA88D	C103, C104, C105
0	50610710001	100nF	16V ±10% X7R	Murata	GRM155R71C104KA88D	C101 (Not Mounted)
2	50620810001	1µF	6.3V ±10% X5R	Murata	GRM188R60J105KA01D	C102, C106
0	50620810001	1µF	6.3V ±10% X5R	Murata	GRM188R60J105KA01D	C108 (Not Mounted)
0	50610610000	10nF	16V ±10% X7R	Murata	GRM155R71E103KZ01E	C107(Not Mounted)
1	53300833001	3.3µF	10V 20%	Vishay Sprague	293D335X0010A2TE3	C109
2	50210268000	6.8pF	50V ±0.25pF NP0/C0G	Murata	GRM1555C1H6R8DZ01J	C110, C111
1	50210310000	10pF	50V ±5% NP0/C0G	Murata	GRM1555C1H100JZ01D	C112
1	50210210000	1.0pF	50V ±0.25pF NP0/C0G	Murata	GRM1555C1H1R0CZ01D	C113
0	40110003303	MM3Z3V3T1G	3.3V/200mW 5%	ON Semiconductor	MM3Z3V3T1G	D101 (Not Mounted)
1	41100017001	Green_LED		Citizen	CL-170G-CD-T	D102
1	35501320200	MC13202		Freescale Semiconductor	MC13202	IC101
1	34000298109	LP2981IM5-3.3	-40 to +125°C	National	LP2981IM5-3.3 NOPB	IC102
1	20030404001	2*20p Pin Header - Right Angle	mot/molex70216-40	10-89-4402	J101	
1	20030402401	2*12p Pin Header - Right Angle	mot/molex70216-24	10-89-4242	J102	
1	20030400400	2*2p Pin Header		AMP	0-826632-2	J103
1	20030400300	jumper_1x3		AMP	826629-3	J104

Table 8-1. Bill of Materials

Qty	Part Number	Value	Rating Tolerance	Manufacturer	Part Number	Reference
0	20030402008	2*10 Pin Header		AMP	1-826632-0	J105 (Not Mounted)
1	20150700202	SMA_edge_Receptacle_Female	mot/sma-end_launch	142-0701-831	J106	
2	20030000100	ProbeLoop		Toby Electronics	TP-107-02-5-T	J107, J108
2	54710518001	1.8nH	300mA ±0.3nH	TOKO	LL1005-FHL1N8S	L101, L102
2	54710539002	3.9nH	±0.3nH	TOKO	LL1005-FHL3N9S	L103, L104
1	71000566010	fsl566-1		Freescale Semiconductor	FSL566-1 FR4 0.76mm	PCB101
4	61100000001	0R	62.5mW/25V 5%	YAGEO	RC0402JRE070RL	R103, R112, R115,R104
0	61100000001	0R	62.5mW/25V 5%	YAGEO	RC0402JRE070RL	R101, R102 (Not Mounted)
0	61100410001	100R	62.5mW/25V 5%	YAGEO	RC0402JRE07100RL	R105 (Not Mounted)
0	61100610001	10K	62.5mW/25V 5%	YAGEO	RC0402JRE0710KL	R106, R107, R108, R110 (Not Mounted)
1	61100747000	470K	62.5mW/25V 5%	YAGEO	RC0402JRE07470KL	R109
1	61100422000	220R	62.5mW/25V 5%	YAGEO	RC0402JRE07220RL	R111
1	61120000001	0R	125mW/150V 5%	YAGEO	RC0805JRE070RL	R113
0	61120000001	0R	125mW/150V 5%	YAGEO	RC0805JRE070RL	R114 (Not Mounted)
1	58130916004	16.000MHz	±20ppm ±20ppm	KDS	ZD00882	X101
1	56360240001	LDB212G4005C-001		Murata	LDB212G4005C-001	Z101

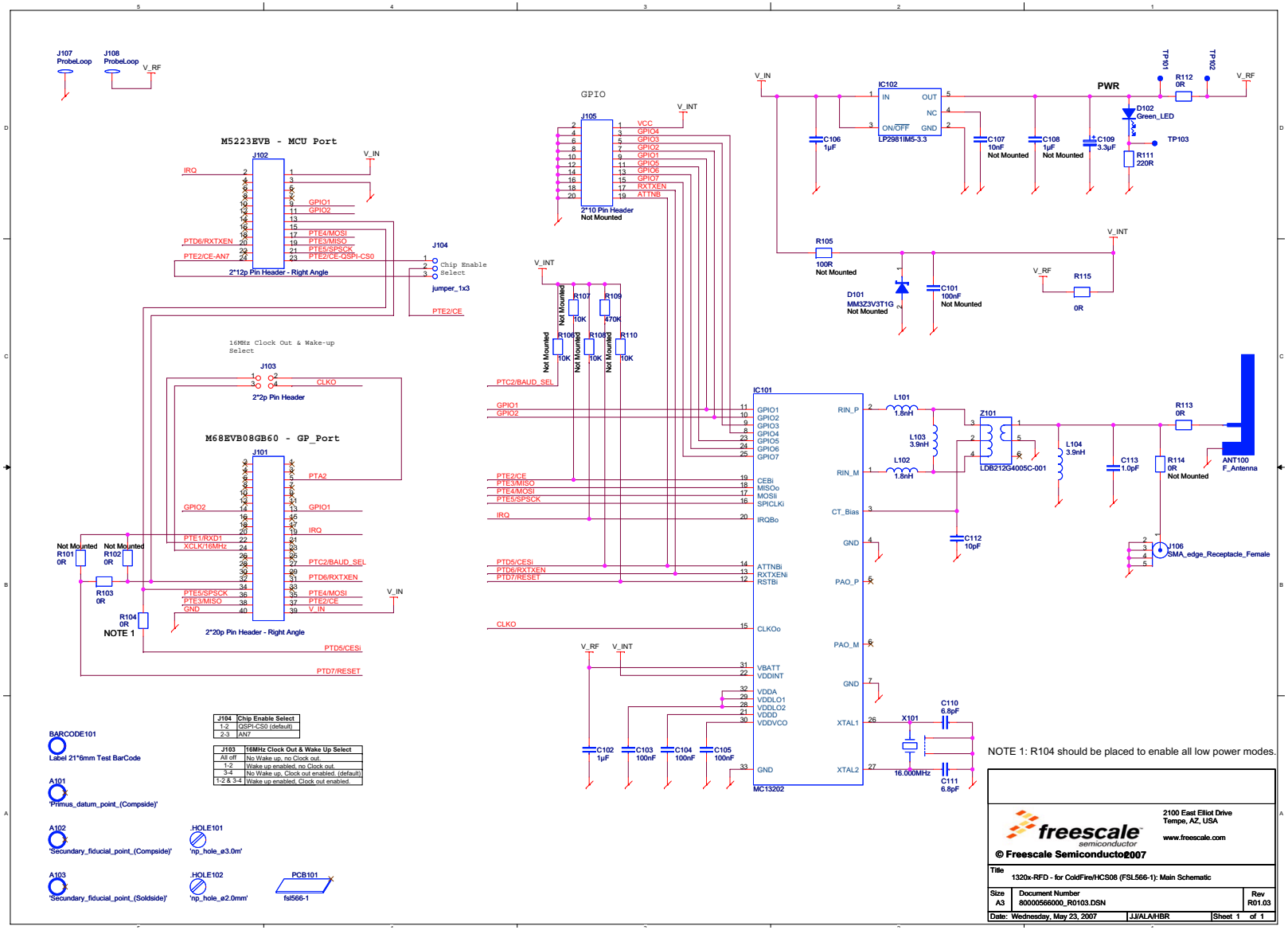

Figure 8-1. Daughter Card Schematic

NOTES

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Document Number: MC1320xRFCUG
Rev. 1.2
03/2010

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