Freescale Semiconductor
Application Note

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NOTE: The theory in this application note is still applicable, but some of the products referenced may be discontinued.

Mounting Method for the MHVIC910HNR2 (PFP-16) and Similar Surface Mount Packages

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INTRODUCTION

This application note describes the mounting methodology for a surface mount plastic device with an exposed heat sink and multiple leads. This mounting methodology was developed for the plastic package commonly known in the industry by its designation PFP-16. The dimensions of the PFP-16 package are listed in Freescale's Case Outline 978 and are found in the *Freescale Wireless RF Product Device Data* book, DL110, and on the Freescale Semiconductor Web site, http://www.freescale.com/rf. The PFP-16 is the standard JEDEC designation for a power flat package with exposed heat sink (for power application) and 16 leads. This mounting methodology is recommended for any device in the same package. The specific design and assembly process to be used will depend on the actual application and the manufacturing platform. Similar methodology can be developed for any surface mount package with similar materials and construction.

The most critical elements to address when developing a mounting or assembly process are:

- Obtaining a good solder joint, particularly under the heat sink
- Determining the heat dissipation path and thermal management of the device and PCB structure
- Avoiding overstressing the part during assembly and solder reflow.

The mounting method described here addresses these issues and should be used as a guide for developing a specific design and assembly process flow for individual applications.

Currently Freescale has two types of RF Power devices in the PFP-16 package. Devices such as the MHVIC910HNR2 are multi-stage amplifier integrated circuit (IC) devices. Devices such as the MRF9002 are discrete power transistors similar to those available in metal-ceramic packages. These devices use Freescale's newest High Voltage (26 Volts) LDMOS discrete and IC technology and are designed for base station PA applications. The target applications include macrocell driver function or microcell final stage in the base station power amplifier. Figure 1 shows the PFP-16 package. The MHVIC910HNR2 operates at 900 MHz with an RF output power of 10 Watts (40 dBm).

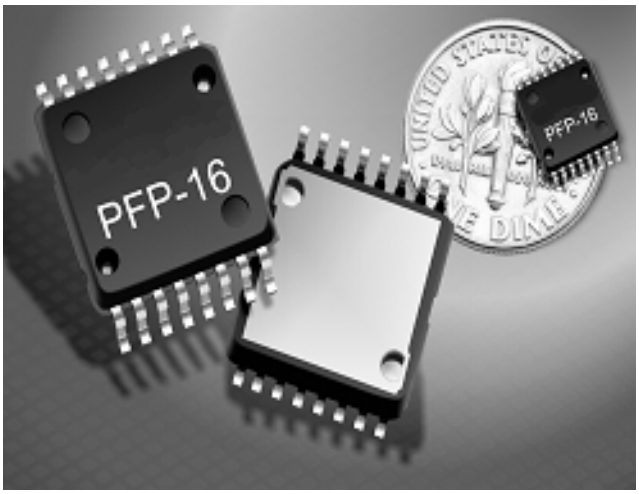

Figure 1. PFP-16 Package (Case 978)

PACKAGE DESCRIPTION

The PFP-16 package uses the conventional lead-frame and overmolded plastic packaging technology commonly found in discrete and IC semiconductor packages. The lead frame for the package is made out of Cu alloy with palladium over nickel plating. Because the PFP-16 package is designed for power applications, the package has a heat sink that is also attached to the lead frame. The heat sink is made from high conductivity copper and plated with palladium over nickel. The die is attached directly to the heat sink. The device is then overmolded using thermoset material in a transfer molding process. In the overmolded package, the underside of the heat sink remains exposed. After the mold compound is cured, the individual units are singulated, and the leads are trimmed and formed in a gull-wing shape. The mounting of the device requires soldering the leads to the appropriate pads on the PCB as well as soldering the exposed portion of the heat sink on the underside of the device to a separate pad on the printed circuit board (PCB).

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The PFP-16 is a surface mount device and is suitable for standard surface mount assembly processes using pick-and-place equipment and common solder reflow processes. Because of the large amount of power being dissipated by the device, the mounting consideration requires an evaluation of thermal dissipation through the PCB. The following section covers the PCB design and its impact on the heat dissipation of the device mounted on top of the PCB. After the PCB design is completed, the next step is assembling the device so that it provides a reliable assembly. A discussion follows on the major process steps needed to assemble a small quantity of PCBs, used to conduct the power cycling and thermal cycling to show the robustness of the assembly. These PCBs are also used to collect temperature data to validate the PCB design.

Thermal Design of the PCB

The PFP-16 package is designed for power devices. In its construction, the die is mounted directly on the copper heat sink. The bottom part of this heat sink is exposed at the base of the package and is provided with the same solderable surface as the leads (Pd over Ni). The leads are formed in a gull-wing shape where the bottom of the lead is slightly lower than the bottom of the heat sink. In the PCB design, a solder pad is provided for each of the 16 leads as well as the heat sink. A typical pad layout used in our design is shown in Figure 2. It has a 6.1 mm (0.240″) square solder pad in the middle for the heat sink and eight land areas 0.41 mm x 0.89 mm (0.016″ x 0.035″) on each side at 0.8 mm (0.032″) pitch for the leads. The maximum lead tip-to-tip dimension is 9.15 mm (0.360″). If more pronounced fillet on the inside of the lead is desired, the pads can be elongated inwards by increasing the 0.035″ (0.89 mm) dimension and correspondingly decreasing the 0.300″ (7.62 mm) dimension. For the PFP-16 package, the mm dimensions are governing dimensions.

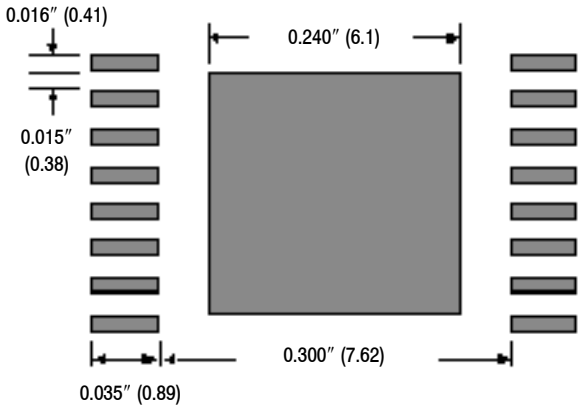

Figure 2. Typical Pad Layout for the PFP-16 Package

In the PFP-16 package, the heat dissipation path is from the junction at the top of the die through the die thickness and the die attach thickness through the copper heat sink to the bottom of the part. From the bottom of the heat sink, the heat is dissipated through the solder joint and PCB. Normally, the PCB material is not very conductive. In order to dissipate the heat through the PCB thickness, via holes are used to connect the top and bottom copper layers in the PCB. Via holes are drilled through the thickness and are plated with copper in the barrel of the via hole. Via holes can be filled or unfilled. In general, the thermal resistance of a via structure is governed by the number of via holes, hole diameter and the thickness of copper in the barrel. Filled via holes have only slight thermal improvement over unfilled via holes. The advantage of having filled via holes is that they prevent the solder on the top of the pad from being drawn into the via holes during reflow process. If the solder were being drawn into the via hole during reflow, it could create a void under the heat sink. In addition, solder may collect on the bottom side of the PCB and interfere in bolting the PCB to the finned chassis structure. There are multiple ways in which filled via holes can be created. Some of the more common ones are prefilling the via holes with solder, filling them with organic material such as silver-filled epoxy, and providing additional solder paste on the pad so that there is enough solder available to create a good solder joint even when the solder is drawn into the via holes. Polyamide-type tape material can be used on the backside to prevent the solder from collecting on the bottom side of the PCB. The tape is removed after soldering so it does not increase the interface resistance.

In manufacturing the PCB, CB-100 ViaPlug® material from duPont® was used to fill the via holes. This material is designed to be screen printed on top of the substrate and allowed to flow into the via holes. Typically, vacuum is applied during this process to help the material flow into the via holes. After drying at 115°C for 15 minutes, the material is planarized by scrubbing on the top and bottom of the PCB. After planarization, the substrate is cured at 160°C for 45 minutes. After curing, the material is plated over with a small amount of Cu. The substrate is then patterned and etched to create a PCB.

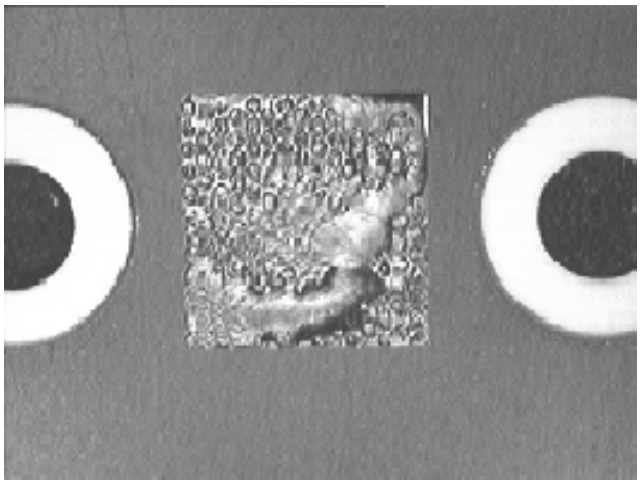

Figure 3. Surface Mount Solder Pad on Top of the Via Structure

Figure 3 shows the finished PCB with the filled via structure in the solder pad for the heat sink created using this process. The PCB was also plated with solder. Figures 4 and 5 show the horizontal and vertical cross-sections through the via holes indicating internal details of the via hole. The via holes are 0.015″ (0.38 mm) in diameter and located in a diamond pattern. The distance between the two via hole centers within a row is .030″ (0.76 mm). The spacing between each row is 0.010″ (0.25 mm). This creates a very closely spaced via

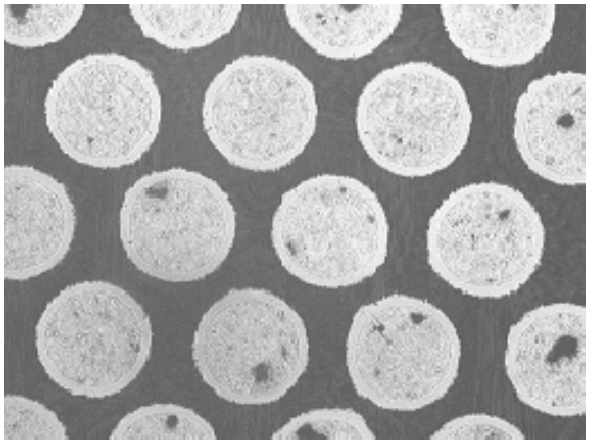

Figure 4. Via Hole Cross-section Parallel to the Solder Pad

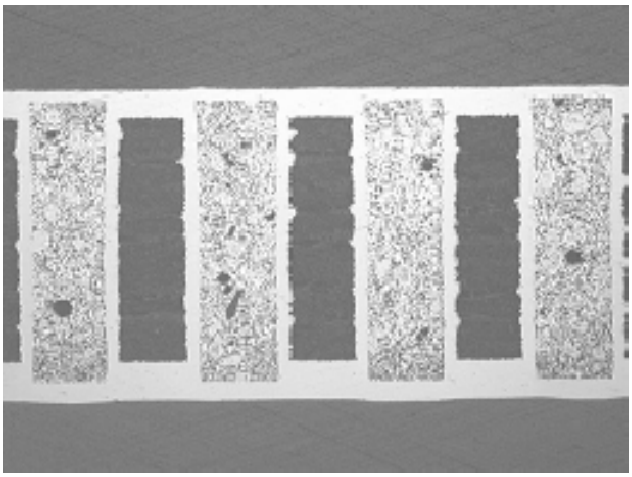

Figure 5. Via Hole Cross-section Through the Thickness of the PCB

pattern. The via holes were plated with 1 oz. (35 μm) of Cu in the barrel. For better thermal performance, 2 oz. (70 μm) of Cu in the barrel of the via hole can be used.

Figures 4 and 5 show a filled via structure with planarized top and bottom surfaces created using the method described here. This method provides a good soldering of the part to the PCB as well as mounting of the PCB to the finned chassis. Small amount of voids can be seen in the filler material within the via holes. The contribution of the filler material to the heat dissipation through the thickness is very minimal. The primary heat conducting path is the thickness of Cu in the barrel of the via holes.

The test board used here was a double-sided PCB using Rogers® RO4350 material for the substrate. The process described here can be used for any substrate material for either double-sided or multi-layer PCBs. All of the processes used here (for example, printing, drying and curing) are commonly used in manufacturing PCBs.

Thermal Design of the PCB

As mentioned before, the main heat dissipation path for a surface mount package such as the PFP-16 is from the die to the package heat sink through the solder joint and then through the PCB thickness to the finned chassis. The finned chassis is cooled either by free air or forced air convection. Because the PCB material is not very conductive, the thermal resistance of the PCB contributes a significant portion of the total thermal resistance from junction to ambient. Thus, it is very important that thermal considerations are addressed early in the PCB layout design process.

Figure 6 shows the test board with the MHVIC910HNR2 device soldered to the top side. The test board is made from 0.032″ (0.81 mm) thick Rogers RO4350 material. The board has a full layer of copper (1 oz., 35 μm) on the bottom side as well as a 0.240″ (6.1 mm) square solder pad of the same thickness on the top side. In addition, there are two bolt holes located on each side of the package. The bolt holes are located at 0.550″ (14.00 mm) center distance. The bolt holes assure that the PCB remains in close contact with the finned chassis or pallet to provide both electrical and thermal ground. As the device is powered, the area of PCB surrounding the MHVIC910HNR2 device heats and tends to expand. As the PCB expands, it may lift off, thus losing electrical and thermal contact. The test board also has a thermocouple attached to the side of the package heat sink to monitor the temperature of the device.

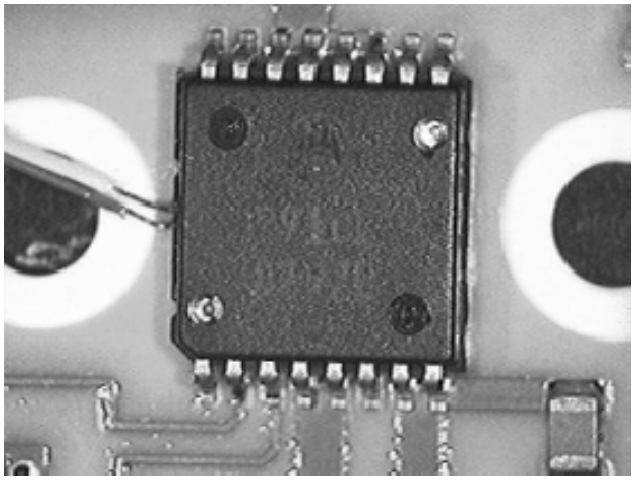

Figure 6. MHVIC910HNR2 Device on the Test Board

A finite element model of the test PCB with MHVIC910HNR2 device was created to compute temperature distribution within the device and the PCB. The model includes the region of the PCB surrounding the device, plus the die, the die attach, the package heat sink and the mold compound. Individual leads and the wires are not included because they are not expected to contribute to the heat dissipation. The model has a solder joint under the package heat sink as well as the PCB with top and bottom copper

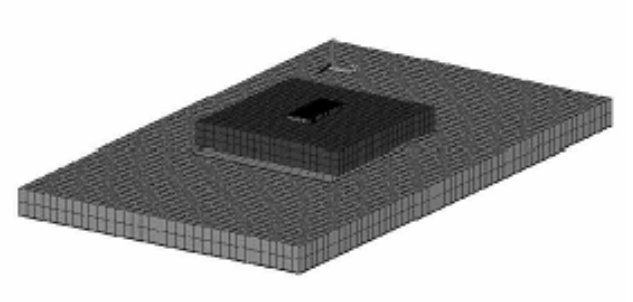

Figure 7. Finite Element Model of the MHVIC910HNR2 Device with Mold Compound Removed

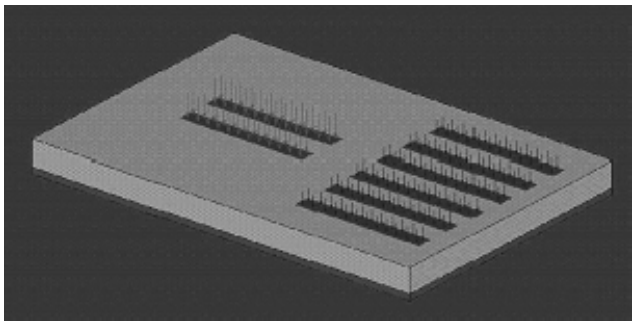

Figure 8. Close-up View of the Die with Heat Sources on the Die

layers. In addition, the via holes are represented by conduction link elements connecting the top copper layer under the package to the bottom copper layer. Figure 7 shows the finite element model with the mold compound removed to show the die. Figure 8 shows the close-up die and the heat sources within the die.

The MHVIC910HNR2 is a two-stage IC, with six active regions in the output stage and two active regions in the driver stage. Each active region consists of several source, gate and drain pairs. The individual active regions are shown with arrows indicating that the heat is uniformly dissipated over this region of the die only. The total power dissipated by the die is assumed to be 12 Watts for the simulation. Out of this total dissipation, the two active regions in the driver stage are assumed to contribute 2.363 Watts each, and the six output stage active regions are assumed to contribute 1.212 Watts each. Because the power density is higher in the driver stage of this die, the maximum temperature is expected to occur in that region rather than in the output stage.

The analysis assumes that all power is dissipated by conduction through the PCB. All convection and radiation losses are assumed to be zero. A very small percentage of power is typically dissipated via convection and radiation off the surfaces. The predominant heat dissipation mode is conduction through the package, PCB with via structure and to the copper pallet on which the test board is mounted.

Simulation and IR Scan Results

The finite element model was used to estimate the temperature distribution in the test setup described above. The model was used to validate that the proposed via structure is adequate for the amount of power being dissipated by the device. In simulation, the diamond via pattern with two different spacings was examined: 0.030″ x 0.010″ (0.76 mm x 0.25 mm) and 0.030″ x 0.015″ (0.76 mm x 0.38 mm). The finite element analysis results indicated that the 0.030″ x 0.015″ via spacing would be only slightly worse than the 0.030″ x 0.010″ via spacing. The more closely spaced via structure does add to the cost of PCB fabrication. Because the test boards were procured with 0.030″ x 0.010″ spacing, the results presented here are for that via spacing.

Figure 9 indicates the temperature distribution in the die at 12 Watts of dissipated power. As expected, the driver stage in the die is slightly hotter than the output stage. The maximum junction temperature was computed to be 139.9°C.

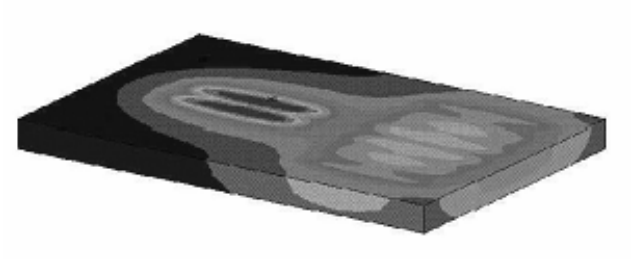

Figure 9. Temperature Distribution in the Die

The finite element model was used to derive temperature at three additional locations. One location is the side of the package heat sink where the thermocouple is attached to the device. The second location is the top of the epoxy mold compound, and the third is the top of the PCB near the output side of the device. In addition to these locations, the maximum temperature at the bottom of the device (case temperature), as well as the temperature on the top and bottom sides of the PCB, were extracted to derive package and PCB thermal resistance. The temperature results are tabulated in Table 1.

Table 1. Comparison between Simulation and IR Scan Results

	Simulation Results	IR Scan Results
Dissipated Power	12 W	12 W
Top of the Mold Compound or Package	111.4°C	115.4°C
Die Junction	139.9°C	
Device Case	103.2°C	
Side of the Package Heat Spreader	96.3°C	97.5°C
Top of the PCB under the Device	102.7°C	
Bottom of the PCB under the Device	101.3°C	
Top of the PCB near the Output Side of the Device	~85°C	~84°C

A test board with two devices and the via structure described here was assembled using the surface mount assembly technique. These devices were used to perform temperature measurement using IR Scan imaging. As mentioned earlier, the device heat sink has a thermocouple attached to the side, since that region will not be visible in the IR image. Three different devices were tested while powered

in DC mode. Each device was tested at three different power dissipation levels: 8 Watts, 10 Watts and 12 Watts approximately. The devices were allowed to stabilize before measurements were taken. The devices and the PCB region around them were painted with black paint of known emissivity. The whole PCB assembly was mounted on a copper pallet, which was located on the cold plate of the IR Scan equipment. The IR Scan was used to record the temperature distribution on the top surface of the device as well as the PCB. A typical IR Scan image is shown in Figure 10. The IR Scan measurements were used to validate the simulation results.

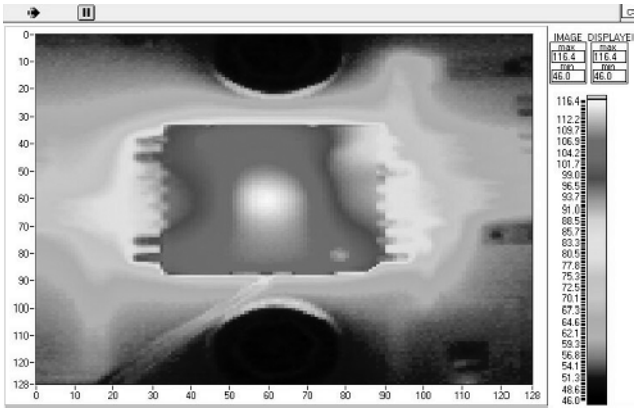

Figure 10. Typical IR Scan Image for the MHVIC910HNR2 on the PCB Being Tested

All three devices being tested showed similar results. The IR Scan image was used to compute the temperature at two locations: the top of the mold compound and the top of the PCB. In addition, the thermocouple recorded the temperature at the side of the heat spreader. The average results of the three devices at 12 Watts dissipated power are tabulated in Table 1 and compared with the simulation results.

The results presented here show that the test device in a PFP–16 package has a total thermal resistance of 3.06°C/W ((139.9–103.2)/12W). Similarly, the PCB with a dense via structure used here has the total thermal resistance of 0.12°C/W ((102.7–101.3)/12). If the via spacing is increased from 0.030″ x 0.010″ to 0.030″ x 0.015″, the number of via holes in the same pad are proportionately reduced. The simulation results indicate that when the spacing is increased, the thermal resistance for the PCB increases from 0.12°C/W to approximately 0.18°C/W. This amounts to an increase in junction temperature of less than 1°C.

From the results presented in Table 1, it can be stated that there is a very good correlation between the simulation results and the IR Scan results.

PCB ASSEMBLY

Assemblies used to verify the reliability of this mounting methodology were built in an automated solder mount assembly line. The PFP–16 devices were mounted to a PCB made from Rogers RO4350 material. The PCB was 0.032″ thick (nominal) with 1 oz. copper plating on the top and bottom surfaces. Solder mask covers both sides of the PCB with relief around solder pads and bolt holes. The backside of the PCB (the side that interfaces with the pallet) had full copper coverage, and the metal plane was exposed (no solder mask) in a region surrounding the bolt holes to provide sufficient contact between the ground plane and the pallet. The PCBs incorporate a dense via pattern on the solder pad beneath the PFP–16 devices to enhance heat transfer through the PCB (see Figure 3).

Two boltdown holes suitable for #4 screws were added in the PCB adjacent to each device at 0.55″ (14.00 mm) center–to–center spacing. These holes were specifically located near the devices to ensure that adequate board–to–chassis contact is maintained for optimum electrical and thermal grounding. Two DC circuits were created on each PCB to allow mounting two PFP–16 devices on the same board. PCB assembly used for the evaluation of the mounting methodology is shown in Figure 11. All soldering was accomplished in one pass using 62/36/2 Sn/Pb/Ag solder. Similar SnPb eutectic alloy Sn63 can also be used.

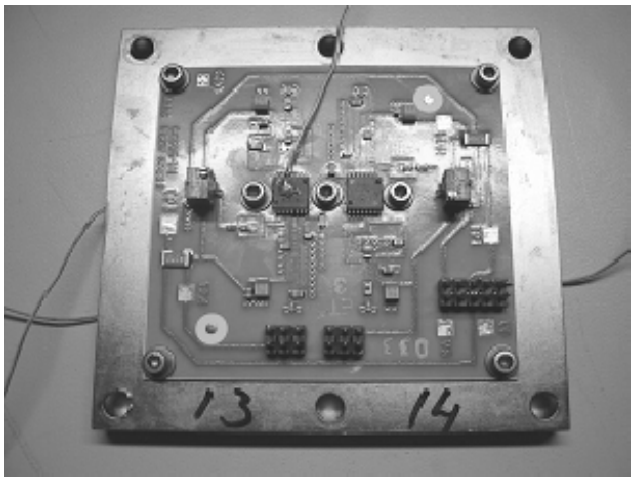

Figure 11. Assembled PFP–16 Power Cycling PCB and Pallet

The PCB assembly flow used to create the test boards was a conventional surface mount assembly flow. The PC boards with via holes and solder plating were procured from a board manufacturer. The PCB was first screen printed with Sn/Pb/Ag solder paste using a 0.006″ thick stainless steel solder stencil. After the application of the solder paste, the PCB was presented to the pick–and–place process, and it was populated using an industry standard pick–and–place machine. The MHVIC910HNR2 devices were provided in a tape and reel. After the PCB was populated, the solder was reflowed using a standard BTU convection furnace.

In the reflow step, the board was preheated to 150°C and held constant for a minimum of one minute to stabilize the board temperature. A “spike” above the 183°C liquidus temperature achieves the best reflow characteristics. To achieve the appropriate temperature profile, the peak temperature and belt speed of the reflow furnace were determined, based on the total mass of the assembly going through soldering. The time above the liquidus temperature was 90 seconds maximum, with 30 to 60 seconds typical. Maximum time above 150°C should be no more than 5.5 minutes. Figure 12 shows a typical reflow profile for this assembly.

In general, we recommend a no−clean solder paste of SnPb eutectic alloy such as Sn63, or equivalent be used for the assembly. The reflow profile recommended by the manufacturer of the solder paste should be followed. The thickness of the stencil should be designed to make sure that adequate solder volume is dispensed to create a good solder fillet at all the leads plus heat sink and leave no opens. Handling and storage of the packages before the reflow operation should follow the requirements of JEDEC Standards and appropriate MSL rating for the device.

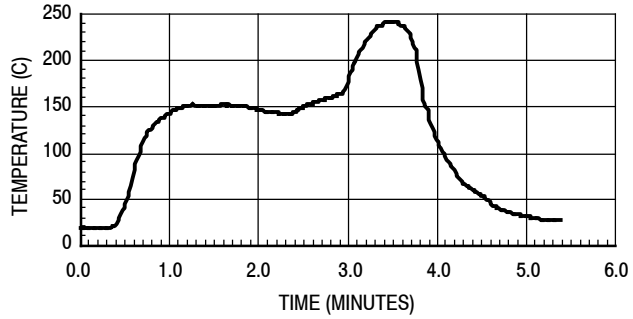

Figure 12. Typical Solder Reflow for Sn63 or Equivalent Solder

After the reflow operation, thermal grease was applied at the bottom of the PCB. The thermal grease was applied using a roller in a thin uniform layer. The thickness of the thermal grease layer was estimated to be ~ 0.001″ (0.025 mm). If the backside of the PCB is covered with solder mask, the thickness of the solder mask may prevent good electrical and thermal grounding in the via hole region. Care should be taken to ensure that proper electrical and thermal ground is provided in the via hole region. The PCB and components were then secured to a copper pallet using seven #4−40 socket head cap screws with a flat washer and a split washer. The use of a split washer with a flat washer in our testing was found to maintain the bolt load throughout the thermal excursion. The tightening torque used was 5 in.−lbs. for #4−40 screws. If M3 screws are used in place of #4−40 screws, the tightening torque should be 0.8 N−m. The complete assembly process flow is shown in Figure 13.

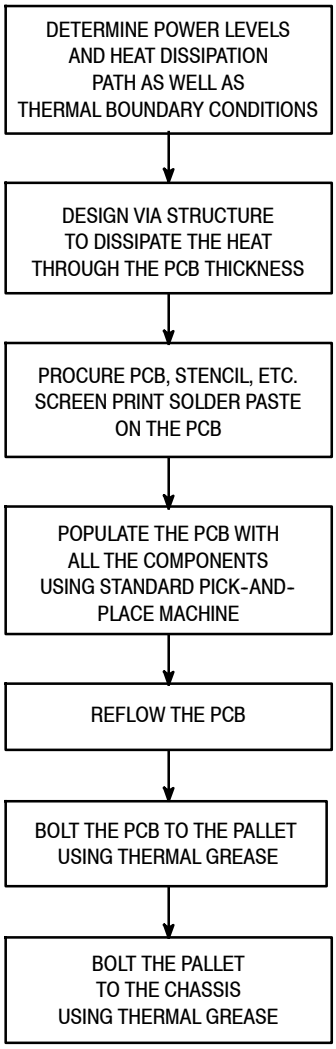

Figure 13. Process Flow for PCB Assembly

Reliability Testing Results

The reflowed boards, assembled on the pallets, were used to conduct power cycling and thermal cycling to verify that the boards assembled in this manner meet customer performance and reliability expectations. The assemblies used in the power cycling are shown in Figure 11. Each PCB had two devices mounted on them. Both devices can be independently powered. Forty such devices were assembled on the PCB. The PCBs were then bolted to the copper pallets, which were mounted on the finned heat sink. Each PCB had one device with a thermocouple on the top center of the device. The drain voltage and current were monitored to record the dissipated power for each device. The gate voltage on each device was adjusted using the potentiometer to reach the specified dissipated power. The junction temperature for each device was estimated based on the thermocouple reading for the top of the mold compound and the dissipated power times the thermal resistance. The devices were powered to provide 12 Watts of dissipated power. As shown in Table 1, the junction temperature was around 140°C. In power cycling, the power was turned on, and the temperature was monitored. A typical power vs. time cycle is shown in Figure 14.

In power cycling, the maximum junction temperature reached ~140°C. The power was turned on for 50 minutes. At 50 minutes, the power was turned off, and the fans on the heat sink were turned on. Once the power was turned off, the devices returned to room temperature in 10 minutes. At that point, the fans were turned off, and the power was turned back on. The devices were cycled for 1,000 power on/off cycles. All of the devices were tested for DC continuity, and the solder joints were examined visually for any cracking. No solder joint cracking was observed.

In addition, 10 additional devices soldered to the PCB and mounted on the pallet were put through temperature cycling. The temperature cycling was performed with 15 minutes of hold time at a high temperature of 150°C and a low temperature of −65°C. The temperature cycling was in air−to−air chambers, where the pallets moved from the hot side to the cold side. At each 250 cycles, the bolts were checked for the tightening torque. None of the bolts were

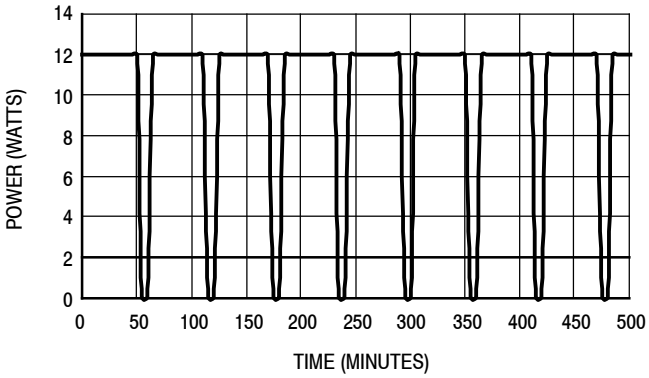

Figure 14. Power as a Function of Time for One Cycle

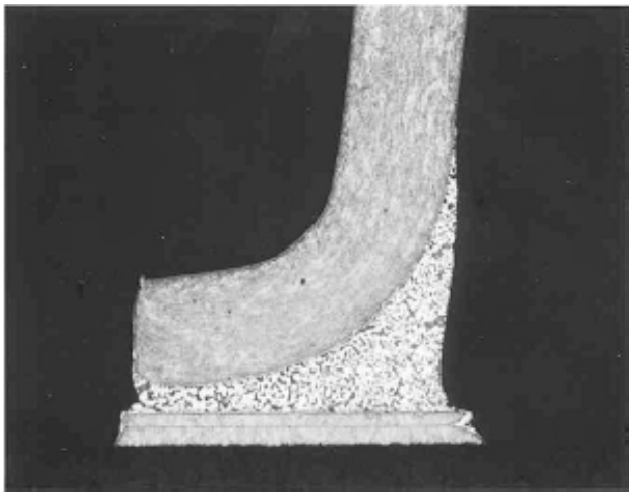

Figure 16. Cross-section of the Typical Solder Joint at the Lead to PCB Bond Pad

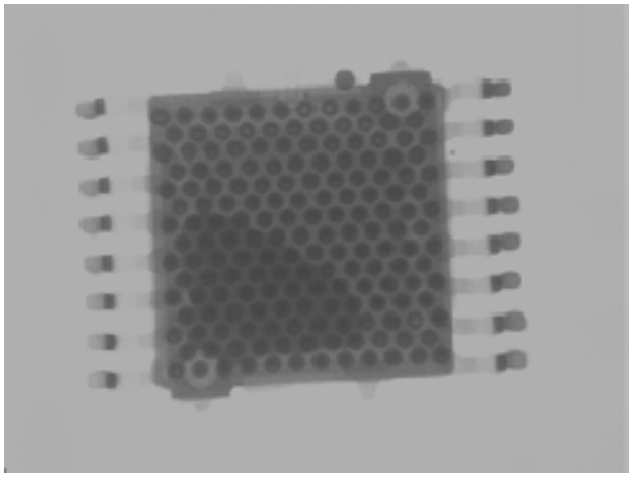

Figure 15. X-Ray Image of the Resulting Solder Joint Between the PFP-16 Package and the PCB After Thermal Cycling

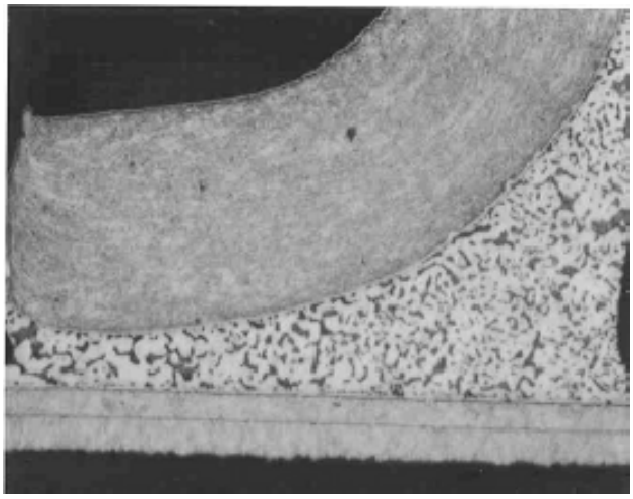

Figure 17. Close-up View of the Solder Cross-section at the Lead to PCB Bond Pad

found to be loose. At the end of 1,000 cycles, the PCBs were removed from the pallet, and all of the solder joints were examined visually.

To check the quality of the soldering, several PCBs were randomly selected, and an X-ray examination was performed. A typical X-ray image is shown in Figure 15.

In addition to the X-ray, all of the solder joints were visually examined. The appearance of the solder was shiny and smooth for the parts that were not thermal cycled and was dull and disturbed for the parts that were thermal cycled, as expected. Two solder joints at the leads were selected at random and cross-sectioned and examined for any sign of solder cracking. Figure 16 shows a typical cross-section of the solder joint at the lead. The cross-section indicates that there is a good wetting of the solder along the heel of the lead. The fillet at the toe is not as good as desired. This is due to bond pads that were 0.005″ (0.13 mm) shorter than specified in Figure 2. In spite of the poor fillet at the toe, there is only minor cracking in the solder joint. Other than the small crack, the rest of the solder joint was completely intact, and no other micro-cracks were noted. The solder structure shows signs of coarsening due to thermal cycling compared to the noncycled solder joint (Figure 17). Coarsening of the grain structure and the dullness of appearance is not uncommon after temperature cycling of the solder joint.

CONCLUSION

This application note describes a process for assembling PFP-16 devices on test boards and a process for designing the proper heat dissipation structure. It also details the reliability tests in terms of power cycling and thermal cycling. The successful completion of these tests shows that the methodology described here can provide a reliable assembly process. This application note provides a guide for developing a mounting assembly process. The steps outlined here can be used to develop a specific structure and a process that is adequate for the application and suitable for the process equipment.

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