



RF Power Field Effect Transistor

N-Channel Enhancement-Mode Lateral MOSFET

Designed for broadband commercial and industrial applications with frequencies from 865 to 895 MHz. The high gain and broadband performance of this device make it ideal for large-signal, common-source amplifier applications in 26 volt base station equipment.

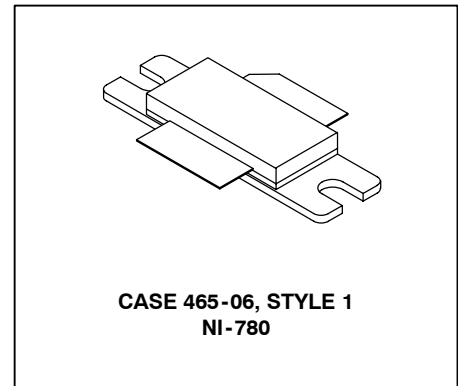
- Typical CDMA Performance @ 880 MHz, 26 Volts, $I_{DQ} = 700$ mA
 IS-95 CDMA Pilot, Sync, Paging, Traffic Codes 8 Through 13
 Output Power — 20 Watts
 Power Gain — 17.9 dB
 Efficiency — 28%
 Adjacent Channel Power —
 750 kHz: -45.0 dBc @ 30 kHz BW
 1.98 MHz: -60.0 dBc @ 30 kHz BW
- Capable of Handling 10:1 VSWR, @ 26 Vdc, 880 MHz, 90 Watts CW Output Power

Features

- Internally Matched for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Low Gold Plating Thickness on Leads, 40 μ m Nominal.
- RoHS Compliant
- In Tape and Reel. R3 Suffix = 250 Units per 56 mm, 13 inch Reel.

MRF9085LR3

**880 MHz, 90 W, 26 V
 LATERAL N-CHANNEL
 RF POWER MOSFET**



LIFETIME BUY

LAST SHIP 03 OCT 09
 LAST ORDER 04 APR 09

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	- 0.5, +65	Vdc
Gate-Source Voltage	V_{GS}	- 0.5, +15	Vdc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25 $^\circ\text{C}$	P_D	250 1.43	W W/ $^\circ\text{C}$
Storage Temperature Range	T_{stg}	- 65 to +150	$^\circ\text{C}$
Case Operating Temperature	T_C	150	$^\circ\text{C}$
Operating Junction Temperature	T_J	200	$^\circ\text{C}$

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	$^\circ\text{C}/\text{W}$

Table 3. ESD Protection Characteristics

Test Conditions	Class
Human Body Model	1 (Minimum)
Machine Model	M2 (Minimum)

Table 4. Electrical Characteristics ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics					
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 65\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 26\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current ($V_{GS} = 5\text{ Vdc}$, $V_{DS} = 0\text{ Vdc}$)	I_{GSS}	—	—	1	μAdc
On Characteristics					
Gate Threshold Voltage ($V_{DS} = 10\text{ Vdc}$, $I_D = 300\ \mu\text{Adc}$)	$V_{GS(th)}$	2.0	—	4.0	Vdc
Gate Quiescent Voltage ($V_{DS} = 26\text{ Vdc}$, $I_D = 700\ \text{mAdc}$)	$V_{GS(Q)}$	—	3.7	—	Vdc
Drain-Source On-Voltage ($V_{GS} = 10\text{ Vdc}$, $I_D = 2\ \text{Adc}$)	$V_{DS(on)}$	—	0.19	0.4	Vdc
Forward Transconductance ($V_{DS} = 10\text{ Vdc}$, $I_D = 6\ \text{Adc}$)	g_{fs}	—	8.0	—	S
Dynamic Characteristics ⁽¹⁾					
Output Capacitance ($V_{DS} = 26\text{ Vdc} \pm 30\ \text{mV(rms)ac}$ @ 1 MHz, $V_{GS} = 0\text{ Vdc}$)	C_{oss}	—	73	—	pF
Reverse Transfer Capacitance ($V_{DS} = 26\text{ Vdc} \pm 30\ \text{mV(rms)ac}$ @ 1 MHz, $V_{GS} = 0\text{ Vdc}$)	C_{rss}	—	2.9	—	pF

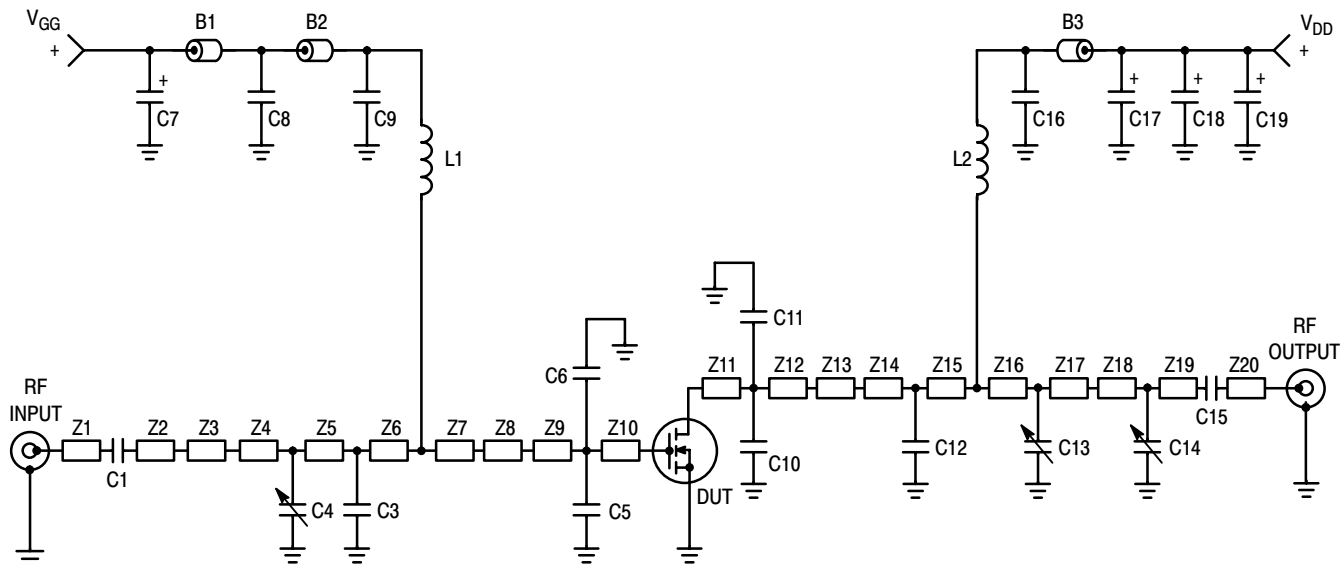
1. Part is internally input matched.

(continued)

Table 4. Electrical Characteristics ($T_C = 25^\circ\text{C}$ unless otherwise noted) (continued)

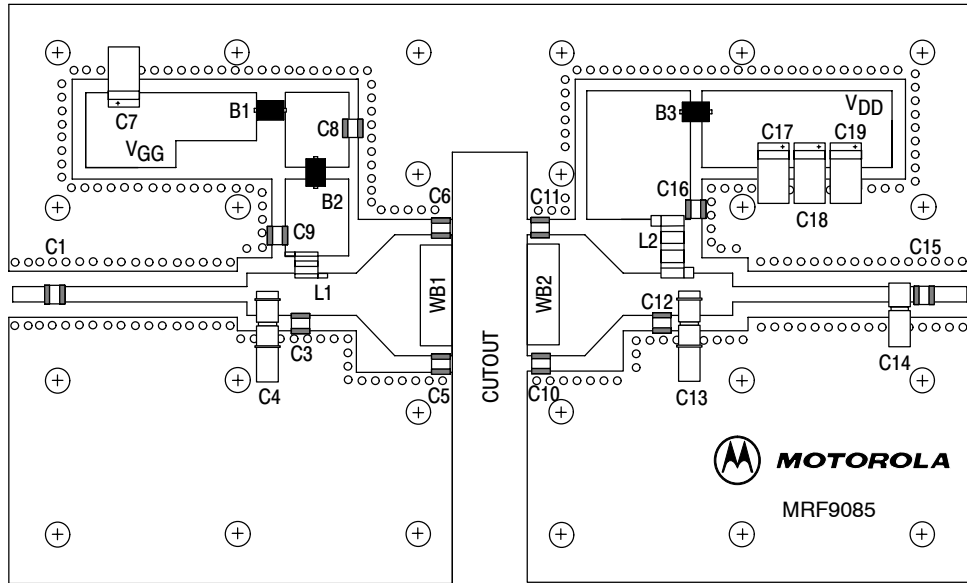
Characteristic	Symbol	Min	Typ	Max	Unit
Functional Tests (In Freescale Test Fixture, 50 ohm system)					
Two-Tone Common-Source Amplifier Power Gain ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 90\text{ W PEP}$, $I_{DQ} = 700\text{ mA}$, $f_1 = 880.0\text{ MHz}$, $f_2 = 880.1\text{ MHz}$)	G_{ps}	17	17.9	—	dB
Two-Tone Drain Efficiency ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 90\text{ W PEP}$, $I_{DQ} = 700\text{ mA}$, $f_1 = 880.0\text{ MHz}$, $f_2 = 880.1\text{ MHz}$)	η	36	40	—	%
3rd Order Intermodulation Distortion ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 90\text{ W PEP}$, $I_{DQ} = 700\text{ mA}$, $f_1 = 880.0\text{ MHz}$, $f_2 = 880.1\text{ MHz}$)	IMD	—	-31	-28	dBc
Input Return Loss ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 90\text{ W PEP}$, $I_{DQ} = 700\text{ mA}$, $f_1 = 880.0\text{ MHz}$, $f_2 = 880.1\text{ MHz}$)	IRL	—	-21	-9	dB
Two-Tone Common-Source Amplifier Power Gain ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 90\text{ W PEP}$, $I_{DQ} = 700\text{ mA}$, $f_1 = 865.0\text{ MHz}$, $f_2 = 865.1\text{ MHz}$)	G_{ps}	—	17.9	—	dB
Two-Tone Drain Efficiency ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 90\text{ W PEP}$, $I_{DQ} = 700\text{ mA}$, $f_1 = 865.0\text{ MHz}$, $f_2 = 865.1\text{ MHz}$)	η	—	40.0	—	%
3rd Order Intermodulation Distortion ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 90\text{ W PEP}$, $I_{DQ} = 700\text{ mA}$, $f_1 = 865.0\text{ MHz}$, $f_2 = 865.1\text{ MHz}$)	IMD	—	-31	—	dBc
Input Return Loss ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 90\text{ W PEP}$, $I_{DQ} = 700\text{ mA}$, $f_1 = 865.0\text{ MHz}$, $f_2 = 865.1\text{ MHz}$)	IRL	—	-16	—	dB
Power Output, 1 dB Compression Point, CW ($V_{DD} = 26\text{ Vdc}$, $I_{DQ} = 700\text{ mA}$, $f_1 = 880.0\text{ MHz}$)	P_{1dB}	—	105	—	W
Common-Source Amplifier Power Gain ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 90\text{ W CW}$, $I_{DQ} = 700\text{ mA}$, $f_1 = 880.0\text{ MHz}$)	G_{ps}	—	17.5	—	dB
Drain Efficiency ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 90\text{ W CW}$, $I_{DQ} = 700\text{ mA}$, $f_1 = 880.0\text{ MHz}$)	η	—	51	—	%
Power Output, 1 dB Compression Point, CW ⁽¹⁾ ($V_{DD} = 26\text{ Vdc}$, $I_{DQ} = 700\text{ mA}$, $f_1 = 960\text{ MHz}$)	P_{1dB}	—	105	—	W

1. These values are derived from a 960 MHz optimized test fixture. Values are not applicable to Figures 1 and 2.



B1, B2, B3	Short Ferrite Beads, Surface Mount	Z6	0.076" x 0.220" Microstrip
C1, C9, C15, C16	47 pF Chip Capacitors, ATC	Z7	0.261" x 0.220" Microstrip
C3	5.6 pF Chip Capacitor, ATC	Z8	0.220" x 0.630" x 0.200" Taper
C4, C13	0.8 - 8.0 Variable Capacitors, Gigatrim	Z9	0.240" x 0.630" Microstrip
C5, C6, C12	8.2 pF Chip Capacitors, ATC	Z10	0.060" x 0.630" Microstrip
C7, C17, C18, C19	10 μ F, 35 V Tantalum Surface Mount Capacitors, Kemet	Z11	0.067" x 0.630" Microstrip
C8	20 K pF Chip Capacitor, ATC	Z12	0.233" x 0.630" Microstrip
C10, C11	16 pF Chip Capacitors, ATC	Z13	0.630" x 0.220" x 0.200" Taper
C14	0.6 - 4.5 Variable Capacitor, Gigatrim	Z14	0.200" x 0.220" Microstrip
L1	7.15 nH Inductor, Coilcraft	Z15	0.055" x 0.220" Microstrip
L2	17.5 nH Inductor, Coilcraft	Z16	0.088" x 0.220" Microstrip
N1, N2	N-Type Panel Mount, Stripline, M/A-Com	Z17	0.226" x 0.220" Microstrip
WB1, WB2	5 Mil BeCu Shim (0.225 x 0.525)	Z18	0.868" x 0.080" Microstrip
Z1	0.219" x 0.080" Microstrip	Z19	0.129" x 0.080" Microstrip
Z2	0.150" x 0.080" Microstrip	Z20	0.223" x 0.080" Microstrip
Z3	0.851" x 0.080" Microstrip	PCB	Arlon GX-0300-55-22, 30 mils
Z4	0.125" x 0.220" Microstrip		$\epsilon_r = 2.55$
Z5	0.123" x 0.220" Microstrip		

Figure 1. 865-895 MHz Broadband Test Circuit Schematic



Freescall has begun the transition of marking Printed Circuit Boards (PCBs) with the Freescall Semiconductor signature/logo. PCBs may have either Motorola or Freescall markings during the transition period. These changes will have no impact on form, fit or function of the current product.

Figure 2. 865-895 MHz Broadband Test Circuit Component Layout

TYPICAL CHARACTERISTICS

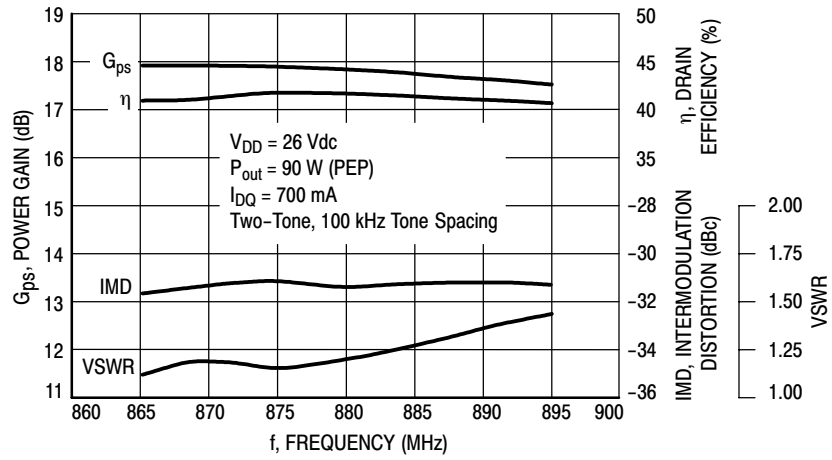


Figure 3. Class AB Broadband Circuit Performance

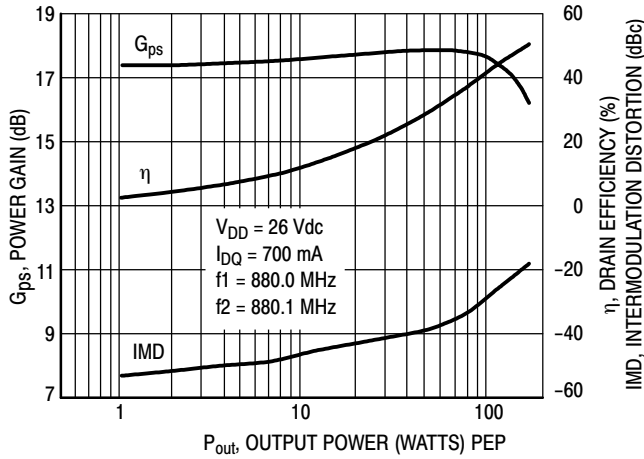


Figure 4. Power Gain, Efficiency, IMD versus Output Power

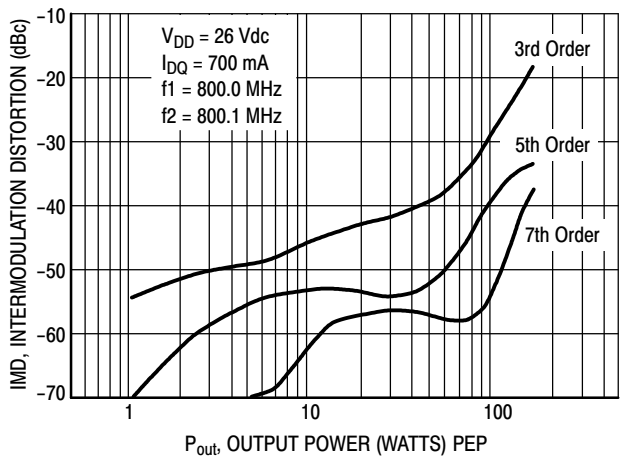


Figure 5. Intermodulation Distortion Products versus Output Power

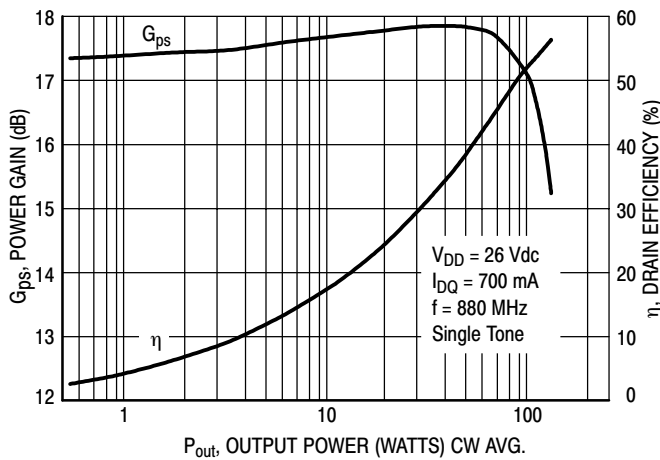


Figure 6. Power Gain, Efficiency versus Output Power

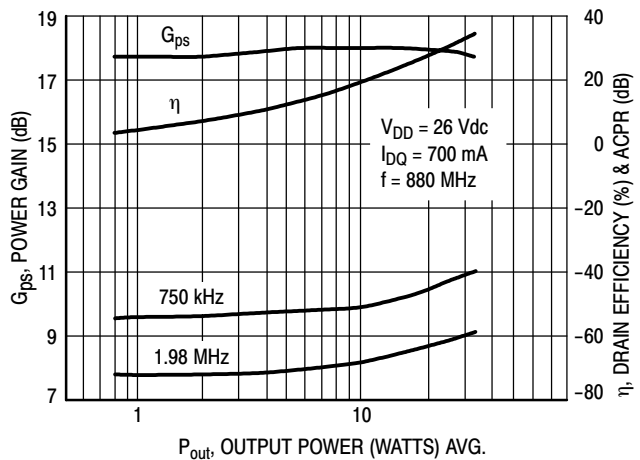
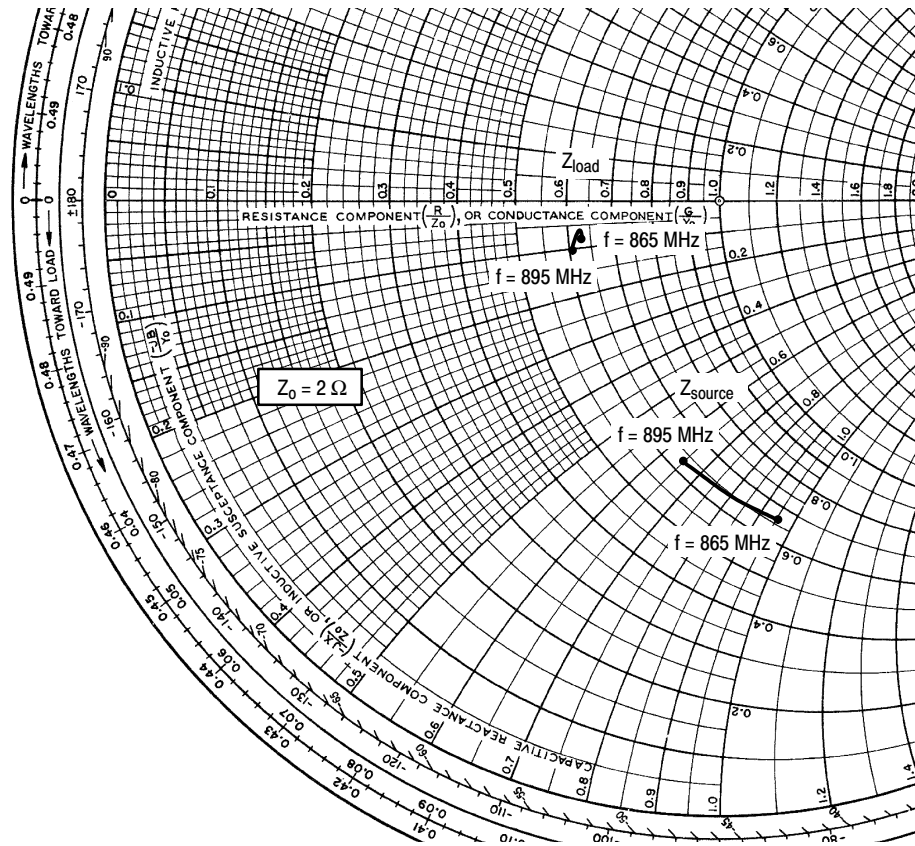


Figure 7. Power Gain, Efficiency, ACPR versus Output Power



$V_{DD} = 26\text{ V}$, $I_{DQ} = 700\text{ mA}$, $P_{out} = 90\text{ W PEP}$

f MHz	Z_{source} Ω	Z_{load} Ω
865	$1.35 - j1.92$	$1.26 - j0.15$
880	$1.33 - j1.66$	$1.26 - j0.10$
895	$1.28 - j1.30$	$1.21 - j0.20$

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

Note: Z_{load} was chosen based on tradeoffs between gain, output power, drain efficiency and intermodulation distortion.

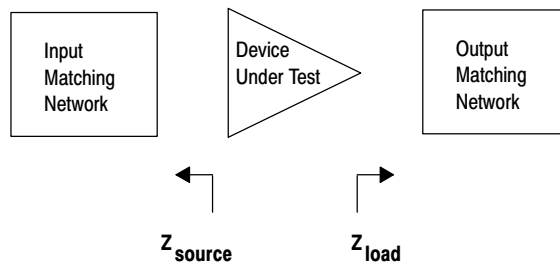
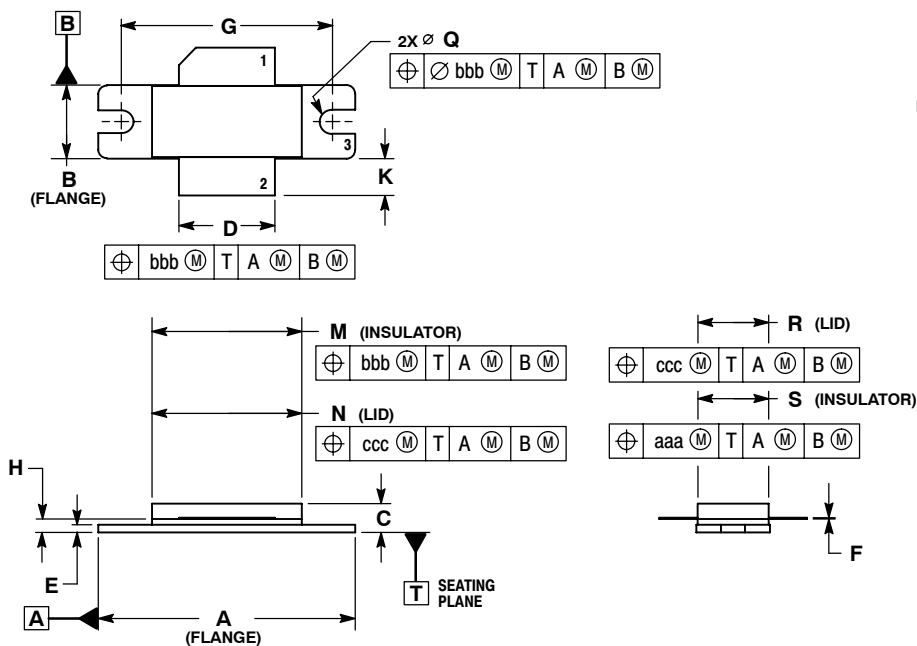


Figure 8. Series Equivalent Source and Load Impedance

PACKAGE DIMENSIONS



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.
 2. CONTROLLING DIMENSION: INCH.
 3. DELETED
 4. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.335	1.345	33.91	34.16
B	0.380	0.390	9.65	9.91
C	0.125	0.170	3.18	4.32
D	0.495	0.505	12.57	12.83
E	0.035	0.045	0.89	1.14
F	0.003	0.006	0.08	0.15
G	1.100 BSC		27.94 BSC	
H	0.057	0.067	1.45	1.70
K	0.170	0.210	4.32	5.33
M	0.774	0.786	19.66	19.96
N	0.772	0.788	19.60	20.00
Q	\varnothing .118	\varnothing .138	\varnothing 3.00	\varnothing 3.51
R	0.365	0.375	9.27	9.53
S	0.365	0.375	9.27	9.52
aaa	0.005 REF		0.127 REF	
bbb	0.010 REF		0.254 REF	
ccc	0.015 REF		0.381 REF	

- STYLE 1:
 PIN 1. DRAIN
 2. GATE
 3. SOURCE

**CASE 465-06
 ISSUE G
 NI-780
 MRF9085LR3**

PRODUCT DOCUMENTATION

Refer to the following documents to aid your design process.

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
13	Sept. 2008	<ul style="list-style-type: none">• Data sheet revised to reflect part status change, p. 1, 2, including use of applicable overlay.• Added Product Documentation and Revision History, p. 9

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