Solder Reflow Attach Method for High Power RF Devices in Air Cavity Packages

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INTRODUCTION

The purpose of this application note is to provide Freescale Semiconductor customers with a guideline for solder reflow mounting of high power RF transistors and integrated circuits in Air Cavity Packages (ACP). This document will aid customers in developing an assembly process suitable for their design as well as their manufacturing operation. Each Power Amplifier (PA) design has its own unique performance requirements. Similarly, each manufacturing operation also has its own process capabilities. Therefore, each design and assembly may require some fine-tuning. The intent of this application note is to provide the information our customers need to establish the process that is most suitable for their design and compatible with their manufacturing operations.

When designing and manufacturing PA systems, electrical performance, thermal performance, quality, and reliability factors must be considered. Using the guidelines presented here, customers should be able to develop a manufacturable assembly process that can do the following:

- Create an interface that is thermally and electrically much more conductive than thermal grease between the device source contact and system ground.
- Provide a thermal ground that will conduct the dissipated heat efficiently from the high power RF device to the system sink.
- Develop a consistent electrical ground to provide a stable RF performance over the life of the PA.
- Obtain a high quality solder joint between the device leads and the solder pads on the Printed Circuit Board (PCB) as well as between the heat spreader of the device and the carrier to ensure good field reliability.
- Maintain the package integrity during assembly as well as in field use.

TERMINOLOGY DEFINITIONS

Throughout this application note, certain terminology is used. Following are definitions of some of these terms.

- Air Cavity Package (ACP) — A package that has the RF devices including the matching components located in the package cavity and surrounded by air as a dielectric medium.
- Base Transceiver Station (BTS) — A system making cellular communication possible in a given cell or other similar communication equipment.
- Carrier — Can either be pallet or coin. This metal piece forms part of the thermal and electrical connection. The carrier is attached to the PCB ground plane as well as to source contact of the RF PA device.
- Coin — A carrier that is smaller than the PCB.
- Flange — The exposed metal at the bottom of the package. The die is attached to the top of the flange, and the exposed bottom surface is designed for attaching to the carrier.
- Heatsink — The carrier is typically bolted to a finned heatsink. The heatsink forms the part of the thermal path that carries heat away from the device to the cooling air.
- Integrated Metal Carrier (IMC) or Pallet — A metal carrier that is bonded to the PCB. Typically pallet is either the same size or slightly larger than the PCB.
- Over-Molded Plastic (OMP) packages — Also referred to as the package. The package that encapsulates the die consists of mold compound, wire bonds, leads and the heats spreader.
- Power Amplifier (PA) — An electronic assembly module that takes in the input signal, amplifies the signal, and feeds it to the antenna.
- Power Device — An RF power device, usually a Si-based LDMOS discrete device, a multi-stage IC device, or a GaAs or GaN device.
- Printed Circuit Board (PCB) — The electrical interconnection between the RF power devices and other electrical components that are part of a PA.

BACKGROUND

Semiconductor devices were first manufactured using metal-ceramic headers in hermetic, metal-can packages. AC packages have evolved from metal and ceramic hermetic packages and have been used in high power RF applications for over two decades. These packages have been a standard for RF power devices with over a 1000 watts power output and a frequency range up to 3.8 GHz. Freescale offers LDMOS power transistors as well as RFIC devices that can be assembled into a PA using the following assembly methods:

- Bolt down or clamping of a high power RF device
- Solder reflow of a high power RF device in the cavity
- Surface mounting of a high power RF device

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This document focuses on the process of soldering AC packages. Until the early 1990s, the industry trend was to bolt down RF power devices into the heatsink. In the mid-1990s, high power RF devices that could be soldered instead of bolted down were introduced by Freescale as the performance and power of these devices started to increase. Soldering power devices offers many advantages:

- The soldered interface provides lower thermal resistance (between 0.1 to 0.2 °C-in^2/W) as well as electrical grounding. This means that the high power devices have lower junction temperature and better RF performance when mounted in a PA with a soldered interface.
- The reduction in junction temperature for all semiconductor devices results in an increase in the device's Mean-Time-To-Failure (MTTF). For Si-based devices, each 15°C to 20°C reduction in junction temperature typically results in a doubling of the MTTF.
- Solder reflow mounting of the RF power device can be integrated with the reflow of the remainder of the components of the PA thus permitting automation and elimination special processes.

This application note focuses on the solder reflow assembly method in which the device flange or source contact is soldered to a metal carrier and the leads are soldered to pads on the PCB simultaneously. This assembly method is a slight modification from industry-standard surface mount assembly technology. In surface mount technology (SMT), the device leads are formed to provide all of the solder joints on the top surface of the PCB. In the solder reflow assembly process, the solder joint for the flange or source contact is in a lower cavity, and the solder joint for the leads are on the top surface of the PCB. Figure 1 shows a typical device dropped through the opening in the PCB. The leads are soldered to the PCB, and the flange or the source contact or the heat spreader is soldered to a metal carrier. These devices are available in a variety of lead sizes, lead pitch, and number of leads.

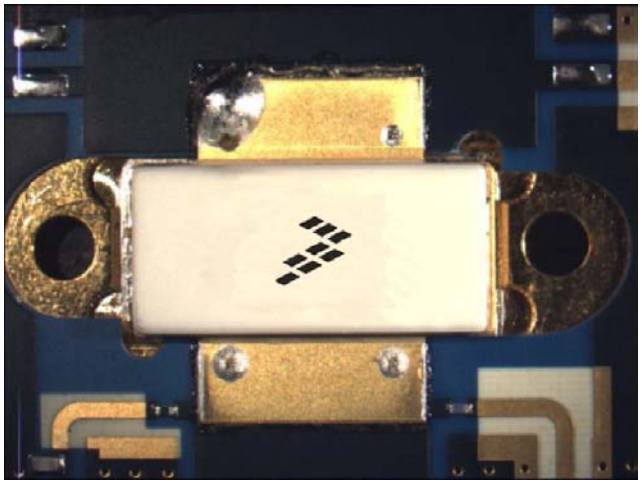


Figure 1. Typical Application of Freescale RF Power Device in Air Cavity Ceramic Package Soldered to a PCB as Well as to Carrier

The AC package is designed for an RF power die using silicon (LDMOS), GaAs or GaN technologies. In most applications, the package will also hold MOSCAP or passive components that are part of the device matching network. A typical air cavity package consists of a gold-plated lead frame, a gold plated metal flange, a ceramic lid, a ceramic window frame, and sealing epoxy between the lid and the window frame. Figure 2 shows a typical ACP construction.

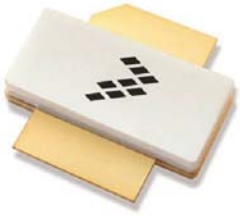


Figure 2. Typical RF Air Cavity Ceramic Package Device Compatible for Solder Reflow Process (Case 465A, NI-780S)

Commonly used AC packages for RF power devices designed for the solder reflow assembly method include the NI-400S (Case 465F), NI-400S-240 (Case 465J), NI-780S (Case 465A and Case 465H), NI-880S (Case 465C), and NI-1230S (Case 375E). Other AC packages such as NI-780 (Case 465) are designed for bolt down and they are designated without suffix "S". This style of packages can also be assembled using the solder reflow assembly method. All electrical contact surfaces of AC packages are solderable, with gold plating on the external surface. For packages that are designed for bolt down but are assembled using a solder reflow process, it is recommended that bolts are not used in addition to the solder joints to attach the flange to the carrier.

PACKAGE CONSTRUCTION

As mentioned earlier, RF power devices are manufactured in both AC and Over-Molded Plastic (OMP) packages. Figure 3 shows the schematic representing a typical cross-section of an AC package.

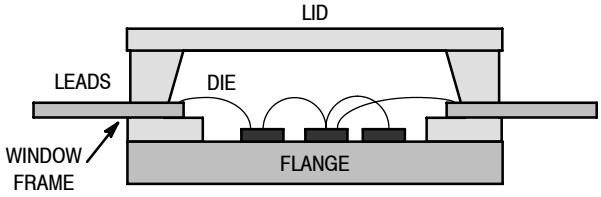


Figure 3. Air Cavity Package Construction for Power Devices

In an AC package, the Si die is typically attached to a Au plated flange or heat spreader made from Cu based laminate or similar material using high conductivity die attach. The lowest resistance die attach used in the semiconductor industry is Au-Si eutectic die attach. The die and wire bonds are surrounded by air and protected from the environment by a lid. The leads and flange are separated by a window frame that forms the cavity for the die and wire bonds. The leads and the flange are typically plated with Au to protect the underlying solderable surface.

Both AC and OMP packages are RoHS (Restriction of Hazardous Substances) compliant. Both are non-hermetic packages. The key differences between the two package technologies are as follows.

- In AC packages, the Si die is typically attached to a metal heat spreader using a Au–Si–based eutectic die attach. In OMP packages, the Si die is typically attached to a Cu alloy heat spreader using high Pb–based soft solder.
- In AC packages, the die and wire bonds are surrounded by a low die–electric constant material such as air (hence, the name Air Cavity). In OMP packages, the die and wire bonds are in direct contact with a higher die–electric constant mold compound.

CARRIER DESIGN CONSIDERATIONS

Figure 4 shows an example of a test board in which the PCB is bonded to a carrier with a cavity. In this particular case, the carrier is the same size as the PCB and is bonded to the PCB underside with an electrically conductive bond layer. The carrier is an integral part of the system and has thermal and electrical functions. RF power devices dissipate thermal energy that must be removed from the device through the back–side of the device. The carrier is an important part of the thermal structure because it spreads the heat to a larger area while dissipating it to the ultimate sink. Also, the carrier provides an electrical ground connection for the device. The PCB shown in Figure 4 is a test circuit, not a power amplifier. The test circuit is designed to accommodate both bolt down and solder reflow devices.

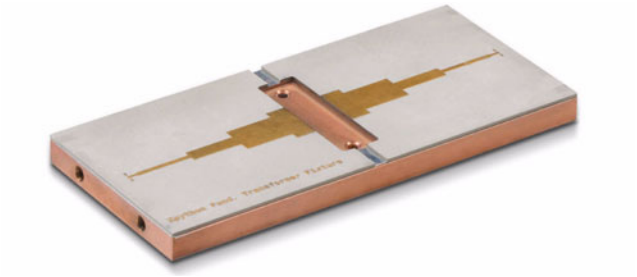


Figure 4. Example of Test PCB Bonded to Carrier with Cavity to Accommodate RF Power Device

Two types of special PCB carriers are more commonly used to dissipate heat from the power devices: the integrated metal carrier (IMC) pallet and the coin.

In one type of PCB assembly, the conventional PCB is attached to a carrier that is the same size or slightly larger than the PCB similar to the test circuit shown in Figure 4. This is known as an Integrated Metal Carrier (IMC) or pallet. The metal carrier is made from mostly copper or aluminum material which provides high thermal and electrical conductivity. The metal is plated to provide a solderable surface. A copper pallet is typically plated with electroless Ni followed by immersion Au. The Au thickness is fairly small and is commonly known as Au flash. The aluminum material is typically plated by a zincation process, followed by Ni and Au flash layer or Ag layer. The purpose of the noble metal layer such as the Au flash layer is to prevent the Ni from oxidizing and to keep it solderable. In addition to the plating layers mentioned previously, other plating materials used in the industry are also available. Vendors familiar with plating technology can provide alternatives and a cost benefit analysis of the plating schemes. The carrier in Figure 4 is unplated copper. Note that this is only a test piece designed for Freescale's internal testing. It is not recommended that bare or unplated copper carrier be used for systems that are put for long term use in the field under various atmospheric conditions. Unplated copper is prone to oxidation and corrosion. Similarly, Al is not a solderable material and it will require application of solderable material such as Ni followed by a noble metal.

The second type of PCB assembly has a carrier of forged or machined metal coin that is also plated with Ni and Au. The coin is usually designed to be larger than the RF power device but typically much smaller than the PCB. The coin should have sufficient perimeter area so it can be bonded to the ground plane of the PCB. Typically, the coin also has a bolt hole on each side of the RF power device so it can be bolted directly to the PA module or a finned heatsink to provide good thermal and electrical grounding for the coin. Figure 5 below shows a picture of the backside of the PCB with coin attached to it.

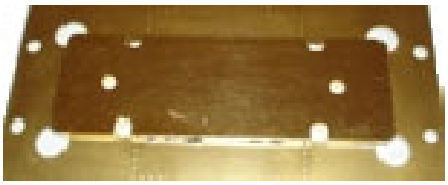


Figure 5. Typical PCB with Coin Attached to the Backside

In recent years, some proprietary coin technologies have been developed where a copper coin is integrated into the PCB assembly and therefore has no protrusion on the back side of the PCB as the conventional coin shown in Figure 5. The coin is essentially coplanar with the back surface of the PCB. Such coins will likely reduce the system cost by eliminating a need for machining a pocket in the heatsink to accommodate a coin. Such coins also increase the complexity of the PCB manufacturing.

The choice between various coin technologies or pallet is purely driven by cost. Typically, if the total footprint area of the RF power devices is a significant portion of the PCB area, the pallet is more cost–effective. If the total footprint area of the RF power devices is not a significant portion of the PCB area and if the coin size can be standardized, the coin is a cost–effective solution. In general pallet adds significantly higher thermal mass than coin putting additional requirements on the solder reflow process, particularly for higher temperature required for Pb–free solder alloys.

GEOMETRICAL DESIGN OF THE CARRIER

In a thermal pathway, the carrier (pallet or coin) is inserted between the RF power device and the aluminum heatsink for thermal management as shown in Figure 6. A properly designed carrier can significantly improve the thermal performance of the system. Normally, the carrier is made of metals with high thermal conductivity such as copper alloys — C101, C102, C151 or aluminum.

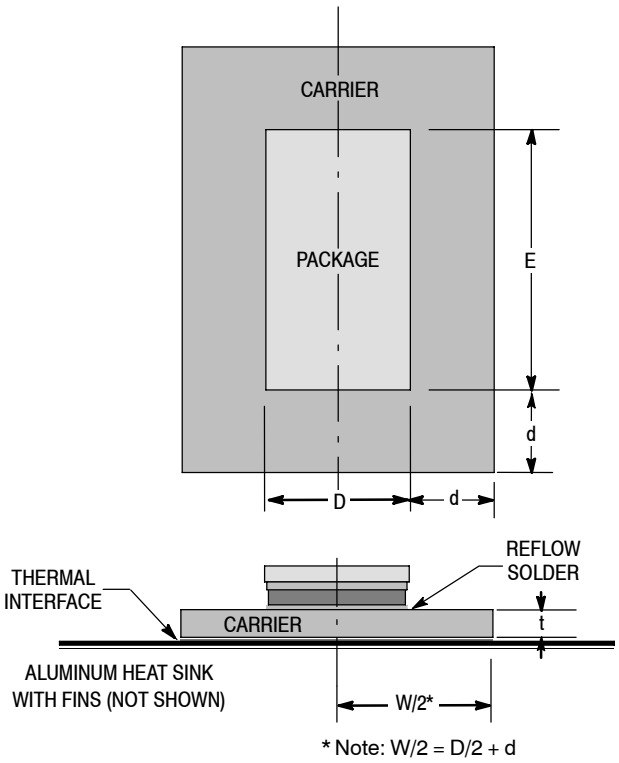


Figure 6. Typical Carrier Inserted between Device and Aluminum Heat Sink

With a metal carrier, two important dimensions affect thermal performance of the system: (a) thickness "t," and (b) extension "d" (shown in Figure 6). A parametric study was conducted using Finite Element Analysis (FEA) for various values of "t" and "d". A typical 600 watt P_{out} RF power device MRF6VP2600H, in the NI-1230HS package (Case 375E) was used as the vehicle for this simulation. In the simulation, the thickness value was varied between 0.125 mm to 5.0 mm, and the extension "d" was varied between 0.0 mm to 12.0 mm. The package footprint is approximately 10 mm by 34 mm.

The evaluation was carried out for two different materials: copper (C102 alloy, conductivity 390 W/m-K) and wrought aluminum (conductivity 206 W/m-K). The evaluation results in terms of normalized junction to heatsink thermal resistance with a copper carrier are shown in Figure 7. Similar results for an aluminum carrier are shown in Figure 8. In both cases, the thermal resistance between junction to heatsink is normalized by the value of the thermal resistance between junction and heatsink with no carrier ("t" = 0.0 mm). The normalized thermal resistance between junction to sink is plotted versus carrier extension "d" for different thicknesses of copper (Figure 7) and aluminum (Figure 8) material. These figures are a guide for designing an effective carrier to reduce the total thermal resistance. A more detailed analysis for each specific design is highly recommended.

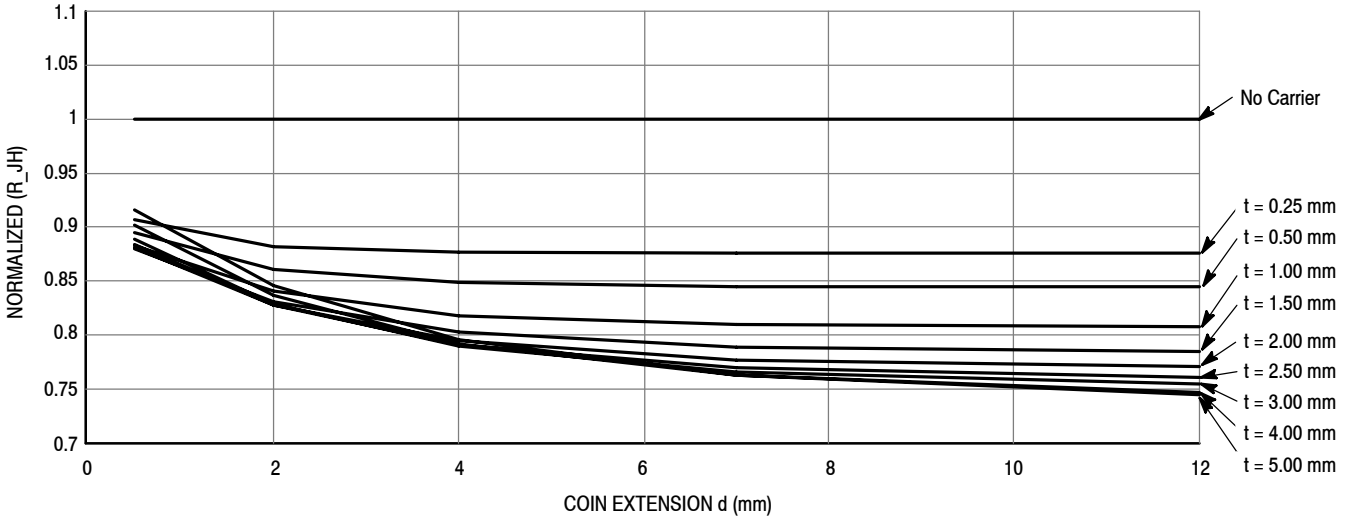


Figure 7. Normalized Thermal Resistance Results for Copper Carrier

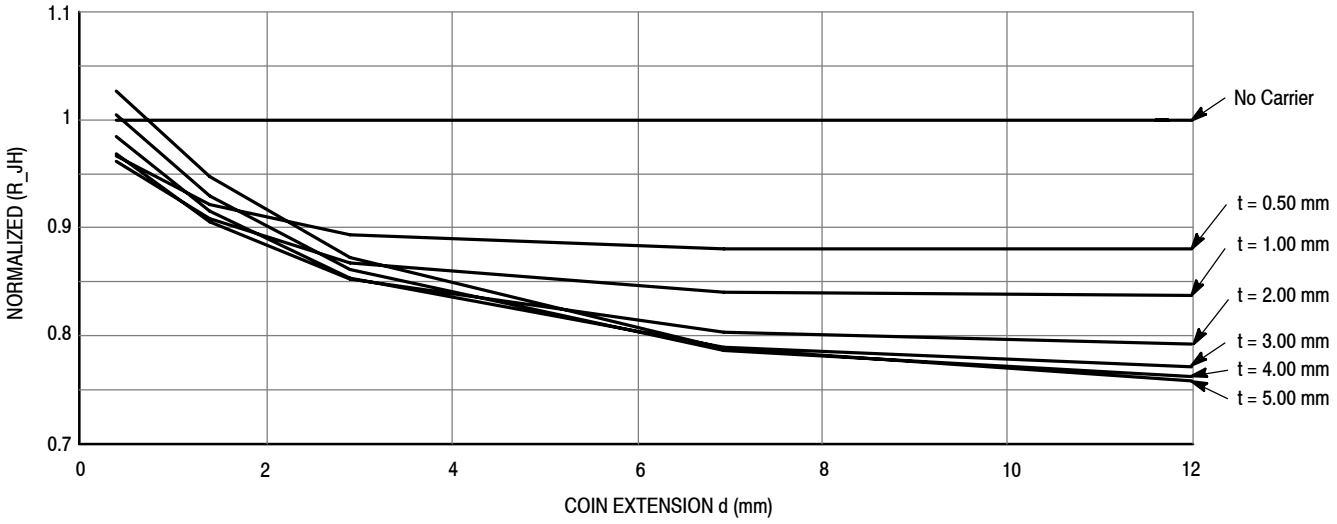


Figure 8. Normalized Thermal Resistance Results for Aluminum Carrier

From the analysis results presented here, we can state the following:

- A copper carrier is more efficient in reducing the total thermal resistance between junction and sink. Aluminum carriers provide slightly less (~15%) reduction in total system thermal resistance than copper carriers.
- For both copper and aluminum carriers, thickness "t" is recommended to be 3.0 mm minimum. As Figures 7 and 8 illustrate, the additional benefit in terms of thermal performance improvement becomes insignificant when the thickness of the carrier is increased above 3.0 mm for either copper or aluminum. For large PCB and carrier, higher thickness may be necessary to prevent warping of the PCB and the carrier.
- The extension "d" of the carrier past the device width is recommended to be 5.5 mm minimum for both copper and aluminum. Increasing the size of the carrier on each side of the device greater than 5.5 mm shows only slight improvement.

Based on this analysis, we recommend using a copper carrier that is 3.0 mm thick and a minimum 5.5 mm wider than the package footprint on all sides. Mechanical considerations, such as sufficient bond line width, warpage etc., should also be included in the design of the carrier.

Besides the footprint of the carrier, the next most important dimension is the cavity depth or pedestal height. If the PCB thickness is less than the seating plane height of the RF power device, the bottom surface of the RF power device will be seated below the backside of the PCB. In such instances, the carrier must have a cavity that accommodates the protruding portion of the RF power device. If the PCB thickness is larger than the device seating plane height, the carrier must have a pedestal that connects to the bottom of the RF power device. In either instance, multiple components are combined to form an assembly so the stack-up tolerance becomes a serious concern, particularly when the assembly method is not a manual process such as bolt down or clamp down and soldered leads.

A simple analysis to determine the cavity depth is to use the worst-case tolerance analysis and determine the optimum cavity depth. This approach assumes that all worst case dimensions will occur simultaneously and frequently. The probability of all the extreme dimensions occurring concurrently is almost nonexistant. In addition, this approach is not very practical because it will result in the dimension of cavity depth with a much larger range than normally necessary.

A better approach is to determine the standard deviation of the protrusion using the square root of sum of the square method. This method gives a somewhat more realistic combination of dimensional tolerances. In performing this analysis, it is ideal to know the mean and standard deviation of the distribution of the critical dimensions, e.g., PCB thickness. If the actual distribution is not known, it is assumed that the dimension follows a normal distribution whose mean is at the nominal dimension and the tolerance band represents $\pm 3\sigma$ (sigma) variation. The assumption that the tolerance band is six times the standard deviation is conservative, because it does not account for process shift. In real life, the tolerance band for a process is defined by process shift plus the standard deviation of the distribution. In order to have a good yield (>95%), the processes are controlled to provide a standard deviation, which is significantly less than one-third of the required tolerance. For example, if a given component dimension is specified as 0.1″ (2.54 mm) ±0.003″ (0.076 mm), we will assume that the dimension is normally distributed with the mean at a nominal value of 0.1″ (2.54 mm) and a standard deviation of 0.001″ (0.025 mm). This method is illustrated in Figure 9 and Tables 1 and 2.

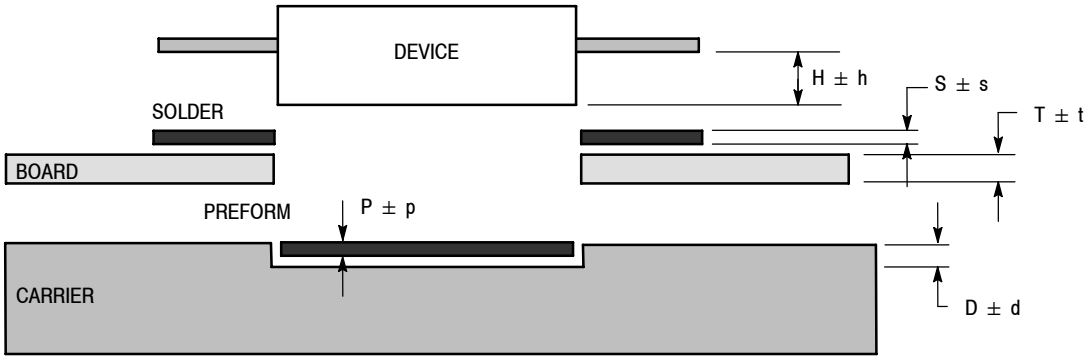


Figure 9. Exploded View Showing Criteria and Tolerances for Calculating Cavity Dimensions

Figure 9 shows that the cavity depth "D" for a complete balanced system should be equal to device protrusion (T + S – H – P). This is possible if the assemblies are made one at a time and the cavity depth is customized for each assembly. For mass production, the distribution of "D" should overlap the distribution of (T + S – H – P). In the method here, a device in NI–780S (Case 465A) has been selected as an example. The nominal dimensions and tolerances are listed for key components.

Table 1. Dimensional Tolerances for Key Component Dimensions

Components	Dimension	Nominal	± Tolerance	Nominal	± Tolerance
		inch	inch	mm	mm
PCB	T	0.032	0.003	0.813	0.076
Solder Joint (leads)	S	0.003	0.001	0.076	0.025
RF Device	H	0.062	0.005	1.575	0.127
Solder Preform	P	0.006	0.001	0.152	0.025
Cavity Depth	D	?	0.001	?	0.025

A good way to perform this analysis is to create a spreadsheet in which different options can be evaluated. Table 2 is an example of a spreadsheet in which the dimensions in inches are taken from Table 1. In this example, the bond line thickness between the backside of the PCB and the carrier is assumed to be negligible. If it is a significant part of the stack–up, it can be added to the evaluation.

Table 2. Evaluation of Cavity Depth "H"

Components	Dimension	Nominal	± Tolerance	Minimum	Maximum	Std. Dev.
		inch	inch	inch	inch	inch
PCB	T	0.032	0.003	0.029	0.035	0.001
Solder Joint (leads)	S	0.003	0.001	0.002	0.004	0.000
RF Device	H	0.062	0.005	0.057	0.067	0.002
Solder Preform	P	0.006	0.001	0.005	0.007	0.000
Cavity Depth	D	???	0.001			
Protrusion (T+S-H-P)						
Worst Case		-0.033		-0.023	-0.043	
SRSS (3*σ)		-0.033		-0.027	-0.039	0.002
SRSS (2*σ)		-0.033		-0.029	-0.037	0.002
Cavity Depth Options (H)						
		0.027	0.001	0.026	0.028	
		0.029	0.001	0.028	0.030	
		0.031	0.001	0.030	0.032	
		0.033	0.001	0.032	0.034	
		0.035	0.001	0.034	0.036	
		0.037	0.001	0.036	0.038	
		0.039	0.001	0.038	0.040	

From the example in Table 2, we can state that the device bottom will protrude below the backside of the PCB an average of 0.033″ (0.84 mm). The standard deviation for the distribution of the protrusion is 0.002″ (0.051 mm). If we use a ±3σ spread, which will cover 99.7% of the population, the device will protrude anywhere between 0.027″ (0.69 mm) to 0.039″ (0.99 mm). If we use a ±2σ spread, which will cover 95.4% of the population, the device will protrude anywhere between 0.029″ (0.74 mm) to 0.037″ (0.94 mm).

It is assumed that the machining tolerance for the cavity depth is ±0.001″ (0.025 mm). If the cavity depth is specified at 0.029″ (0.74 mm), the carrier will be produced with a cavity depth between 0.028″ (0.71 mm) and 0.030″ (0.76 mm). Under these circumstances, a large number of assemblies will protrude much more than the cavity depth, resulting in solder flow out and a potential issue of solder bridging between the source contact and gate or drain side leads as well as potential open solder joints at the gate and drain lead. On the other end, if the cavity depth is specified as 0.037″ (0.94 mm), a large number of assemblies will have no contact between the bottom of the device and the solder preform, leaving either a void or no solder wetting. Our tolerance analysis reveals an obvious fact — the stack-up tolerances are being dominated by one or two components. In this example, the tolerance in the device seating plane height is dominating the stack-up analysis.

For this example, it is recommended that a cavity depth specification of 0.033″ ±0.001″ (0.84 mm ±0.025 mm) be selected. In this case, the cavity distribution and the protrusion distribution overlap each other. In the worst case, the cavity depth would still be too deep for the device to make contact with the solder preform. In the best case, the cavity depth would be close to nominal device protrusion. In the event that the PCB distribution is running toward the high end of the range, the variation can be adjusted by using two preforms or thicker preform instead one without changing the cavity dimensions. That kind of change can be accommodated by reprogramming the pick-and-place equipment rather than changing the hardware. The value recommended here is only as guidance. Another alternative is to design the cavity for the minimum protrusion of 0.029″ (0.74 mm) and use a fixture to press the leads into the solder paste. The main purpose of this discussion is to demonstrate methodology. Each operation and each assembly is different and it is strongly recommended that the customer examine this in detail with their process engineers and experiment with different thickness before settling on the final dimension.

The purpose of the discussion about selecting the cavity depth dimension is to highlight the importance of this dimension on the quality of the solder joint at the flange as well as leads which, in turn, impacts the device performance. A cavity that is too deep will result in potential voiding in the solder joint at the source contact. A cavity that is too shallow will result in solder flowing out and creating solder bridging at the flange joint and open joints at the PCB solder joint. The customer is advised to examine their assemblies very carefully in determining the cavity depth or pedestal height dimension specification. Some times, particularly for thick PCB, which tends to have higher thickness tolerances, it may become necessary to use a small fixture that keeps the device weighted down and maintain a positive contact both at the bottom of the cavity as well as on the top of the PCB to assure good solder joints at all contacts.

PC BOARD LAYOUT CONSIDERATION

For the soldered-down RF power device, the leads must be soldered on the top surface of the PCB, and the flange must be soldered to the carrier. This requires a slot, or opening, in the PCB through which the RF power device protrudes. The case outline drawing shows the length and width dimensions at the bottom surface of the flange. The minimum dimensions (nominal minus milling or punching tolerance for the PCB) for the slot should be at least 0.002″ (0.05 mm) in the shorter dimension and 0.003″ (0.076 mm) in the longer dimension larger than the maximum dimension of the package to allow easy insertion of the device into PCB opening.

For example, Case 465A (NI-780S) shows dimension “A” as the length of the package. The maximum value is 0.815″ (20.70 mm). Therefore the minimum cavity length or PCB slot should be 0.003″ (0.076 mm) longer or 0.818″ (20.78 mm). The width of the package is defined by two dimensions and their interaction. Dimension “B” is the width of the flange and dimension “S” is the dimension of the insulator, or the “window frame”. Both of these components fit into the PCB slot. For this package, the maximum value of dimension “B” is 0.390″ (9.91 mm). The maximum value of dimension “S” is 0.375″ (9.52 mm). Even when the positional tolerance “aaa” between the window frame and the flange is applied, the governing dimension will be the maximum width of the package, which is 0.390″ (9.91 mm). Therefore the minimum recommended slot width is 0.392″ (9.96 mm).

Normally, there is a corner radius in the slot based on the mill or router diameter. This radius value should also be considered when defining the size of the slot. The length dimension of the slot can be enlarged so that the corner radius will clear the body of the RF device. In general, for RF performance and for consistency, the slot width should not be much larger than the package body. In addition, there will be a corner radius at the bottom of the cavity in the carrier. This radius between the bottom of the cavity and the vertical wall is usually not very large and should not affect the slot dimension. It is important that this corner radius is considered in determining the slot dimension. If the corner radius is too large, it may require opening the cavity size but not increasing the PCB slot dimension due to RF performance considerations. Case outline drawings are available in the data sheet for each device.

The top surface of the PCB has solder pad areas for soldering the leads to the traces on the PCB. It is good manufacturing practice to pull back these metal traces from the edge of the slot. PCB manufacturers would provide a design rule on how far these metal traces should be pulled back. In the absence of a PCB design rule, Freescale recommends that the metal in the solder pad area should be at least 0.010″ or 0.25 mm from the edge of the slot. The outside edge of the solder pad should be longer than the outside tip of the leads by a minimum of 0.010″ (0.25 mm). Similarly, the design rules from the PCB supplier and the assembly process should be followed on the width direction in terms of how close the two adjacent pads of metal should be to define the pad width. In the absence of a PCB design rule from the assembly process and PCB manufacturer, it is recommended that the metal in the solder pad area should be at least 0.010″ (0.25 mm) wider than the lead width.

Another concern is the opening in the solder mask. The industry has two common practices of either using a solder

mask defined pad or using a copper defined pad. In the solder mask defined pad, the solder mask overlaps the underlying metal pad, which is slightly larger than the solder mask opening. In the copper defined pad, the solder mask opening is slightly larger than the exposed metal pad. The type of solder mask opening used is entirely based on the PCB supplier's preference and the preference of the PA board assembly operation. In either case, it is recommended that the design rules from the PCB suppliers as well as the assembly process should be followed for the solder mask opening. The dimensions given here are for the solderable portion of the PCB trace. Typically, the difference between a solder mask opening and a copper pad is 0.003″ (0.076 mm) per side. For example, for the NI-780S (Case 465A) package, the gate lead is 0.500″ (12.7 mm) wide. Thus, the solderable trace at the gate lead should be at nominal 0.520″ (13.21 mm) wide. If the customer's PCB is using a copper defined trace, then the PCB should have a dimension of 0.526″ (13.36 mm) in the solder mask around the trace. If the customer is using the solder mask defined pads for the PCB, the opening in the solder mask will be 0.520″ (13.21 mm) and the copper trace will be 0.526″ (13.36 mm).

Even if the metal trace on the PCB extends well beyond the dimensions shown above, it is recommended that the rest of the trace be covered with solder mask or a solder mask is used to define the solderable area for the lead. This prevents the solder running away from the lead and wetting the remaining trace rather than soldering the lead.

In general, the PCB trace dimensions for RF devices are governed more by the matching circuit consideration than anything else. The recommendations given here are based purely on common manufacturing considerations.

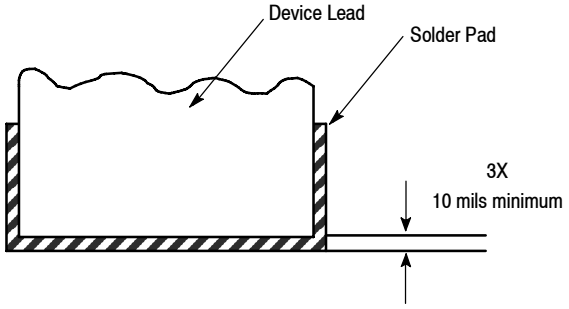


Figure 10. Pad Size for Gate and Drain Side Leads

The recommended solder pad dimensions as well as the slot dimensions for the case outlines of various air cavity parts are shown in Appendix A. These dimensions are to be used as a guide and should be validated with the design rules from the PCB supplier as well as the assembly process. In case of conflict, the PCB supplier design rules should supersede the recommendations in Appendix A.

PCB TO CARRIER ATTACH

The coin or the pallet is attached to the underside of the PCB using either a high temperature solder or a conductive adhesive such as Ag-filled epoxy. Freescale Application Note AN1907 for *Solder Reflow Attach Method for High Power RF Devices in Over-Molded Plastic Packages* [1] has extensive details on the most common attach method for PCB to carrier attach. For that reason the details are not repeated here. The user should refer to AN1907 for the PCB to carrier attach. The details are applicable for both AC and OMP packages.

SOLDER MATERIAL

RF devices are soldered to the land areas on the PCB and the carrier in one heating process. Solder is used for the electrical and thermal connection from the device to the carrier. Solder is available in preform and paste form. Freescale recommends solder preforms for the attachment of the device flange to the carrier in the carrier cavity and solder paste for the connections between the device leads and the PCB land area. The paste is made from solder material, binder, solvent and flux. The preforms are pre-cut solder foils typically provided with a coating of flux. The solder paste tends to create more voids in the solder joint than solder preform due to the presence of binders, flux and solvents. For this reason, Freescale recommends using preform at the source contact. That solder joint is part of the prime heat dissipation path and a reduction in void at that joint will result in lowering the total system thermal resistance.

Common solders used in the industry until recently were Sn-Pb alloys. In the last few years, due to RoHS regulation from various government entities, many customers have been switching to Pb-free solder alloys. The most common Pb-free alloy used in such applications is SAC305 (Sn3.0Ag0.5Cu) with a liquidous temperature of 221°C. When reflowed, the solder forms a metallurgical joint with Ni or Cu in the device as well as Ni or Cu from the carrier.

No-clean flux is recommended because it does not require a subsequent aqueous cleaning process. Fluxes that must be cleaned in a subsequent step can leave water residue in the cavity and under the PCB. Because high power RF devices are reflowed on the PCB with all other components, Freescale strongly recommends that the PCB with the RF device in a cavity style package is not washed to remove the flux. It is recommended that solder paste with only no-clean flux be used.

Solder preforms are precut or stamped to precise shapes and delivered in tape and reel for use in a pick-and-place system to populate the PCB. Solder preforms also have some flux coating on it but typically the level of flux in the paste is much higher than in the preform. Solder paste is available in jars and is typically printed in a pattern to coincide with solder land areas on the PCB. The patterning is done using a stainless steel stencil. The stencil is typically laser-cut to precise patterned openings which allow solder paste to pass through and deposit on the PCB in the same shape as the opening. Stencil thickness is defined by the pitch of the component leads. Typically, RF power devices do not have a pitch that is as fine as some digital components on the PCB. A 0.006″ (0.15 mm) thick laser-cut stencil is usually adequate for use in screen-printing solder paste on the PCB. When using solder paste, the binders and solvents evaporate during the reflow, and the finished solder joint is typically 45% to 55% of the printed volume. Solder preforms retain all of their volume during the reflow process.

One of the key concerns for solder joint reliability for AC packages is the presence of Au in solder. Typically AC packages are plated with Au over Ni. The thickness of Au on the flange has been 100 μ-in (2.54 μ-m) minimum and 130 μ-in (3.3 μ-m) typical. In the last few years Freescale has introduced

what is known as Low Au packages (suffix L and H in the device part number) with the Au thickness specification of 40 ± 10 μ-in. (1 ± 0.25 μ-m) for the lead. In 2007, Freescale introduced air cavity packages with minimum Au thickness of 60 μ-in (1.52 μ-m). In 2009, the minimum Au thickness was further reduced to 30 μ-in (0.76 μ-m). For the Au thickness specification for a given outline package, contact a Freescale representative.

The main focus for the solder joint reliability is to limit the presence of Au-Sn intermetallics in the solder joint. In technical publications, the criteria are listed as % of Au in solder by weight. The acceptable % is generally quoted in the range of 4% to 8% by weight. Freescale's own experiments [2] show that there is only marginal difference in solder joint reliability between 3.2% and 10.4% Au in SnAgCu solder. In the graphs below, % of Au in solder for different preform thickness and different paste thickness have been plotted. For leads and flanges at 30 μ-inch (0.76 μ-m) minimum, the maximum Au thickness is expected to be 50 μ-inch (1.27 μ-m). The customer can use the graph in Figure 11 to determine what should be the minimum thickness of the solder preform to be used for soldering the flange. Similarly, Figure 12 can be used to determine what should be the minimum paste thickness for the soldering of the leads. It is believed that a minimum of 4 mil and preferably a 6 mil thickness preform and 5 or 6 mil thick solder paste are adequate to restrict the % of Au in solder and provide sufficient reliability for the solder joint.

Figure 11. Percentage of Au in SnAgCu Solder for Various Thickness of Solder Preform

Figure 12. Percentage of Au in SnAgCu Solder for Various Thickness of Solder Paste

In some applications, customers prefer to use a pre-tinning process to remove all the Au out of the package before soldering. Freescale does not think that pre-tinning is necessary to provide a reliable solder joint. If the customer wants to pretin the device, it is recommended that the device be checked for gross leak hermeticity after pretinning and the device should not be dipped into the solder to the depth that the solder touches the lid sealing epoxy.

PCB ASSEMBLY PROCESS

So far we have described how to design a carrier and its cavity or pedestal to accommodate the difference between the solder joint at the source contact and the solder joint between the gate and drain side leads and the PCB land areas. Guidelines have also been described for the PCB layout, different alternatives for attaching a PCB to a carrier and selection of solder material as well as thickness. The next step is to follow a standard surface mount process to dispense the solder pattern, pick–and–place the devices on a PCB, and reflow the entire assembly in a belt furnace. A typical solder reflow assembly process flow is shown in Figure 13. One key difference for this process from a surface mount assembly process is that the device source contact is soldered to a surface lower than the top of the PCB. Due to the lower surface level as well as the need to reduce void levels in the solder joint at the source contact, it is recommended to use a solder preform instead of solder paste. The preforms are typically precut or stamped to the required size and delivered in tape and reel. They are usually dispensed using pick–and–place equipment just before the RF power device is placed in the PCB slot. Other than that, the process is very similar to the surface mount assembly process that is a very common assembly technique currently used in the electronics industry.

Freescale uses the JEDEC–specified solder profile in qualifying its devices. The JEDEC criterion for Pb–free solder alloy is shown in Table 3. The profile specified in JEDEC specification is defined to specify limits that need to be used to qualify semiconductor devices. It is an example device testing profile, not a specific device assembly profile. Typically, the solder supplier will provide a recommended profile for use with their paste and preforms. A specific profile used for the assembly will depend on the reflow furnace capabilities and the thermal mass going through the furnace. Freescale RF power devices are qualified to survive three reflows that meet the criteria shown in Table 3.

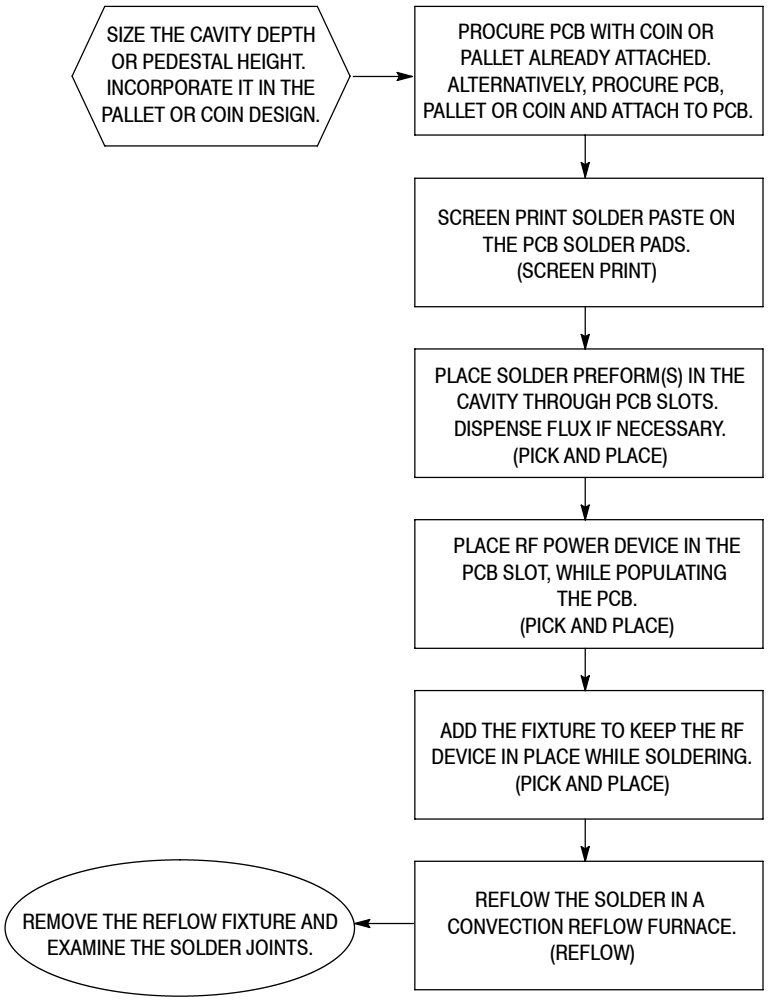


Figure 13. Typical Process Flow for Assembly of PCB using Solder Reflow Method

Table 3. JEDEC J-STD-020D.1 Solder Reflow Profile Requirements

Profile Feature	Pb-free Assembly
Preheat/Soak Temperature Min (T_{smin}) Temperature Max (T_{smax}) Time (t_s) from (T_{smin} to T_{smax})	 150°C 200°C 60-120 seconds
Ramp-up rate (T_L to T_p)	3°C/second max
Liquidous temperature (T_L) Time (t_L) maintained above T_L	217°C 60-150 seconds
Peak package body temperature (T_p)	< 260°C
Time (t_p)* within 5°C of the specified classification temperature (T_c)	 30* seconds
Ramp-down rate (T_p to T_L)	6°C/second max
Time 25°C to peak temperature	

* Tolerance for peak profile temperature (T_p) is defined as a supplier minimum and a user maximum.

For production use, most common reflow ovens are often forced convection or conduction types. In forced convection ovens, the boards with carriers are often put in boats, or holders, and sent on a moving belt though the oven. The convection oven has different zones in which the air or nitrogen-rich gas is heated independently. This results in a controlled profile of specific temperatures that the PCB experiences for specific times. Examples of these profiles are shown in Figures 14 and 15. In a conduction oven, the heat transfer occurs by conducted heat from the platen in the oven to the substrate on which the PCB and carrier sit. The method of heating is therefore not from heated air or gases, but from the direct heat transfer from the bottom of the carriers to the PCB. Instead of a conveyor belt, sweeper mechanisms move the substrate from zone to zone, creating a temperature profile.

Other types of heating, such as IR furnaces or vapor phase reflow, are not appropriate methods for this product. Vacuum furnaces may be used in laboratory situations but are not suitable for production volumes.

In all cases, the profile must be optimized for the specific PCB assemblies based on parameters such as total thermal mass going through the furnace, furnace capabilities, temperature restrictions for key components and size of the PCB. At the beginning of the assembly operation, the system is characterized with dummy units going through the reflow operation. Thermocouples are attached to the dummy units at critical solder joint locations. All thermocouple profiles are monitored to determine optimum process parameters, such as the temperature of each individual zone and the belt speed. Figures 14 and 15 show typical profiles indicating the temperature versus time plot at a given location on the PCBs. It also identifies parameters such as different zones of the furnace, temperature in the zones and the peak reflow temperature, total time, belt speed and time at critical temperature (e.g., time above solder melting temperature).

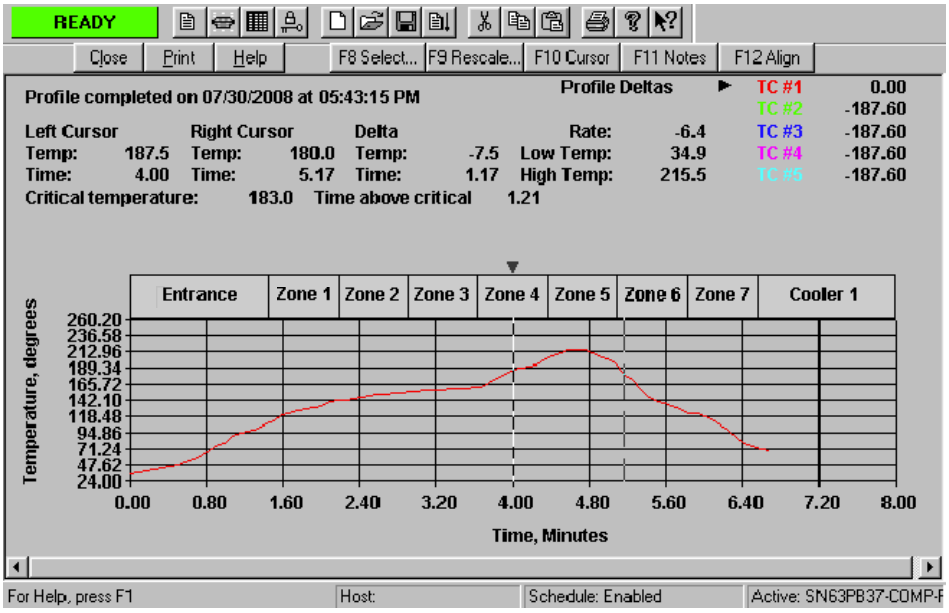


Figure 14. Typical Solder Reflow Profile for Eutectic SnPb Solder

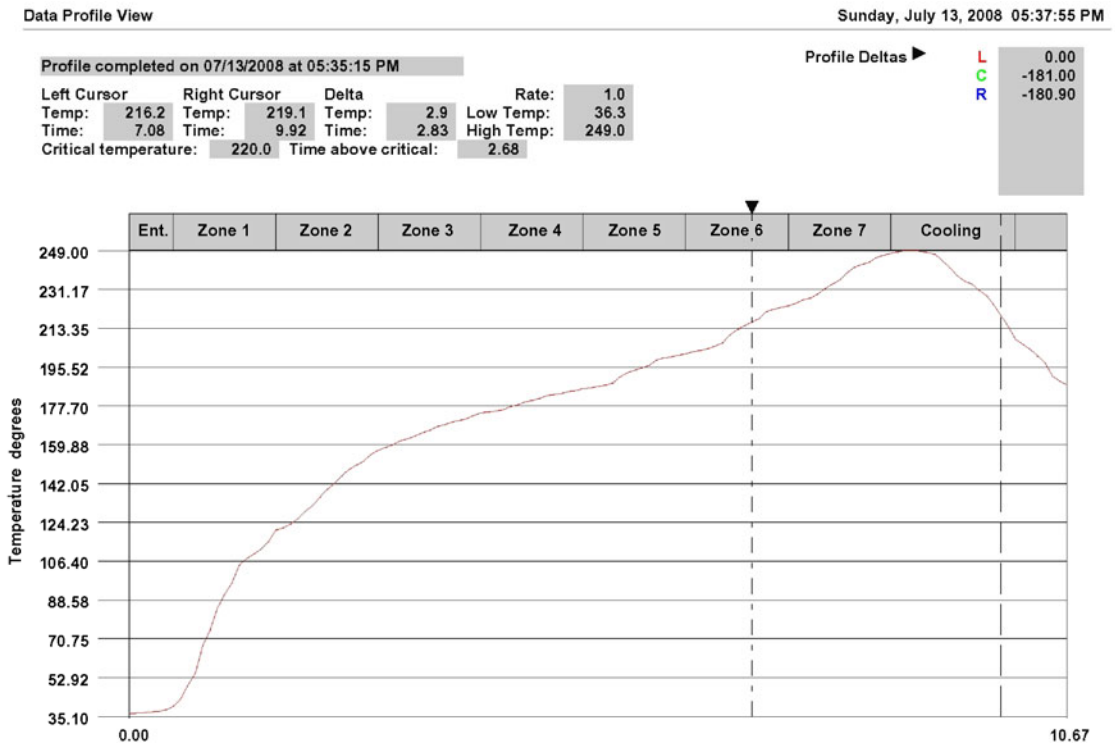


Figure 15. Typical Solder Reflow Profile for Pb-free SnAgCu Solder

For the solder reflow process, a fixture may be required to (a) keep the device in place while running though the reflow furnace, (b) prevent the device from lifting off due to buoyancy forces when the solder melts, and (c) keep the leads in contact with the solder paste so it forms a good solder joint. The amount of force needed depends on the amount and type of solder used and the soldering process. An experiment was designed to examine the effects of downward force on solder quality. The heat spreaders of NI-780S packages (Case 465A) were soldered to a copper plate. Two types (eutectic 63/37 Sn/Pb solder and SAC305 Pb-free solder) of 0.004″ (0.10 mm) thick solder preforms were used for the solder layer. No-clean flux was applied to the heat spreader and the copper plate. The parts were reflowed in a convection oven to the profiles shown in Figure 14 for SnPb and Figure 15 for Pb-free solders. In the design of experiments, four different values of weights (0, 0.3, 2.5, 5.0 grams for eutectic solder and 0, 2.5, 5.0 and 10 grams for PB-free solder) were placed on top of the device in addition to self-weight. Based on the voiding observed and the solder flow outside the package footprint, it was determined that 2.5 grams of weight plus the self-weight of the component in the NI-780S package (Case 465A) provided the best solder joint. The voiding was minimal at self-weight plus 2.5 grams of weight. With just the self-weight alone, the void distribution was higher. Increasing the weight above the 2.5 grams caused more solder flow out as well as more voids.

In general, Freescale recommends a slight downward force equivalent to 2.5 grams of weight on a NI-780S package (Case 465A) to improve the solder joint quality. Adding weight on top of the device is possible and can be accomplished within the pick-and-place operation. One problem with using weight alone is that it may move during the reflow process. Instead, a clip or fixture can be designed to hold the part in place as well as applying a slight downward force.

It is important to ensure that any force applied does not flex or bend the leads more than 0.015″ (0.38 mm) from their received nominal position. Excessive bending of the leads can result in mechanical failure of the device or less reliable solder joints.

SOLDER JOINT INSPECTION

Inspection of the solder joint in the cavity between the package flange and the heatsink cannot be accomplished by a simple optical inspection. Two methods have been assessed for investigating this joint. Both X-ray and scanning acoustical microscopy look through the carrier to image the solder attach layer.

X-ray has been demonstrated to show voids through up to 0.25″ (6.0 mm) thick copper. Figure 16 demonstrates a typical X-ray image of solder voiding. In this demonstration, an NI-780 (Case 465) is viewed on a 0.162″ (4.11 mm) thick copper plate using purposely voided eutectic SnPb solder. The assembly was analyzed using an SMT Cougar™ X-ray system from Xylon International. This system used 160 kV at 12 watts. X-ray is a viable tool because it can be done in air. Many of the larger X-ray systems can accommodate PCBs up to 20″ × 24″.

X-ray inspection does have some drawbacks. Because the X-rays are transmitted through the piece, all artifacts in the path of the X-rays are captured. Any die attach voids or other artifacts will be captured and subject to interpretation. Also, an X-ray image of void-free solder is very difficult to interpret. Even state-of-the-art X-ray equipment cannot penetrate copper thicknesses greater than 0.25″ (6.0 mm).

Scanning acoustical microscopy has been used to identify voids in the solder layer through a Cu heatsink up to 0.25″ thick. A main drawback to this method is that it uses water to transmit the energy. The introduction of finished PCBs into a

DI water bath is considered a substantial field reliability risk. Acoustic microscopy also has the same limitations in terms of the thickness they can penetrate as X-rays. Freescale does not recommend use of this method to determine the quality of solder joint on devices that are going to be deployed in the field.

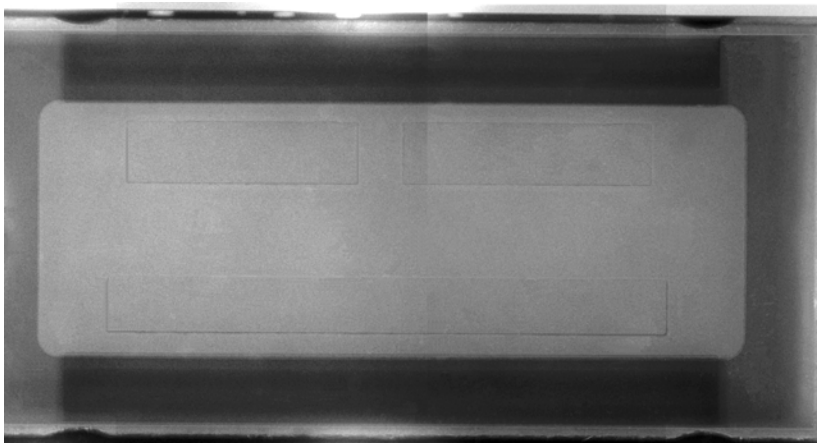


Figure 16. X-Ray Image Showing Voids in Solder Attach for NI-780 on a 0.162″ (4.11 mm) Thick Copper Plate
(The image was taken on a XYLON International system. Used with permission.)

RELIABILITY OF THE SOLDER JOINT

For the purpose of establishing the reliability of the PA assembly performed using the methodology described here, a power life test evaluation was performed using an MRF19090S power transistor. This device operates at 1.9 GHz with a P1dB output power of 90 watts. Similar devices in Freescale's RF portfolio operate at frequencies as high as 3.5 GHz and power as high as 1000 watts of RF output power. The methodology described here is applicable to all the devices with metal flange and leads that have gold plating as the final layer.

Assemblies using these design concepts were built in an automated solder mount assembly line with device leads solder attached to a PCB and the flange soldered to a copper carrier. The test assemblies were bolted to fan-cooled, finned aluminum heatsinks with thermal compound as the interface between the bottom of the copper carrier and aluminum heatsink. Power life testing was done at a specific duty cycle and heatsink temperature. A power cycling test specimen using MRF19090S device is shown in Figure 17. The assemblies were fabricated in accordance with the procedure described in this Application Note.

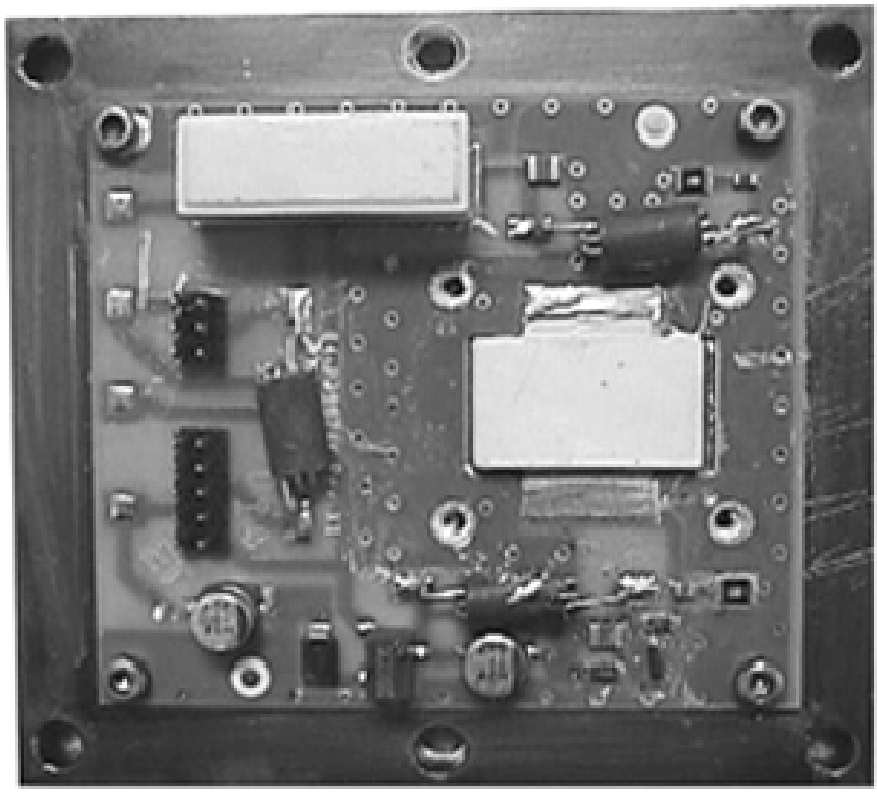


Figure 17. Power Cycling Test Samples Used to Check the Reliability of Solder Joints

The PCB is screen-printed with Sn/Pb/Ag solder paste using a stainless steel stencil, 0.006″ (0.15 mm) thick. The copper carriers were plated with approximately 1,000 to 1,500 micro-inches (25 to 38 micron) of electroless nickel to prevent copper from oxidizing. Au plating was omitted due to cost and not much of a storage time between the time the carriers were fabricated and PA boards were assembled. The carriers contain a recessed cavity that is plated with 0.0003″ (7.6 micron) of tin lead (60-40). The PCB with solder paste was put on top of the carrier and loosely attached using #4-40 screws. Since this test board is fairly small and the test condition only involves DC biasing, the PCB was not soldered down to carrier to avoid cost. After the PCB is placed on the carrier and prior to placing the component in the recessed cavity, two 0.002″ (50 micron) thick solder preforms and two drops of no-clean flux are set into the recess. Next, the device is placed on top of the solder preform where the flange of the device is touching the solder preform and the leads are touching the solder paste. After placing the component, the assembly is placed on a reflow boat. Finally, the entire assembly is placed in a forced convection reflow furnace.

After the reflow operation, the PCB is secured to the copper carrier using six #4-40 socket head cap screws with 5 in.-lbs. of torque (M3 screws with 0.6 N-m of torque). For small PCBs, it is possible to attach the backside of the entire PCB to the copper carrier using either solder or conductive epoxy instead of bolting it to the pallet.

The completed, reflowed board/carrier assemblies are screw mounted to the aluminum heatsink after evenly spreading the backside of the copper pallet with ~0.001″ (25 micron) of thermal compound. An actual board assembly used for the power life test with the MRF19090S device (NI-880S, Case 465C) is shown in Figure 17. Care should be taken to ensure that adequate electrical and thermal contact is established between the carrier and the bottom of the device flange.

RESULTS

The assemblies were cycled under DC conditions at 26 volts and 135 watts of dissipated power. At 90 watts of RF output power and 40% efficiency for the HV4 technology of this device, the dissipated power is 135 watts. A peak case temperature of more than 90°C was achieved as measured by a thermocouple directly under the heatsink of each device. The MRF19090S device has the specified junction to case resistance (θ_{JC}) of 0.65°C/W. Based on this, the junction temperature at 135 watts power dissipation will be 180°C when the sink temperature is 90°C. The temperature rise is calculated based on the θ_{JC} plus the interface resistance. The devices were cycled at a 50% duty cycle with a 15 minute hold time at power on and a 15 minute hold time at power off condition for 2000 cycles. This represents 1000 hours of power cycling

Lead and solder joint temperatures were measured on several PCBs using a scanning infrared microscope after the power cycling. Lead temperatures were found to be approximately 90°C at 135 watts of power dissipation and a 90°C sink temperature. Figure 18 displays an image taken from the infrared microscope. Following the power life testing, solder joints were visually inspected and found to have no cracks after 2000 cycles. This prescribed mounting methodology satisfies the thermal and mechanical requirements of mounting a power transistor in a metal-ceramic package.

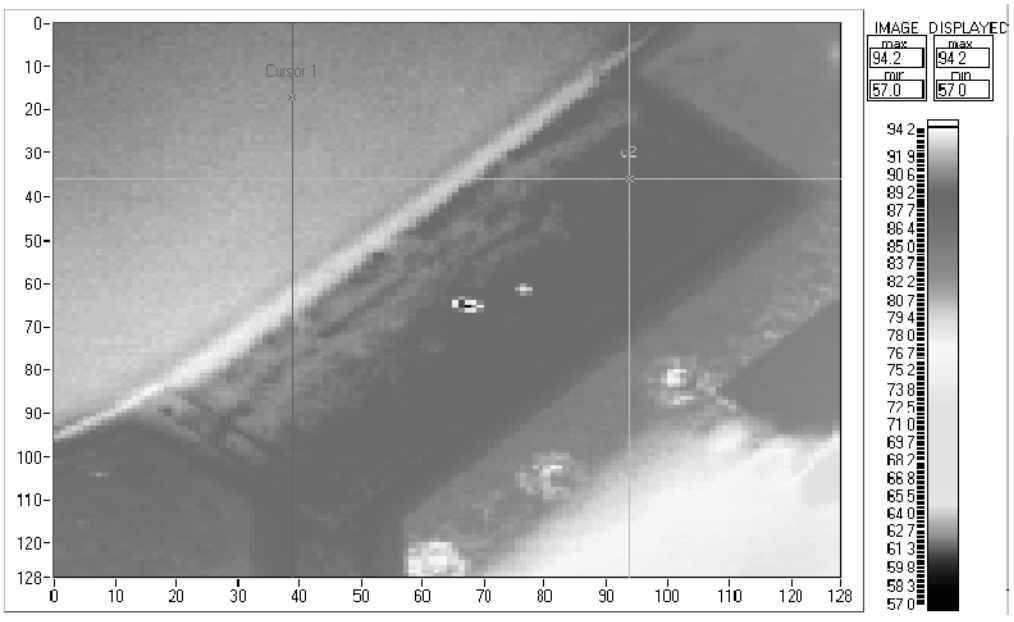


Figure 18. IR Image of Solder Joints at Drain Lead

The mounting scheme design significantly influences both the thermal and electrical performance of the device. The mounting method described here uses solder as an interface at the source contact of the RF power device. It is highly recommended that the customer carefully evaluate thermal and electrical performance for their power amplifier assembly. The selection of the interface material will depend on the customer's sink temperature, as well as the amount of power being dissipated by the transistor in the application. The total thermal resistance between the junction and the sink should

be such that the temperature rise between the junction and the sink at maximum power and maximum sink temperature condition will still keep the junction temperature below the maximum value, based on the expected lifetime. The mounting method described here is a guide; it should not be substituted for a complete system-level performance analysis.

SUMMARY

This application note provides the information needed to develop a robust assembly process for mounting RF power devices in air cavity packages into customer PA applications by soldering the device to PCBs and carriers. Consideration was given to factors such as material selection, mechanical design parameters, assembly methodologies, and inspection tools. Successfully integrating the guidelines provided here can lead to an assembly process that can yield:

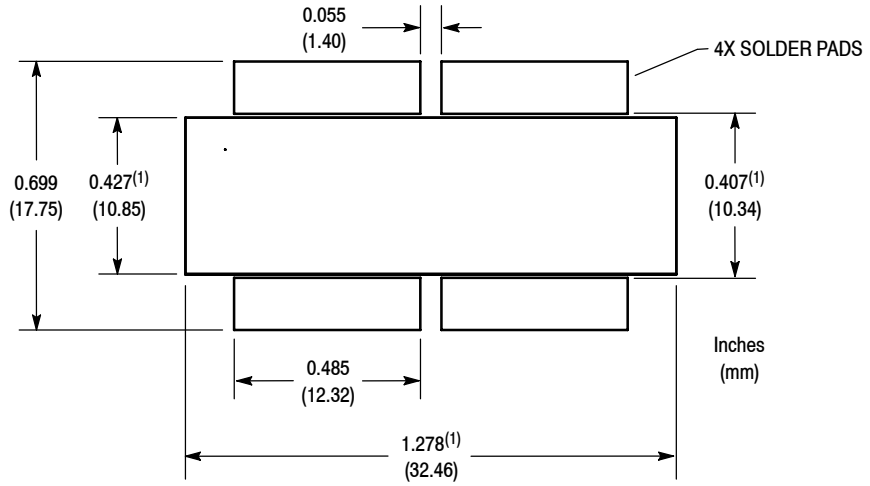
- A reliable solder joint at the source contact to provide low thermal resistance for the system.
- A low and constant source impedance to provide stable RF performance.
- A reliable solder joint at the leads that will withstand extensive thermal cycling in field use.
- A cost-effective automated assembly process that will provide superior thermal and electrical performance even though the initial bill of material cost may be higher.
- Controlling design factors such as PCB tolerances and pad layout can minimize impact on solder joint reliability and placement interaction between the package, the PCB and the carrier.

Material selection and assembly process choices lead to high quality and reliable solder joints, which results in a lower-cost system level solution and improved performance for the PA assembly.

LIST OF REFERENCES

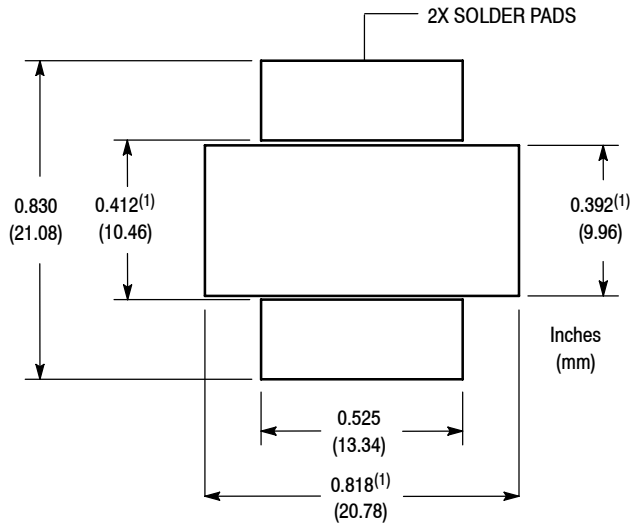
1. Freescale Application Note AN1907, *Solder Reflow Attach Method for High Power RF Devices in Over-Molded Plastic Packages.*
2. Shah, M., Wetz, R., & Jang, J. (2007), “Reliability and Microstructure of SnAgCu Solder Joints in High Power RF Packaging,” *40th International Symposium on Microelectronics*, San Jose, CA.

Appendix A. PCB Layout Recommendations



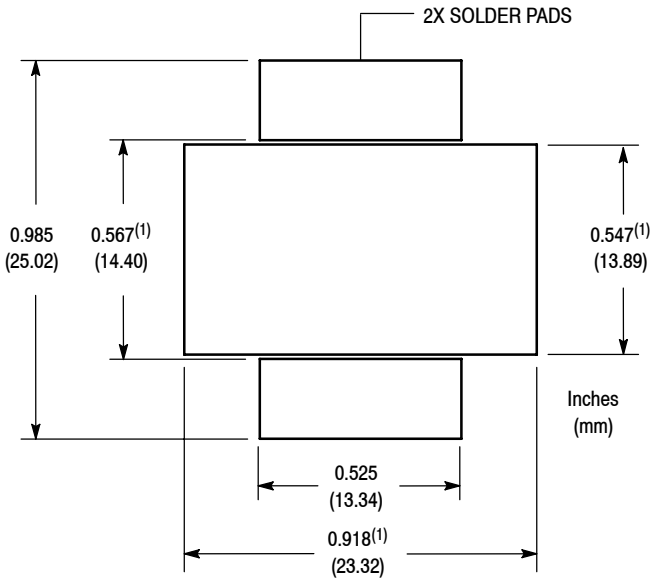
1. Slot dimensions are minimum dimensions and exclude milling tolerances.

Figure A-1. Case 375E (NI-1230S)



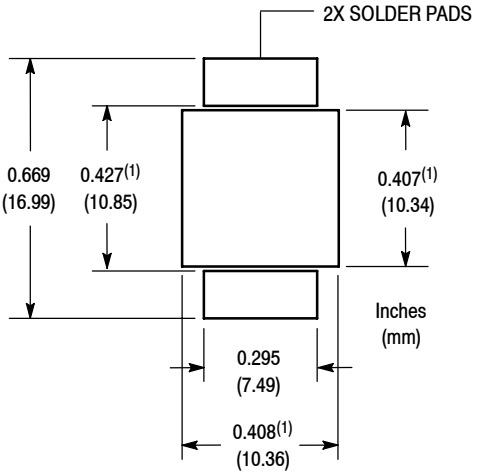
1. Slot dimensions are minimum dimensions and exclude milling tolerances.

Figure A-2. Case 465A (NI-780S)



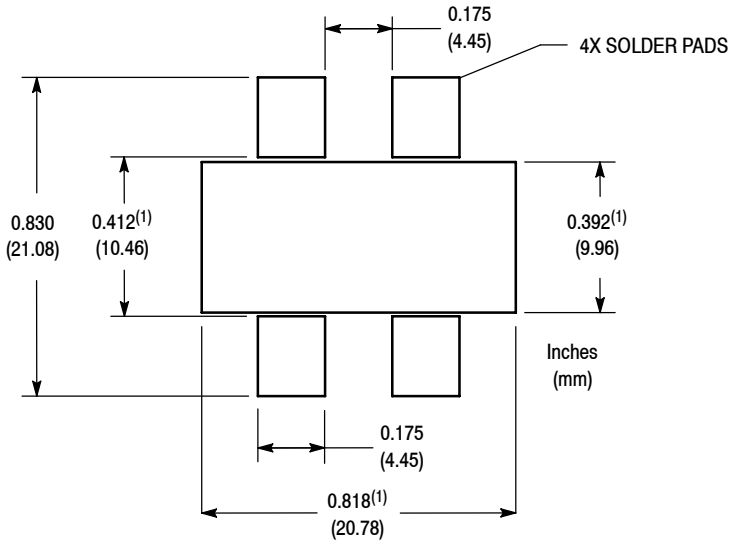
1. Slot dimensions are minimum dimensions and exclude milling tolerances.

Figure A-3. Case 465C (NI-880S)



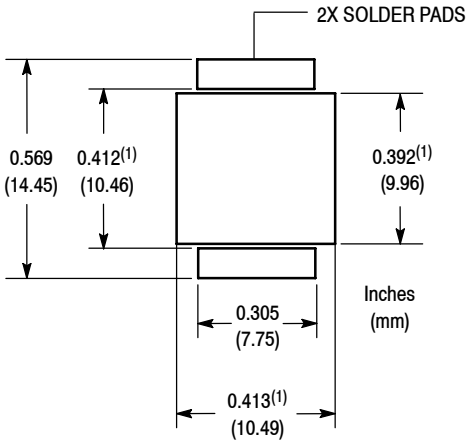
1. Slot dimensions are minimum dimensions and exclude milling tolerances.

Figure A-4. Case 465F (NI-400S)



1. Slot dimensions are minimum dimensions and exclude milling tolerances.

Figure A-5. Case 465H (NI-780S-4)



1. Slot dimensions are minimum dimensions and exclude milling tolerances.

Figure A-6. Case 465J (NI-400S-240)

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