RFUV1702

17.7GHz TO 19.7GHz GaAs MMIC IQ UPCONVERTER

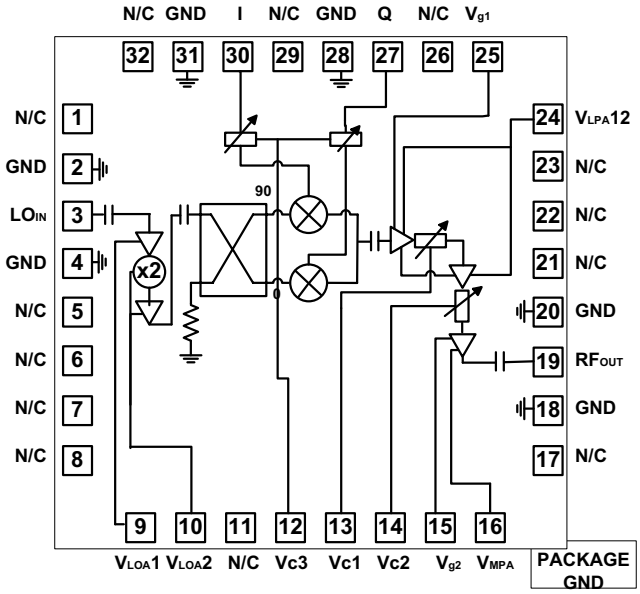
Package: QFN, 32-Pin, 5mm x 5mm x 0.95mm

Features

- RF Frequency: 17.7GHz to 19.7GHz
- LO Frequency: 6.85GHz to 11.85GHz
- IF Frequency: DC to 4GHz
- Conversion Gain (Max): 21dB
- Conversion Gain (Min): -5dB
- NF (Max. Gain): 9dB
- NF (Min. Gain): 18dB
- OIP3 (Max. Gain): +28dBm
- OIP3 (Min. Gain): +10dBm
- Image Rejection: ≥15dBc

Applications

- Point-to-Point
- VSAT



Functional Block Diagram

Product Description

RFMD's RFUV1702 is a 17.7GHz to 19.7GHz GaAs pHEMT upconverter, incorporating an integrated frequency multiplier (x2), LO buffer amplifier, a balanced single sideband (image rejection) mixer followed by variable gain amplifier, and DC decoupling capacitors. The combination of high performance parts and low-cost packaging makes the RFUV1702 a cost-effective solution, ideally suited to both current and next generation point-to-point and VSAT applications. RFUV1702 is packaged in a 5mm x 5mm QFN to simplify both system level board design and volume assembly.

Ordering Information

RFUV1702S2	2-Piece Sample Bag
RFUV1702SB	5-Piece Bag
RFUV1702SQ	25-Piece Bag
RFUV1702SR	100 Pieces on 7" reel
RFUV1702TR7	750 Pieces on 7" reel
RFUV1702PCBA-410	Evaluation Board

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Absolute Maximum Ratings

Parameter	Rating	Unit
LPA Drain Voltage V_D	6	V
LOA Drain Voltage	6	V
IF Input Power	15	dBm
LO Input Power	15	dBm
T_{OPER}	-55 to +85	°C
T_{STOR}	-65 to +150	°C
ESD Human Body Model	Class 1A	

Caution! ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

RFMD Green: RoHS compliant per EU Directive 2002/95/EC, halogen free per IEC 61249-2-21, < 1000 ppm each of antimony trioxide in polymeric materials and red phosphorus as a flame retardant, and <2% antimony in solder.

Nominal Operating Parameters

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
RF Frequency	17.7		19.7	GHz	
LO Frequency	6.85		11.85	GHz	
IF Frequency	DC		4.0	GHz	
LO input Drive		0		dBm	
Conversion Gain (Max.)		21		dB	
Conversion Gain (Min.)		-5		dB	
NF (Max. Gain)		9		dB	
NF (-5dB Gain)		18		dB	
OIP3 (Max. Gain)		28		dBm	
OIP3 (-5dB Gain)		10		dBm	
Image Rejection		15		dBc	
LO Leakage at RF-Port (Max. Gain)		-5		dBm	With IQ bias
LO Return Loss		10		dB	
RF Return Loss		10		dB	
V_{VA}	-4		0	V	
V_{MPA}		4.5		V	
V_{LPA12}		3.5		V	
V_{LOA1}, V_{LOA2}		4		V	
I_{LOA1}, I_{LOA2}		206		mA	
I_{LPA12}*		120		mA	Adjust $V_{G1} \approx$ -0.4V to achieve I_{LPA12} = 120mA
I_{MPA}*		120		mA	Adjust $V_{G2} \approx$ -0.4V to achieve I_{MPA} = 120mA

*Note: These currents can be adjusted to optimize performance for varying application requirements.

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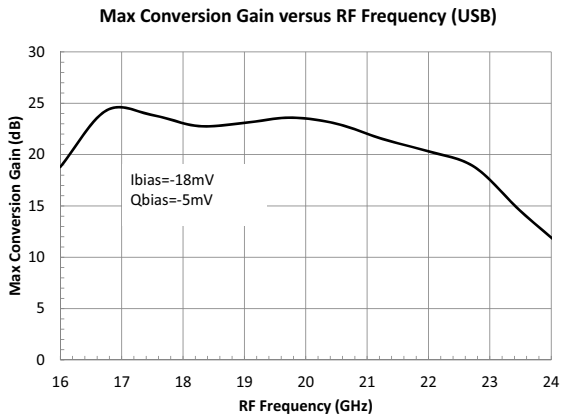
Typical Electrical Performance

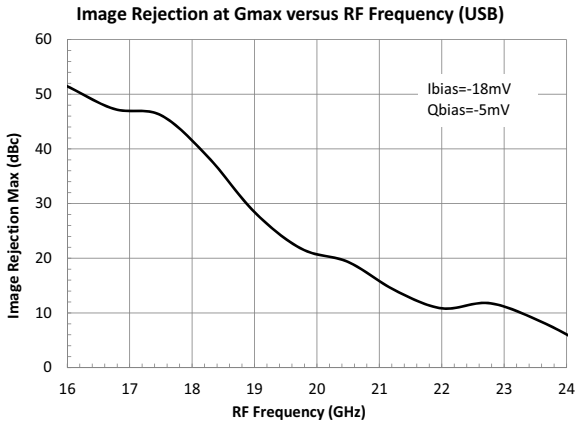
Measurements performed on connectorized evaluation board as shown on P.8 with I and Q (IF) ports connected to an external 90° Hybrid, LO Power = 0dBm and IF = 2.5GHz, -10dBm, V_{LPA12} = 3.5V, I V_{LPA12} = 120mA* , V_{MPA} = 4.5V, I V_{MPA} = 120mA**, V_{LOA1} = V_{LOA2} = 4V and V_{C1} = V_{C2} = V_{C3} = -4V, unless otherwise stated.

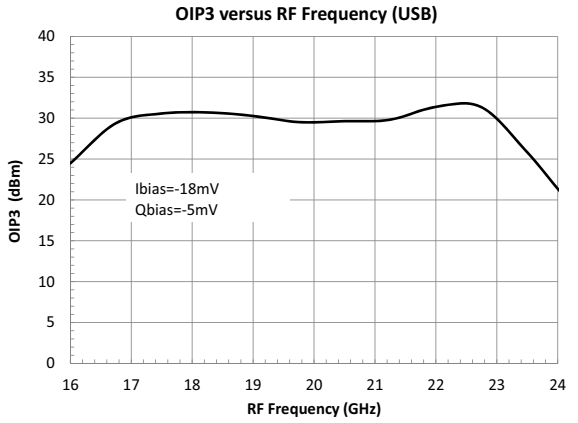
*Adjust V_{G1} around -0.45V to get I V_{LPA12} = 120mA

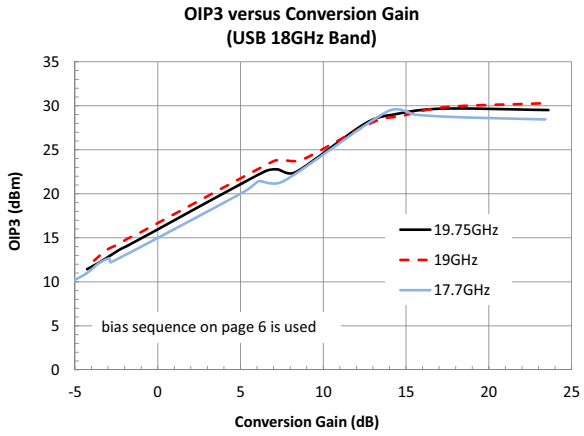
**Adjust V_{G2} around -0.45V to get I V_{MPA} = 120mA

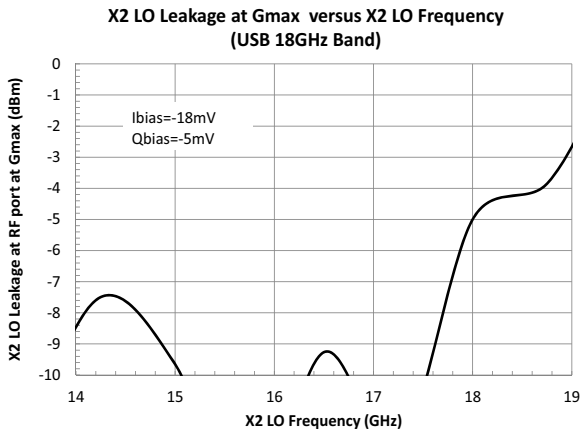
USB Conversion Gain, Image Rejection, OIP3, and LO Leakage

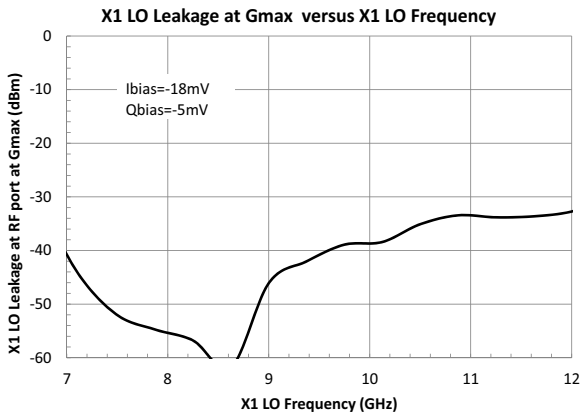






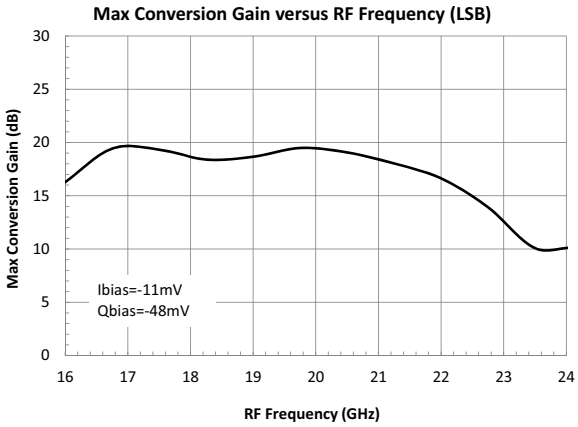


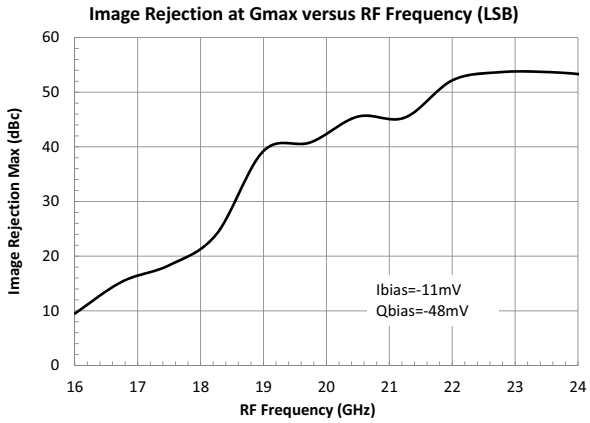


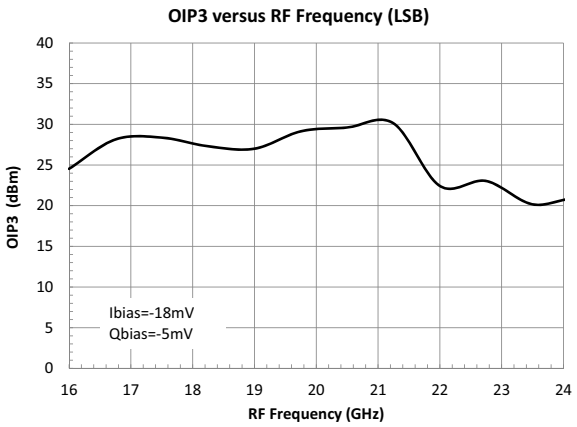


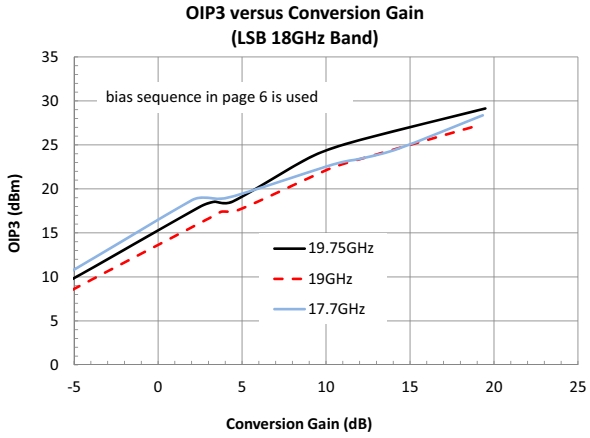
LO Frequency (13.5GHz to 21.5GHz)

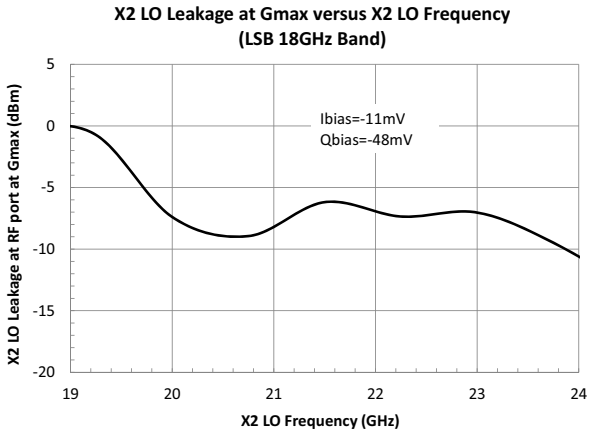
LSB Conversion Gain, Image Rejection, OIP3, and LO Leakage











LO Frequency (18.5GHz to 26.5GHz)

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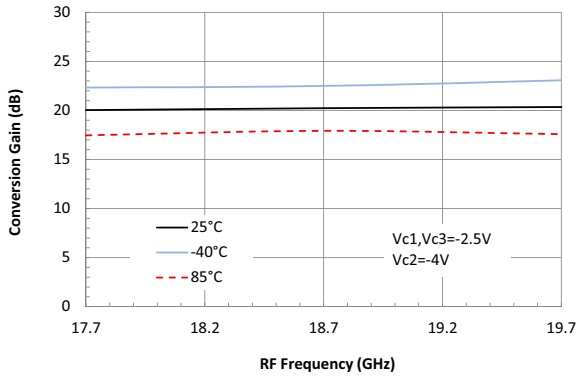
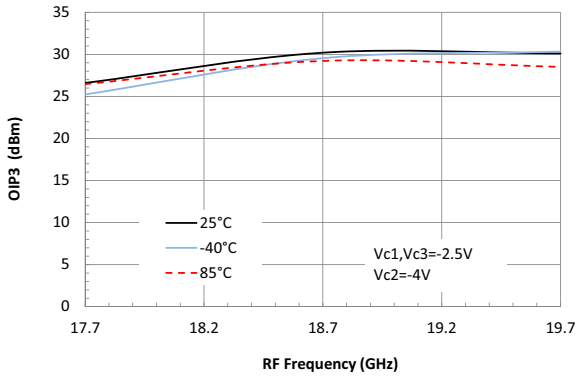
Over Temperature Performance (USB)

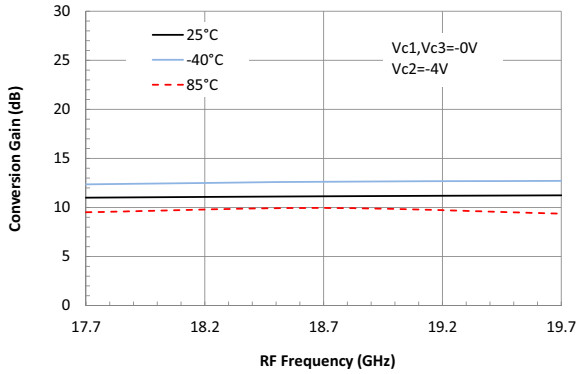
Conversion Gain versus RF Frequency Over Temperature at 20dB CG set point (USB)



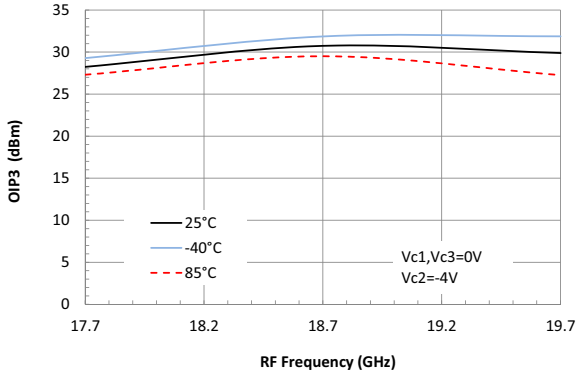
OIP3 at 20dB CG versus RF Frequency Over Temperature (USB)



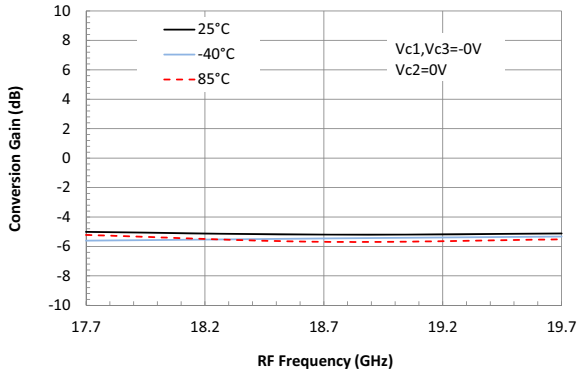
Conversion Gain versus RF Frequency Over Temperature at 11dB CG set point (USB)



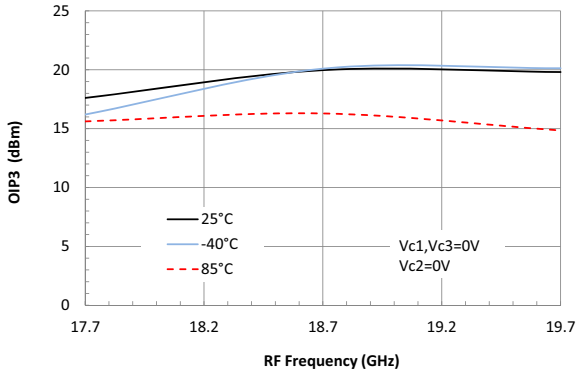
OIP3 at 11dB CG versus RF Frequency Over Temperature (USB)



Conversion Gain versus RF Frequency Over Temperature at -5dB CG set point (USB)



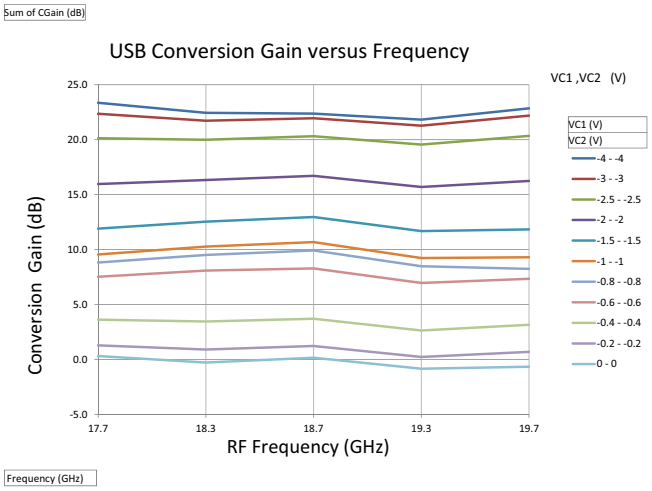
OIP3 at -5dB CG versus RF Frequency Over Temperature (USB)

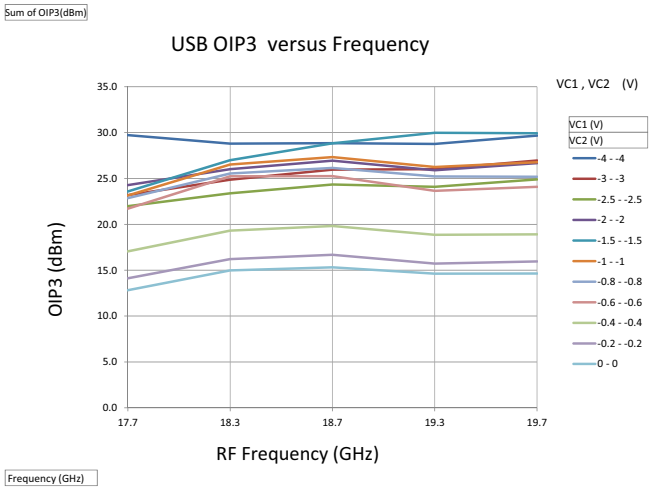


LO Frequency (15.2GHz to 17.2GHz)

Performance Using Single Control Line (without IQ bias)_1

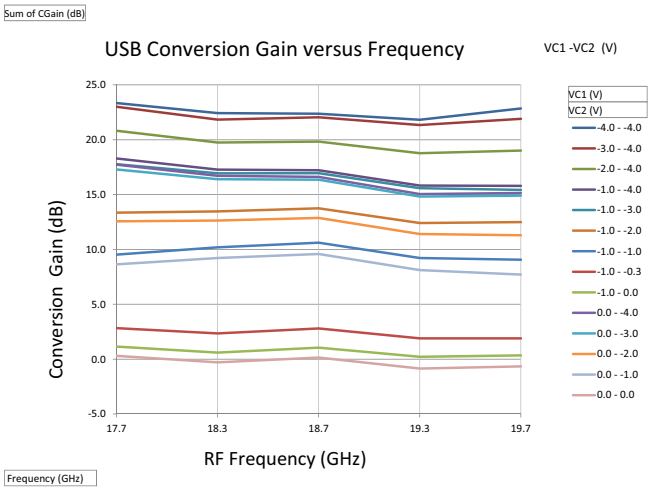
V_{MPA} = 4.5V, V_{LPA12} = 3.5V, V_{LOA1} = V_{LOA2} = 4V, I_{total} = 450mA, V_{G1} = V_{G2} = -0.4V, V_{C3} = -4V
V_{C1} and V_{C2} are connected together off chip and changes over (-4V to 0V)

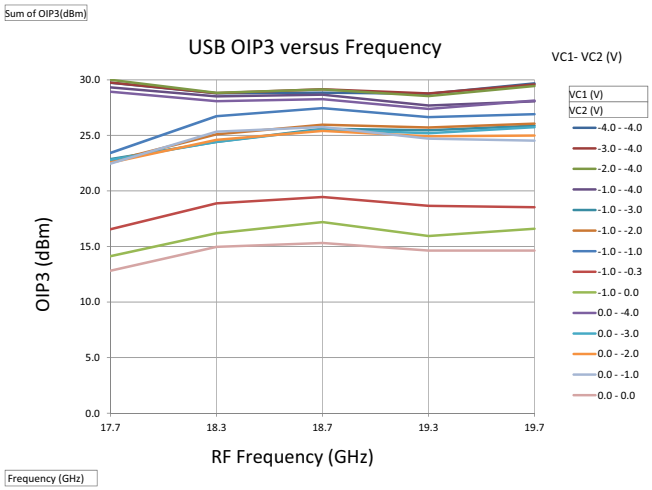




Performance Using Double Control Line (without IQ bias)_2

V_{MPA} = 4.5V, V_{LPA12} = 3.5V, V_{LOA1} = V_{LOA2} = 4V, I_{total} = 450mA, V_{G1} = V_{G2} = -0.4V, V_{C3} = -4V
V_{C1} and V_{C2} are separately controlled and changes over (-4V to 0V)





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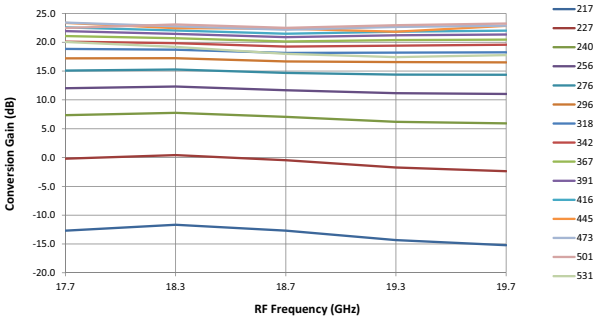
Performance Using Single Control on V_{G1} = V_{G2} (without IQ bias)_3

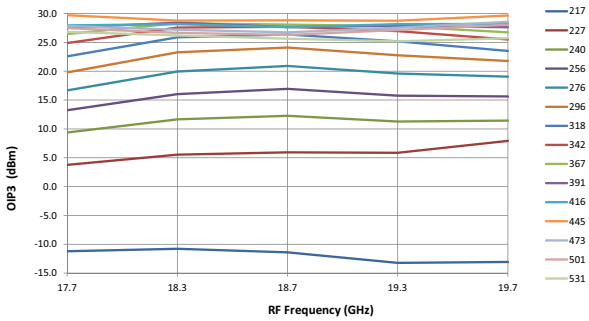
V_{MPA} = 4.5V, V_{LPA12} = 3.5V, V_{LOA1} = V_{LOA2} = 4V, V_{C1} = V_{C2} = V_{C3} = -4V

V_{G1} and V_{G2} are connected together off chip and changes over (-0.3V to 1V)

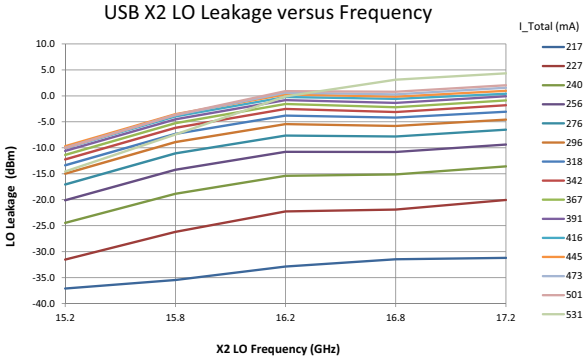
USB Conversion Gain versus Frequency



USB OIP3 versus Frequency



USB X2 LO Leakage versus Frequency



Bias Sequence and Gain Control

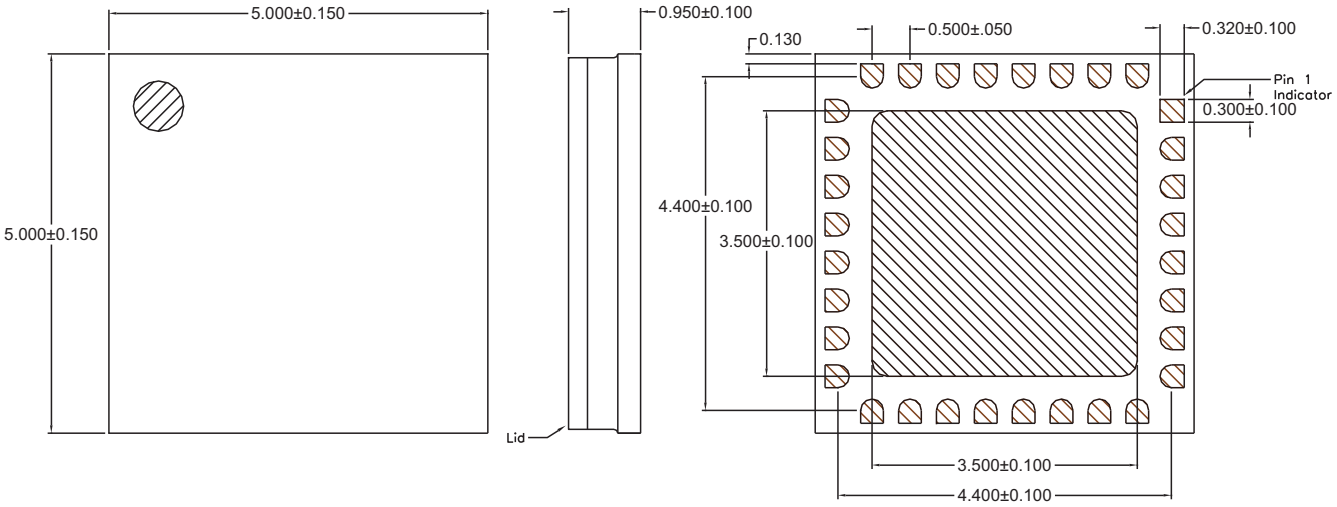
Optimum performance is achieved using sequential bias. At maximum gain (V_{C1}, V_{C3}), and V_{C2} are set at -4V and V_{G2} is set at -0.4V. (V_{C1}, V_{C3}), V_{C2} and V_{G2} are biased in sequence. The first dynamic range is achieved by setting (V_{C2} at -4V and V_{G2} at -0.4V) and varying (V_{C1}, V_{C3}) over the (-4 to -1V) range as shown in the table below. Similarly, the second dynamic range is achieved by setting (V_{C1}, V_{C3}) at -1V, V_{G2} at -0.4V and varying V_{C2} over the (-4 to -0.3V) range. Finally, the third dynamic range is achieved by setting (V_{C1}, V_{C3}) at -1V, V_{C2} at -0.3V and varying V_{G2} over the (-0.4 to -1V) range.

Test Conditions and Bias Sequence

Bias Sequence										
	G_{MAX}									G_{MIN}
(V_{C1}, V_{C3})	-4	-2	-1	-1	-1	-1	-1	-1	-1	-1
V_{C2}	-4	-4	-4	-2	-1	-0.3	-0.3	-0.3	-0.3	-0.3
V_{G2}	-0.4	-0.4	-0.4	-0.4	-0.4	-0.4	-0.6	-0.8	-0.9	-1

Package Outline Drawing

QFN, 32-Pin, 5mm x 5mm x 0.95mm



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Pin Names and Description

Pin	Name	Description
1	N/C	Not Connected.
2	GND	Ground.
3	LO	Local Oscillator Input. AC Coupled and Matched to 50Ω.
4	GND	Ground.
5	N/C	Not Connected.
6	N/C	Not Connected.
7	N/C	Not Connected.
8	N/C	Not Connected.
9	VLOA1	LOA Stage1 Drain Bias.
10	VLOA2	LOA Stage2 Drain Bias.
11	N/C	Not Connected.
12	VC3	Control Line Number 3 (See Bias Sequence Description).
13	VC1	Control Line Number 1 (See Bias Sequence Description).
14	VC2	Control Line Number 2 (See Bias Sequence Description).
15	VG2	MPA Gate Bias.
16	VMPA	MPA Drain Bias.
17	N/C	Not Connected.
18	GND	Ground.
19	RFOUT	RF Output. AC Coupled and Matched to 50Ω.
20	GND	Ground.
21	N/C	Not Connected.
22	N/C	Not Connected.
23	N/C	Not Connected.
24	VLPA1, VLPA2	LPA Stage 1, 2 Drain Bias.
25	VG1	LPA Stage 1, 2 Gate Bias.
26	N/C	Not Connected.
27	Q	IF Q Input.
28	GND	Ground.
29	N/C	Not Connected.
30	I	IF I Input.
31	GND	Ground.
32	N/C	Not Connected.

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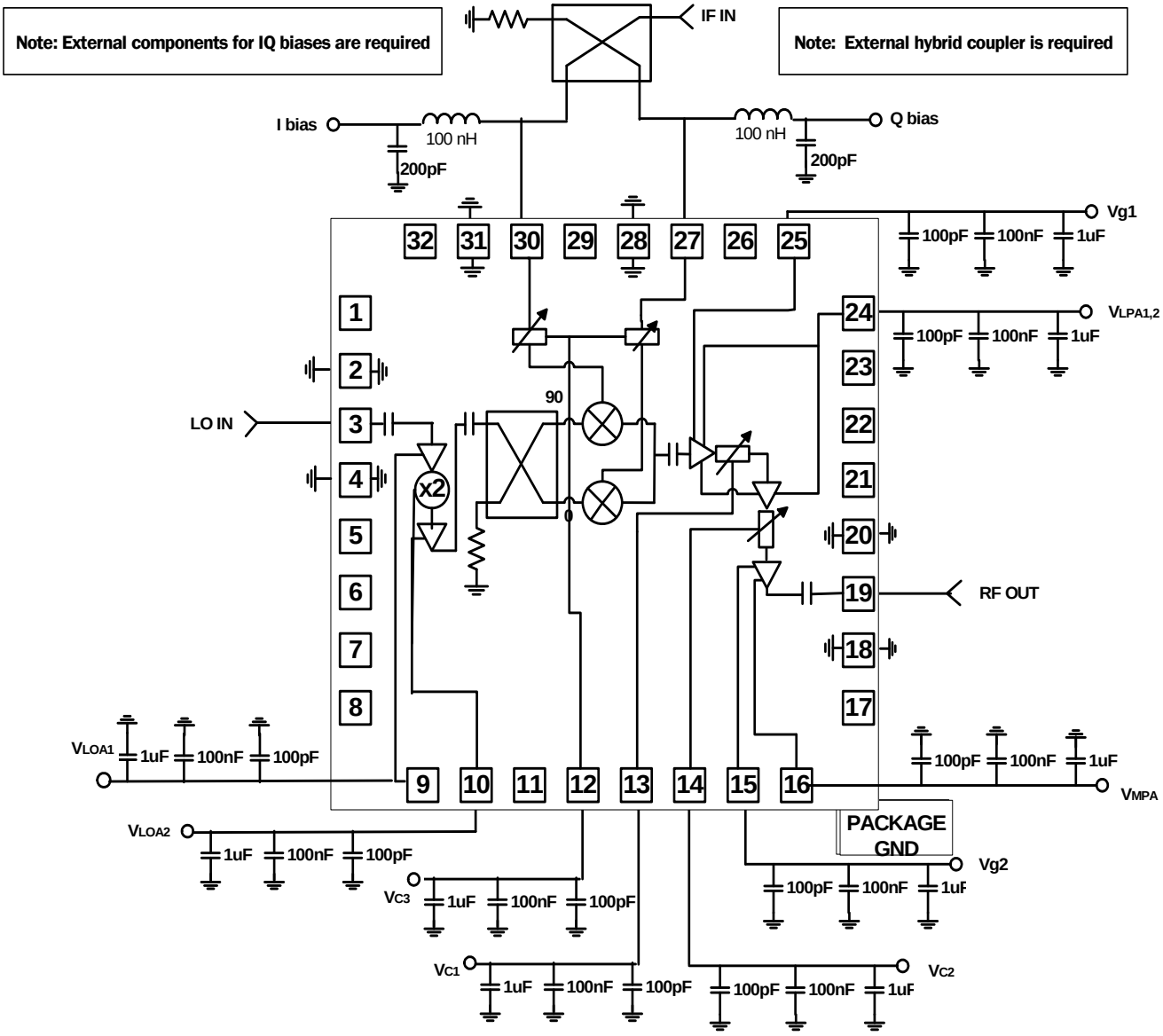
Application Circuit Block Diagram



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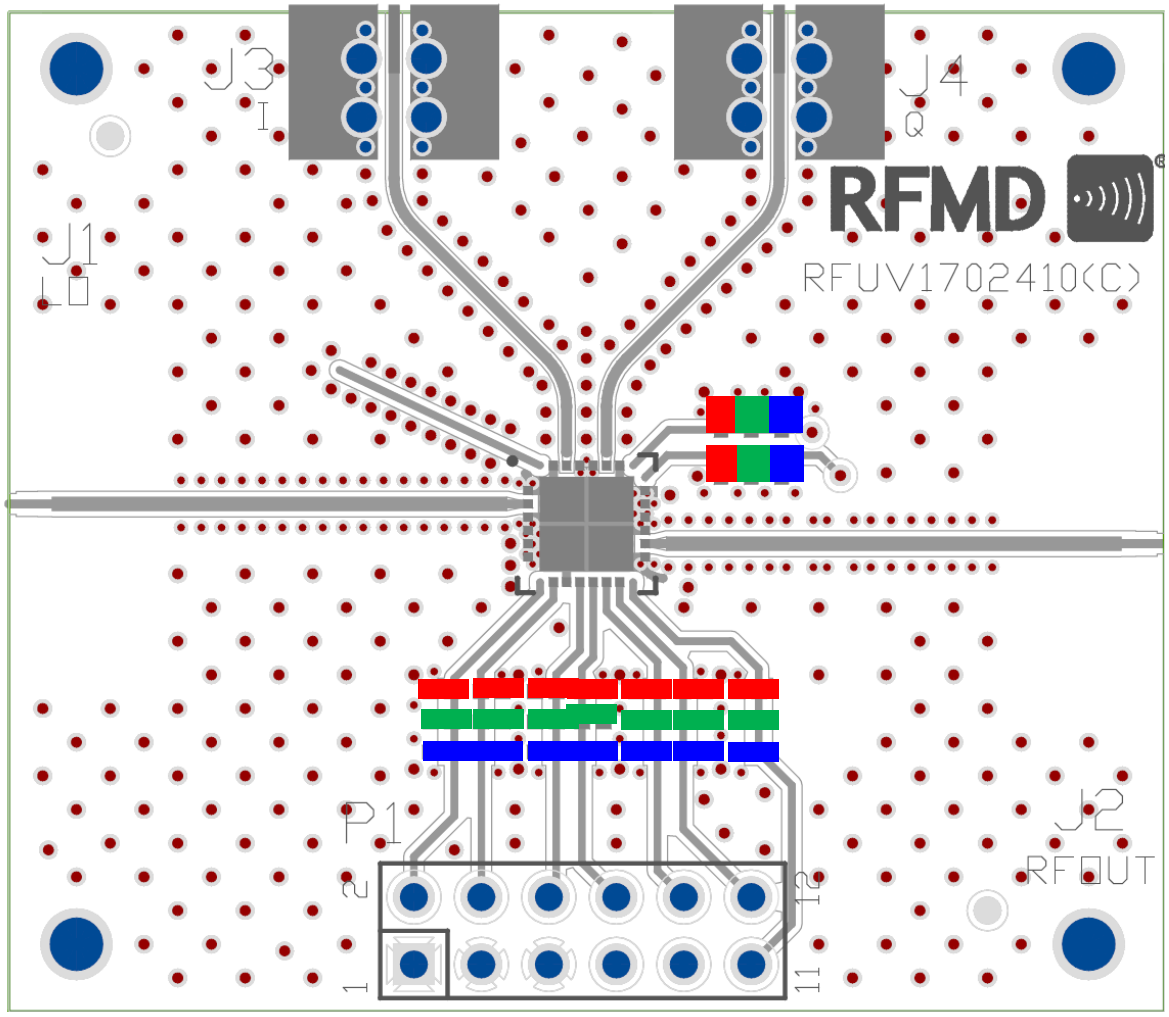
Evaluation Board Layout



VLOA1 VLOA2 VC3 VC1 VC2 VG2

GND GND GND VG1 VLPA2 VMPA

100pF (0402)

100nF (0402)

1uF (0402)

Test Condition

LO Power	0dBm
IF Power	-10dBm
V_{MPA}	4.5V, 120mA
$V_{LPA1,2}$	3.5V, 120mA
V_{LOA1}, V_{LOA2}	4V, 200mA
V_{C1},V_{C3}	-4 to -1V (no current)
V_{C2}	-4 to -0.3V (no current)

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