Freescale Semiconductor
Application Note

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MC13892 Functional Pin Description

1 Overview

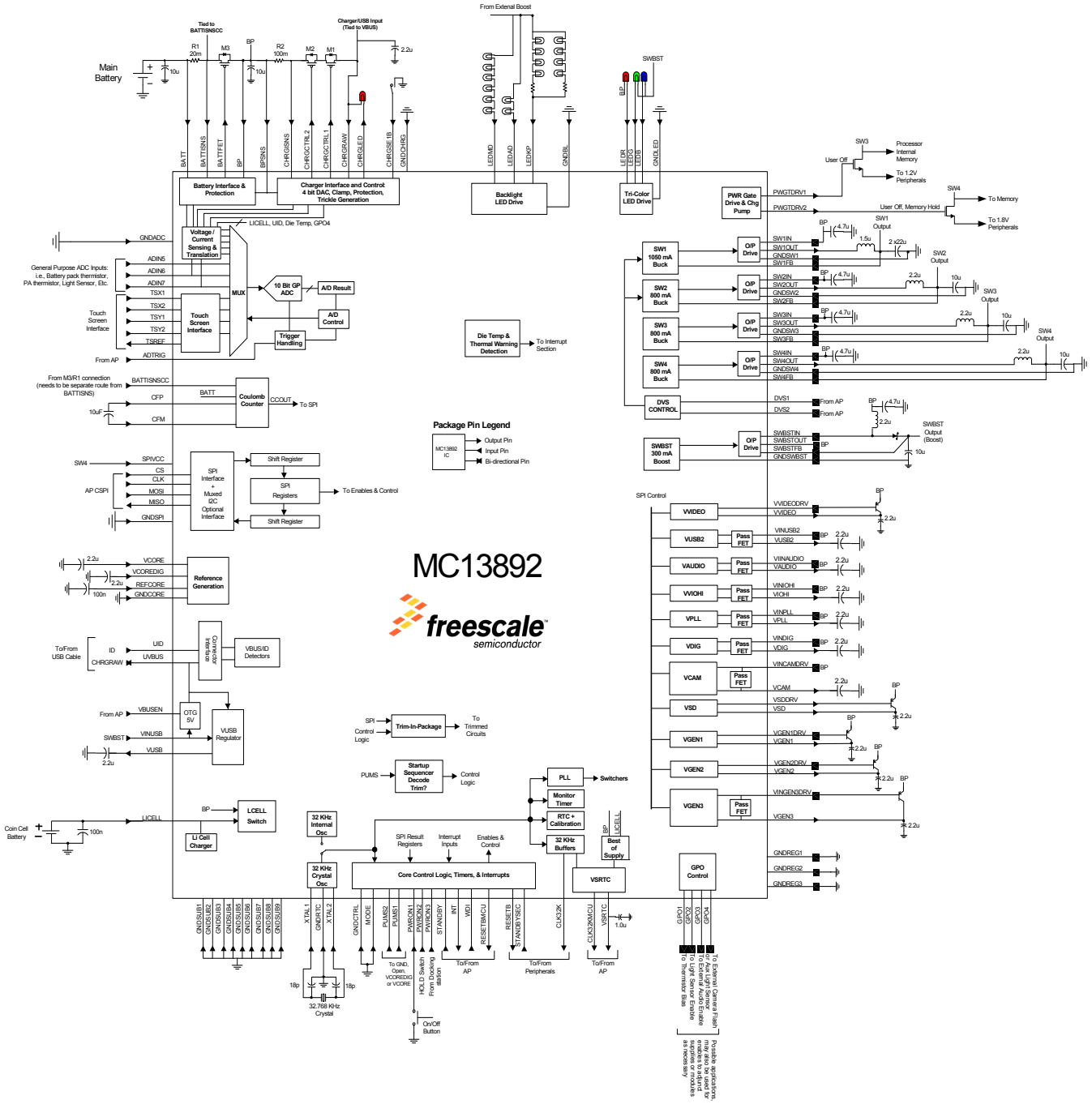
This document is intended to show how to design a schematic using the MC13892, by describing the functionality of each one of its pins, as well as how to connect them for a specific application.

Contents

2 Scope

The typical connection of each pin is presented in the following table. It is common that some of the pins have different functionalities, so more than one typical connections are presented, and the applications explained. This table also shows how to connect the pins when they are not used.

3 Typical Application Diagram



4 Typical Connections

Pin	Description	Typical Connection	Connection if Unused
Charger			
CHRGRAW	1. Charger input. The charger voltage is measured through an ADC at this pin. The minimum voltage for this pin depends on BATTMIN threshold value. 2. Output to the battery supplied accessories. The battery voltage can be applied to an accessory by enabling the charge path for the accessory via the CHRGRAW pin.	Connect the wall charger/USB charger here. This pin must be shorted to the UVBUS pin in cases where the charger is being supplied from the USB cable.	Unconnected
CHRGCTRL1	Driver output for charger path FET M1.	Base of MOSFET M1.	Unconnected
CHRGCTRL2	Driver output for charger path FET M2.	Base of MOSFET M2.	Unconnected
CHRGISNS	Charge current sensing point 1. The charge current is read by monitoring the voltage drop over the charge current 100 mOhm sense resistor connected between the CHRGISNS and BPSNS pins.	Connect this pin directly to one of the terminals of the 100 mOhm sense resistor.	Connect to BP pin
BPSNS	1. BP sense point. The BP voltage is sensed at this pin and compared with the voltage at CHRGRAW. 2. Charge current sensing point 2. The charge current is read by monitoring the voltage drop over the charge current 100 mOhm sense resistor. This resistor is connected between this pin and CHRGISNS.	Connect this pin directly to the other terminal of the 100 mOhm sense resistor.	Connect to BATT pin
BP	This pin is the application supply point, which is the input supply to the IC core circuitry. The application supply voltage is sensed through an ADC at this pin.	This pin will provide the charging voltage of the battery and the supply voltage of all the switchers and LDOs. Connect it to their input pins.	Connect to BATT pin
BATTFET	Driver output for battery path FET M3.	Connected to the base of M3 FET.	If no charging system is required, the pin BATTFET must be floating. When a single path is implemented, it must be connected to Ground

Pin	Description	Typical Connection	Connection if Unused
Charger			
BATTISNS	Battery current sensing point 1. The current flowing out of and into the battery can be read via the ADC by monitoring the voltage drop over the sense resistor between BATT and BATTISNS.	Connect this pin directly to one of the terminals of the 20 mOhm sense resistor.	Connect to BATT pin.
BATT	1. Battery positive terminal. The supply voltage of the battery is sensed through an ADC on this pin. 2. Battery current sensing point 2. The current flowing out of and into the battery can be read via the ADC by monitoring the voltage drop over the sense resistor between BATT and BATTISNS.	This pin must be connected directly to the other terminal of the 20 mOhm sense resistor. Also the positive terminal of the battery must be connected here to charge it and/or supply power to the circuit.	It is mandatory to connect the positive terminal of the battery or power supply on this pin.
BATTISNSCC	Coulomb Counter current sense point.	It should be connected directly to the 0.020 Ohm sense resistor via a separate route from BATTISNS.	Connect to BATT pin
CFP and CFM	Accumulated current filter cap plus and minus terminals respectively.	The coulomb counter will require a 10 μF output capacitor connected between these pins.	Unconnected
CHRGSE1B	This pin is to indicate to the device if the charger is being supplied through a wall charger or USB.	An unregulated wall charger configuration can be built, in which case this pin must be pulled low. When charging through a USB, it can be left open, since it is internally pulled up to VCORE. The recommendation is to place an external FET that can pull it low or leave it open, depending on the charge method.	Unconnected
CHRGLED	Trickle LED driver output 1. Since normal LED control via the SPI bus is not always possible in the standalone operation, a current sink is provided at the CHRGLED pin. This LED is to be connected between this pin and CHRGRAW.	To be connected to the cathode of the charger LED.	Unconnected
GNDCHRG	Ground for charger interface.	Ground	Ground

Typical Connections

Pin	Description	Typical Connection	Connection if Unused
LED Drivers			
GNDBL	Ground for backlighting LED drivers	Ground	Ground
LEDMD, LEDAD, LEDKP	LEDMD: Main display backlight LED driver output. LEDAD: Auxiliary display backlight LED driver output. LEDKP: Keypad lighting LED driver output. Independent programmable current sink channels.	LED strings must be connected from SWLEDOUT (anodes) to these pins (cathodes). When parallel strings are ganged together on a driver channel, ballast resistance is recommended to help balance the currents in each leg.	Unconnected
LEDR, LEDG, and LEDB	General purpose LED driver output Red, Green, and Blue respectively. Each channel provides flexible LED intensity control. These pins can also be used as general purpose open drain outputs for logic signaling, or as generic PWM generator outputs.	These pins are to be connected to the cathodes of the red, green and blue LEDs respectively.	Unconnected
GNDLED	Ground for LED drivers.	Ground	Ground
IC Core			
VCORE	Regulated supply output for the IC analog core circuitry.	Place a 2.2 μF capacitor from this pin to GNDCORE. It will also have to be connected to other pins as reference or for configuration (i.e. PUMSx for initialization configuration).	It is mandatory to place a 2.2 μF capacitor
VCOREDIG	Regulated supply output for the IC digital core circuitry. No external DC loading is allowed on VCOREDIG.	Place a 2.2 μF capacitor from this pin to GNDCORE.	It is mandatory to place a 2.2 μF capacitor
REFCORE	Main bandgap reference. All regulators use the main bandgap as the reference. The main bandgap is bypassed with a capacitor at REFCORE. No external DC loading is allowed on REFCORE.	Place a 0.1 μF capacitor from this pin to GNDCORE.	It is mandatory to place a 0.1 μF capacitor
GNDCORE	Ground for the IC core circuitry.	Ground	Ground

Pin	Description	Typical Connection	Connection if Unused
Power Gating			
PWRGTDRV1 and PWRGTDRV2	PWGTDRV1 is provided for power gating peripheral loads sharing the processor core supply domain(s) SW1, and/or SW2, and/or SW3. In addition, PWGTDRV2 is provided to support power gate peripheral loads on the SW4 supply domain.	The SW1, SW2, and SW3 power gating FET drive would typically be connected to PWGTDRV1 (for parallel NMOS switches). The SW4 power gating FET drive would typically be connected to PWGTDRV2.	Unconnected
Switchers			
SW1IN, SW2IN, SW3IN, and SW4IN	Switchers 1, 2, 3, and 4 input.	Connect these pins to BP to supply Switchers 1, 2, 3, and 4 respectively. Place a 4.7 μF capacitor from each of these pins to GND for decoupling.	Unconnected
SW1FB, SW2FB, SW3FB, and SW4FB	Switchers 1, 2, 3, and 4 feedback. Switchers 1, 2, 3, and 4 output voltage sense respectively.	Connect these pins to the farther point of each of their respective SWxOUT pins, in order to sense and maintain voltage stability.	Ground
SW1OUT	Switcher 1 output. Buck switcher for processor core(s).	Connect this pin to switcher 1 load.	Unconnected
GNDSW1	Ground for switcher 1.	Ground	Ground
SW2OUT	Switcher 2 output. Buck switcher for processor SOG, etc.	Connect this pin to switcher 2 load.	Unconnected
GNDSW2	Ground for switcher 2.	Ground	Ground
SW3OUT	Switcher 3 output. Buck switcher for internal processor memory and peripherals.	Connect this pin to switcher 3 load.	Unconnected
GNDSW3	Ground for switcher 3.	Ground	Ground
SW4OUT	Switcher 4 output. Buck switcher for external memory and peripherals.	Connect this pin to switcher 4 load.	Unconnected
GNDSW4	Ground for switcher 4.	Ground	Ground

Pin	Description	Typical Connection	Connection if Unused
Switchers			
DVS1 and DVS2	Switcher 1 and 2 DVS input pins. Provided for pin controlled DVS on the buck switchers targeted for processor core supplies (SW1 and 2 respectively). When the output voltage of the switchers transition from one voltage to another, its slope is controlled in steps of 25 mV per time step. The DVS pins may be reconfigured for Switcher Increment/Decrement (SID) mode control.	These pins must be set high in order for the DVS feature to be enabled for each of switchers 1 or 2, or low to disable it. These pins are referenced to SPIVCC, a logic one means 0.7*SPIVCC, however, the maximum voltage of these pins is 3.1 V. They are internally pulled low, so the system will interpret that no DVS function is desired when left Unconnected.	Unconnected
SWBSTIN	Switcher BST input. This is the switching node of SWBST.	The 2.2 μH switcher BST inductor must be connected from BP to this pin.	Unconnected
SWBSTOUT	Power supply for gate driver for the internal power NMOS that charges SWBST inductor.	It must be connected to BP.	Unconnected
SWBSTFB	Switcher BST feedback. When SWBST is configured to supply the UVBUS pin in OTG mode, the feedback will be internally switched to sense the UVBUS pin instead of the SWBSTFB.	Connect this pin to the farthest point of SWBSTOUT in order to sense this voltage. Note: No need to connect it to UVBUS since this sensing is made internally when working in OTG mode.	Ground
GNDSWBST	Reference ground for SWBST.	Ground	Ground
Regulators			
VINIOHI	Supply input of VIOHI regulator.	Connect this pin to BP in order to supply VIOHI regulator.	Connect to BP pin
VIOHI	Output regulator for high voltage IO. A fixed 2.775 V output for high voltage level interface.	An output 2.2 μF capacitor is needed from this pin to Ground	Unconnected
VINPLL and VINDIG	Input of regulators for processor PLL and Digital respectively.	VINDIG and VINPLL can be connected either to BP or a 1.8 V switched mode power supply rail (such as from SW4) for the two lower set points of each regulator (1.2 V and 1.25 V output for VPLL, and 1.05 and 1.25 V output for VDIG). In addition, when the two upper set points are used (1.50 and 1.8 V output for VPLL, and 1.65 and 1.8 V for VDIG), they can be connected to either BP or a 2.2 V nominal external switched mode power supply rail to improve power dissipation.	Connect to BP pin
VPLL	Output of regulator for processor PLL. Quiet analog supply (PLL, GPS).	An output 2.2 μF capacitor is needed from this pin to Ground	Unconnected

Pin	Description	Typical Connection	Connection if Unused
Regulators			
VDIG	Output regulator Digital. Low voltage digital (DPLL, GPS).	An output 2.2 μF capacitor is needed from this pin to Ground	Unconnected
VVIDEODRV	Drive output for VVIDEO external PNP transistor.	Connect this pin to the base of the external PNP transistor of VVIDEO in order to drive it.	Unconnected
VVIDEO	Output regulator for TV DAC.	This pin must be connected to the collector of the external PNP transistor of the VVIDEO regulator. An output 2.2 μF capacitor is needed from this pin to Ground	Unconnected
VINAUDIO	VAUDIO regulator input .	Typically connected to BP in order to supply VAUDIO regulator.	Connect to BP pin
VAUDIO	Output regulator for audio supply.	An output 2.2 μF capacitor is needed from this pin to Ground	Unconnected
VINUSB2	Supply input for regulator VUSB2.	Connect this pin to BP in order to supply the VINUSB2 regulator.	Connect to BP pin
VUSB2	Output regulator for powering USB PHY.	An output 2.2 μF capacitor is needed from this pin to Ground	Unconnected
VINCAMDRV	Input of the camera regulator when using the internal pass device and drive output of the VCAM transistor, in case of external PNP pass device.	This regulator has the option of using either internal or external pass device. When using internal pass device, this pin has to be connected to BP in order to supply the VCAM regulator. When using external, this is the pin that drives the PNP transistor, so in must be connected to its base.	Unconnected
VCAM	Output regulator for camera module.	When using external PNP device, this pin must be connected to its collector. An output 2.2 μF capacitor is needed from this pin to ground in both internal and external pass device cases.	Unconnected
VSDDRV	Drive output for VSD external PNP transistor.	Connect this pin to the base of the VSD external PNP in order to drive it.	Unconnected
VSD	Output regulator for multi-media cards, such as micro SD.	This pin must be connected to the collector of the external PNP transistor of the VSD regulator. An output 2.2 μF capacitor is needed from this pin to Ground	Unconnected
VGEN1DRV	Drive output for VGEN1 external PNP transistor.	Connect this pin to the base of VGEN1 external PNP in order to drive it.	Unconnected

Pin	Description	Typical Connection	Connection if Unused
Regulators			
VGEN1	Output of general purpose 1 regulator.	This pin must be connected to the collector of the external PNP transistor of the VGEN1 regulator. An output 2.2 μF capacitor is needed from this pin to Ground	Unconnected
VGEN2DRV	Drive output for VGEN2 external PNP transistor.	Connect this pin to the base of VGEN2 external PNP in order to drive it.	Unconnected
VGEN2	Output of general purpose 2 regulator.	This pin must be connected to the collector of the external PNP transistor of the VGEN2 regulator. An output 2.2 μF capacitor is needed from this pin to Ground	Unconnected
VGEN3DRV	Input for the VGEN3 regulator when internal pass device is used and drive output of VGEN3 transistor in case of external PNP pass device.	This regulator has the option of using either the internal or external pass device. When using the internal pass device, this pin has to be connected to BP in order to supply the VCAM regulator. When using external, this is the pin that drives the PNP transistor, so in must be connected to its base.	Unconnected
VGEN3	Output of general purpose 3 regulator.	When using external PNP device, this pin must be connected to its collector. An output 2.2 μF capacitor is needed from this pin to ground in both internal and external pass device cases.	Unconnected
VSRTC	Output regulator for SRTC module on processor. The VSRTC regulator provides the CLK32KMCU output level (1.2 V). Additionally, it is used to bias the Low Power SRTC domain of the SRTC module, integrated on certain FSL processors.	An output 1.0 μF capacitor is needed from this pin to Ground	It is mandatory to place the 1.0 μF capacitor
GNDREG1	Ground for regulators 1.	Ground	Ground
GNDREG2	Ground for regulators 2.	Ground	Ground
GNDREG3	Ground for regulators 3.	Ground	Ground
GPO1	General purpose output 1.	Intended to be used for battery thermistor biasing. In this case, connect a 10 kOhm resistor from GPO1 to ADIN5, and another one from ADIN5 to GND.	Unconnected
GPO2	General purpose output 2.		Unconnected

Pin	Description	Typical Connection	Connection if Unused
Regulators			
GPO3	General purpose output 3.		Unconnected
GPO4	General purpose output 4. A second general purpose input ADIN7B is available on channel 7 of the ADC. This input is muxed on the GPO4 pin.	On a typical application, a second ambient light sensor is supposed to be connected at ADIN7B (another one should be connected to ADIN7, please check the ADIN7 pin).	Unconnected
Control Logic			
LICELL	Coin cell supply input and charger output. If the main battery is deeply discharged, removed, or contact-bounced (i.e., during a power cut), the RTC system and coin cell maintained logic will switch over to the LICELL for backup power. This pin also works as a current-limited voltage source for battery charging.	The LICELL pin provides a connection for a coin cell backup battery or supercap. A small 0.1 μF capacitor should be placed from LICELL to ground under all circumstances.	0.1 μF capacitor to Ground
XTAL1 and XTAL2	32.768 kHz crystal oscillator connections.	The 32.768 kHz crystal oscillator must be connected between these pins, also an 18 pF capacitor from each pin to ground in this case. The oscillator accepts a clock signal from an external source. This clock signal is to be applied to the XTAL1 pin, the signal can be DC or AC coupled. A capacitive divider can be used to adapt the source signal to the XTAL1 input levels. When applying an external source, the XTAL2 pin is to be connected to VCOREDIG.	Connect XTAL1 to ground and XTAL2 to VCOREDIG pin
GNDRTC	Ground for the RTC block.	Ground	Ground
CLK32K	32 kHz clock output for peripherals. At system startup, the 32 kHz clock is driven to CLK32K (provided as a peripheral clock reference), which is referenced to SPIVCC. CLK32K is restricted to state machine activation in normal On mode.	Connect this pin to the clock input of the peripheral devices of the system.	Unconnected

Pin	Description	Typical Connection	Connection if Unused
Control Logic			
CLK32KMCU	32 kHz clock output for processor. At system startup, the 32 kHz clock is driven to CLK32KMCU (intended as the CKIL input to the system processor) referenced to VSRTC. The driver is enabled by the startup sequencer and CLK32KMCU is programmable for Low Power Off mode control by the state machine.	Connect this pin to the clock input of the MCU.	Unconnected
RESETB and RESETBMCU	Reset output for peripherals and processor respectively. These depend on the Power Control Modes of operation (see the Functional Device Operation section of the datasheet). These are meant as a reset of the processor, or peripherals in a power up condition, or to keep one in reset while the other is up and running.	Connect these pins to the reset input of the peripheral devices and processor respectively. Both need external pull-ups to VIOHI, since they are open drain outputs. If this regulator is not being used, it can be pulled-up to SW4 instead.	Unconnected
WDI	Watchdog input. This pin must be high to stay in On mode. The WDI IO supply voltage is referenced to SPIVCC (typically connected to SW4 = 1.8 V). SPIVCC must therefore remain enabled to allow for proper WDI detection. If WDI goes low, the system will transition to the Off state or Cold Start (depending on the configuration).	This pin has an internal weak pull-down. The recommendation is to place an external transistor, or connect this pin to a processor GPIO, in order to drive it low, with an external pull-up resistor to SPIVCC.	Connect to VCOREDIG pin
STANDBY and STANDBYSEC	Standby input signal from the processor and from peripherals respectively. To ensure that shared resources are properly powered when required, the system will only be allowed into Standby when both the application processor (which typically controls the STANDBY pin) and peripherals (which typically control the STANDBYSEC pin) allow it. The Standby pins are programmable for Active High or Active Low polarity, and that decoding of a Standby event will take into account the programmed input polarities associated with each pin. Since the Standby pin activity is driven asynchronously to the system, a finite time is required for the internal logic to qualify and respond to the pin level changes.	These pins have internal weak pull-downs. The recommendation is to connect them to processor and peripherals GPIOs to drive them high or low.	If only STANDBY is being used, it is recommended to tie STANDBYSEC to STANDBY. If none of them are being used, they can be left Unconnected

Pin	Description	Typical Connection	Connection if Unused
Control Logic			
INT	Interrupt to processor. Unmasked interrupt events are signaled to the processor by driving the INT pin high.	Connect this pin to a processor general purpose input or a pin that interrupts its programming.	Unconnected
PWRON1, 2 and 3	A turn on event can be accomplished by connecting an open drain NMOS driver to the PWRONx pin of the MC13892, so that it is in effect a parallel path for the power key to ground, if it has been programmed for such capability.	These pins have internal pull-ups to VCOREDIG. Grounding of the pins can be accomplished by either a push button, an open drain NMOS, or a processor GPIO.	Unconnected
PUMS1 and PUMS2	Power up mode supply setting. Default startup of the device is selectable by hardwiring the Power Up Mode Select pins. The Power Up Mode Select pins (PUMS1 and 2) are used to configure the startup characteristics of the regulators. Supply enabling and output level options are selected by hardwiring the PUMSx pins for the desired configuration. The power up defaults table below shows the initial setup for the voltage level of the switchers and regulators, and if they get enabled or not, according to the PUMS pins configuration.	Connect these pins to either VCOREDIG, VCORE, GND, or left them open according to the system needs. For further reference please check the following tables.	It is mandatory to select the power up sequence and voltage startup values by hardwiring these pins

i.MX	37/51	37/51	37/51	37/51	35	27/31
PUMS1	**GND**	**Open**	**VCOREDIG**	**VCORE**	**GND**	**Open**
PUMS2	**Open**	**Open**	**Open**	**Open**	**GND**	**GND**
SW1 (1)	0.775	1.050	1.050	0.775	1.200	1.200
SW2 (1)	1.025	1.225	1.225	1.025	1.350	1.450
SW3 (1)	1.200	1.200	1.200	1.200	1.800	1.800
SW4 (1)	1.800	1.800	1.800	1.800	1.800	1.800
SWBST	Off	Off	Off	Off	5.000	5.000
VUSB	3.300 (2)	3.300 (2)	3.300 (2)	3.300 (2)	3.300 (4)	3.300 (4)
VUSB2	2.600	2.600	2.600	2.600	2.600	2.600
VPLL	1.800	1.800	1.800	1.800	1.500	1.500
VDIG	1.250	1.250	1.250	1.250	1.250	1.250
VIOHI	2.775	2.775	2.775	2.775	2.775	2.775
VGEN2	3.150	Off	3.150	Off	3.150	3.150

(1) The switchers SWx are activated in PWM pulse skipping mode, allowed when enabled by the startup sequencer.

(2) USB supply VUSB is only enabled if 5.0 V is present on UVBUS.

(3) The following supplies are not included in the matrix, since they are not intended for activation by the startup sequencer: VCAM, VGEN1, VGEN3, VVIDEO, VAUDIO.

(4) SWBST = 5.0 V powers up and so does VUSB, regardless of 5.0 V present on UVBUS. By default VUSB will be supplied by SWBST.

Tap x 2.0 ms	PUMS2=Open (I,MX37, i.MX51)	PUMS2=GND (i.MX35, i.MX27)
0	SW2	SW2
1	SW4	VGEN2
2	VIOHI	SW4
3	VGEN2	VIOHI
4	SW1	SWBST, VUSB (4)
5	SW3	SW1
6	VPLL	VPLL
7	VDIG	SW3
8		VDIG
9	VUSB (3), VUSB2	VUSB2

(1) Time slots may be included for blocks which are defined by the PUMS pins as disabled to allow for potential activation.

(2) The following supplies are not included in the matrix, since they are not intended for activation by the startup sequencer: VCAM, VGEN1, VGEN3, VVIDEO, VAUDIO. SWBST is not included on the PUMS2=Open column.

(3) USB supply VUSB, is only enabled if 5.0 V is present on UVBUS.

(4) SWBST = 5.0 V powers up and so does VUSB regardless of 5.0 V present on UVBUS. By default VUSB will be supplied by SWBST.

Pin	Description	Typical Connection	Connection if unused
MODE	USB LPB mode, normal mode, and test mode selection is made through this pin. During evaluation and testing, the IC can be configured for normal operation or test mode via the MODE pin.	Ground: Normal operation. VCOREDIG: USB Low Power Boot allowed. VCORE: Test mode.	It is mandatory to select the mode of operation through this pin
GNDCTRL	Ground for control logic.	Ground	Ground
SPIVCC	Supply for SPI bus.	Connect this pin to a 1.75 to 3.1 V voltage source as supply for SPI and I^2C communication pins. (Typically connected to SW4 = 1.8 V)	Mandatory
CS	Chip select pin for SPI communication. This pin is not used in I^2C mode other than for configuration.	CS held low at Cold Start configures interface for SPI mode; once activated, CS functions as the SPI Chip Select. CS tied to VCORE at Cold Start configures interface for I^2C mode. Because the SPI interface pins can be reconfigured for reuse as an I^2C interface, a configuration protocol mandates that the CS pin is held low during a turn on event for the IC (a weak pull down is integrated on the CS pin).	Mandatory
CLK	Primary SPI clock input. In I^2C mode, this pin is the SCL signal (I^2C bus clock).	Connect this pin to either the SPI or I^2C clock pin of the processor.	Mandatory
MOSI	Primary SPI write input. In I^2C mode, the MOSI pin hardwired to ground or VCORE is used to select between two possible addresses (A0 selection).	Connect this pin to the MOSI output of the processor, if working in SPI mode, or to either ground or VCORE when working on I^2C mode.	Mandatory
MISO	Primary SPI read output. In I^2C mode this pin is the SDA signal (bi-directional serial data line).	Connect this pin to the MISO input pin of the processor if working in SPI mode, or to the SDA signal of the processor when working in I^2C mode.	Mandatory
GNDSPI	Ground for SPI interface.	Ground	Ground

USB			
UID	This pin identifies if a mini-A or mini-B style plug has been connected on the application. The state of the ID detection can be read via the SPI to poll dedicated sense bits for a floating, grounded, or factory mode condition on the UID pin.	Please refer to the following table for more information on how to connect the UID pin.	Unconnected

UID Pin External Connection	UID Pin Voltage	Accessory
Resistor to Ground	0.18*VCORE<UID<0.77*VCORE	Non-USB accessory is attached
Grounded	0<UID<0.12*VCORE	A type plug (USB Host)
Floating	0.89*VCORE<UID<VCORE	B type plug (USB peripheral, OTG device or no device) is attached
Voltage Applied	3.6 V<UID (1)	Factory mode
(1) UID maximum voltage is 5.25 V		

Pin	Description	Typical Connection	Connection if unused
UVBUS	USB transceiver cable interface VBUS & OTG supply output. VBUS is defined as the power rail of the USB cable (5.0 V).	Connect this pin to the VBUS of the USB cable. Also short it to CHRGRAW pin if USB charging is allowed on the application.	Unconnected
VUSB	USB transceiver regulator output. This pin is the regulator used to provide a voltage to an external USB transceiver IC.	An output 2.2 μF capacitor is needed from this pin to Ground	Unconnected
VINUSB	Input option for VUSB. This pin is internally connected to the UVBUS pin when in OTG mode operation.	Typically supplied by SWBST. If SWBST is not being used by the application, this pin can be supplied by another 5.0 V source.	Unconnected
VBUSEN	External VBUS enable pin for the OTG supply.	When VBUSEN = 1 (a logic one means more than 0.7*SPIVCC) and VUSBIN = 1 (5.0 V), SWBST will be driving the VBUS, in all other cases, the internal switch from VINUSB to UVBUS will be open. This pin has an internal weak pull-down and its maximum voltage is SPIVCC+0.3 V.	Unconnected

A to D Converter			
ADIN5	ADC generic input channel 5. ADIN5 may be used as a general purpose unscaled input but in a typical application, ADIN5 is used to read out the battery pack thermistor. The thermistor will have to be biased with an external pull-up resistor to a voltage rail greater than the ADC input range. In order to save current when the thermistor reading is not required, it can be biased from one of the general purpose IO's such as GPO1.	When used for reading the battery pack thermistor, a 10 kOhm resistor should be placed from GPO1 to ADIN5, and another one from ADIN5 to ground, in order to assure the resulting voltage falls within the ADC input range. The battery pack thermistor should be connected at this pin.	Unconnected
ADIN6	ADC generic input channel 6.	ADIN6 may be used as a general purpose unscaled input but in a typical application, the PA thermistor is connected here.	Unconnected
ADIN7	ADC generic input channel 7.	ADIN7 may be used as a general purpose unscaled input or as a divide by 2 scaled input. In a typical application, an ambient light sensor is connected here.	Unconnected
TSX1, TSX2, TSY1 and TSY2	Touch Screen Interface X1 and X2, Y1 and Y2. In inactive mode, these pins can be also used as general purpose ADC inputs (see Touch Screen Interface section in the data sheet), they are respectively mapped on ADC channels 4, 5, 6 and 7.	The touch screen X plate is connected to TSX1 and TSX2 while the Y plate is connected to Y1 and Y2. In interrupt mode, a voltage is applied to the X-plate (TSX2) via a weak current source to VCORE, while the Y-plate is connected to ground (TSY1).	Unconnected
A to D Converter			
TSREF	Touch Screen Reference regulator. This regulator is powered from VCORE.	Connect a 2.2 μF capacitor from this pin to Ground In applications not supporting touch screen at all, the TSREF can be used as a low current general purpose regulator.	Unconnected (the bypass capacitor can be omitted)
ADTRIG	ADC trigger input. A rising edge on this pin will start an ADC conversion.	This rising edge can be produced by either a push button, a FET connected to this pin, or a GPIO from the processor. This pin has an internal weak pull-down and a voltage from 1.0 to 3.6 V is interpreted as a logic 1.	Unconnected
GNDADC	Ground for A to D circuitry.	Ground	Ground
Thermal Grounds			
GNDSUB	Non critical signal grounds and thermal heat sinks.	Big ground plane for thermal dissipation.	Big ground plane for thermal dissipation

5 References

1. MC13892 Datasheet

6 Revision History

REVISION	DATE	DESCRIPTION OF CHANGES
3.0	1/2011	• Added revision history page
	4/2013	• No technical changes. Revised back page. Updated document properties.

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