

KIT34700EPEVBE Evaluation Board

Table of Contents

| | |
|---------------------------------------|----|
| Kit Contents / Packing List | 2 |
| Notification / Disclaimer | 3 |
| Kit Introduction | 4 |
| Required Equipment | 5 |
| EVB Setup Configuration Diagram | 6 |
| Using Hardware | 7 |
| Schematic | 11 |
| Board Layout | 12 |
| Bill of Material | 19 |
| References | 21 |
| Revision History | 22 |

List of Figures

| | |
|---------------------------------------|----|
| EVB Setup Configuration Diagram | 6 |
| EVB Schematic | 11 |
| Assembly Top | 12 |
| Assembly Bottom | 13 |
| Top | 14 |
| Gnd Layer 2 | 15 |
| Power Layer 3 | 16 |
| Bottom | 17 |
| Drill Location | 18 |

List of Tables

| | |
|----------------------------|----|
| Board Configuration | 4 |
| Output Current | 4 |
| Jumper Configuration | 8 |
| Bill of Material | 19 |

1 Kit Contents / Packing List

- Evaluation Board - KIT34700EPEVBE
- Hardware Document CD, CD34700

2 Important Notice

Freescale provides the enclosed product(s) under the following conditions:

This evaluation kit is intended for use of ENGINEERING DEVELOPMENT OR EVALUATION PURPOSES ONLY. It is provided as a sample IC pre-soldered to a printed circuit board to make it easier to access inputs, outputs, and supply terminals. This EVB may be used with any development system or other source of I/O signals by simply connecting it to the host MCU or computer board via off-the-shelf cables. This EVB is not a Reference Design and is not intended to represent a final design recommendation for any particular application. Final device in an application will be heavily dependent on proper printed circuit board layout and heat sinking design as well as attention to supply filtering, transient suppression, and I/O signal quality.

The goods provided may not be complete in terms of required design, marketing, and or manufacturing related protective considerations, including product safety measures typically found in the end product incorporating the goods. Due to the open construction of the product, it is the user's responsibility to take any and all appropriate precautions with regard to electrostatic discharge. In order to minimize risks associated with the customers applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards. For any safety concerns, contact Freescale sales and technical support services.

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3 Kit Introduction

The MC34700 is a four output DC to DC regulator for multi-rail applications. The Evaluation Board is designed to provide the user with the ability to configure the part using a single 9V to 18V input supply, a dual supply, or with each regulator supplied individually. The Evaluation Board has three buck regulators that are setup for outputs of 3.3V at 1.5A, 2.5V at 1.25A and 1.25V at 1.25A and an LDO with a 0.9V at 400mA output. Inputs to enable each output channel are provided as well as a Power Good LED indicator.

| Channel | Input | Vout | Iout(max) |
|---------|---------|--------|-----------|
| DC/DC 1 | VIN1 | 3.3 V | 1.5 A |
| DC/DC 2 | VIN2 | 2.5 V | 1.25 A |
| DC/DC 3 | VIN3 | 1.25 V | 1.25 A |
| LDO | VIN_LDO | 0.9 V | 400 mA |

When operating from a single input supply be aware that CH2 and CH3 are run off the output of CH1 and that the LDO is run off the output of CH3. As a result, the output current available from CH1 is not the full 1.5A, but the current remaining after supplying VIN2 and VIN3. Similarly the current available for CH3 is not the full 1.25A.

| Channel | Input | Vout | Iout(max) |
|---------|-------|--------|---|
| DC/DC 1 | VIN1 | 3.3 V | $1.5 \text{ A} - ((V_{out2} * I_{out2}) + (V_{out3} * (I_{out3} + I_{out \text{ LDO}}))) / (V_{out1} * 0.85)$ |
| DC/DC 2 | VOUT1 | 2.5 V | 1.25 A |
| DC/DC 3 | VOUT1 | 1.25 V | 1.25A - Iout LDO |
| LDO | VOUT3 | 0.9 V | 400 mA |

4 Required Equipment

The following equipment is required to power and make measurements on the MC34700:

- a) Power Supply, 9V to 18V adjustable, capable of 2A output current (required).
- b) Power Supply, 1.5V to 6V adjustable, capable of 3A output current (optional).
- c) Digital Multi-Meter, Agilent 34401A, 6 1/2 digit, or equivalent (required).
- d) Oscilloscope, 4 Channel, 500 MHz bandwidth, or equivalent (required).
- e) DC Electronic Load, Agilent 6060B, 0V to 6V, capable of 5A, or equivalent (required).
- f) DC Current Probe (optional)

5 EVB Setup Configuration Diagram

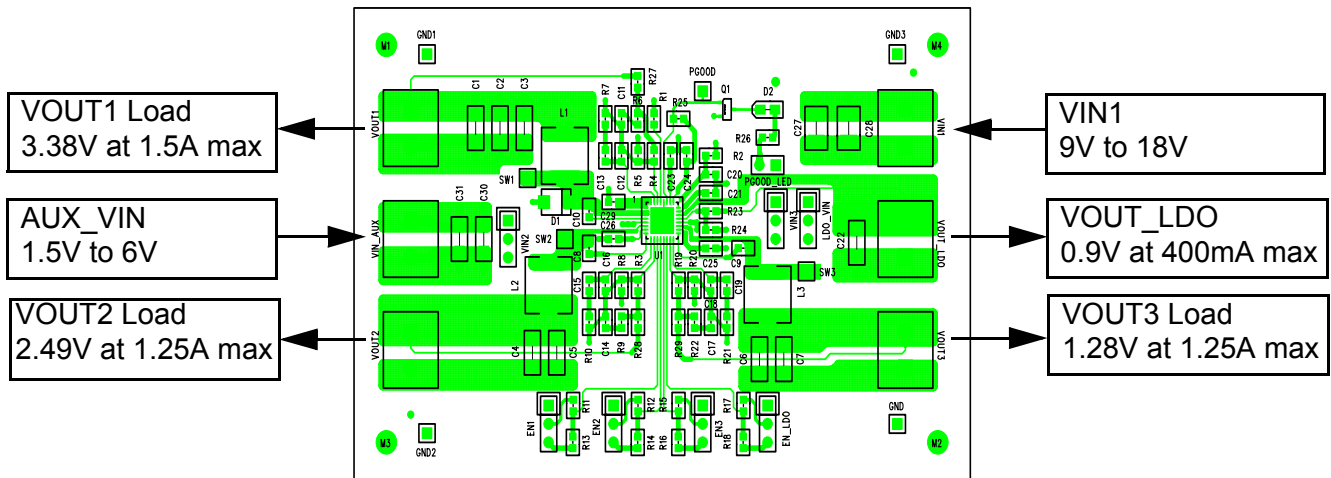


Figure 1. EVB Setup Configuration Diagram

6 Using the Hardware

Use the following steps to verify that the Evaluation Board is operational:

- a) Verify jumpers are installed as shown in Jumper Connections Section. Use the default settings.
- b) Check polarity and connect a 12V, 2A supply to VIN1 terminal.
- c) Check 12V supply current with all the regulators disabled. The supply current should not exceed 15mA.
- d) Enable CH1 by moving EN1 jumper to 1-2 position. Verify 3.3V channel is operating by measuring voltage at VOUT1 terminal. VOUT1 is typically 3.38V.
- e) Enable CH2 by moving the EN2 jumper to the 1-2 position. Verify the 2.5V channel is operating by measuring the voltage at the VOUT2 terminal. VOUT2 is typically 2.49V.
- f) Enable CH3 by moving EN3 jumper to 1-2 position. Verify that the 1.25V channel is operating by measuring the voltage at the VOUT3 terminal. VOUT3 is typically 1.28V.
- g) Enable LDO by moving EN_LDO jumper to 1-2 position. Verify 0.9V channel is operating by measuring voltage at VOUT_LDO terminal. VOUT_LDO is typically 0.9V.
- h) If all the regulators are up and running, verify that the PGOOD LED (D2) is on.

After board verification, it can be reconfigured and tested per system requirements.

6.1 Jumper Connections

A description of the jumper settings is given in the following table.

| Jumper | Position | Default | Description |
|-----------|---------------|---------|--|
| EN1 | 1-2 2-3 | X | DC/DC 1 ENABLED DC/DC 1 DISABLED |
| EN2 | 1-2 2-3 | X | DC/DC 2 ENABLED DC/DC 2 DISABLED |
| EN3 | 1-2 2-3 | X | DC/DC 3 ENABLED DC/DC 3 DISABLED |
| EN_LDO | 1-2 2-3 | X | LDO ENABLED LDO DISABLED |
| VIN2 | 1-2 2-3 | X | VIN2 CONNECTED TO VOUT1 VIN2 CONNECTED TO VIN_AUX |
| VIN3 | 1-2 2-3 | X | VIN3 CONNECTED TO VOUT1 VIN3 CONNECTED TO VIN_AUX |
| LDO_VIN | 1-2 2-3 | X | LDO_VIN CONNECTED TO VOUT3 LDO_VIN CONNECTED TO VIN_AUX |
| PGOOD_LED | SHORT OPEN | X | LED is active, running off VOUT1 LED is disconnected |

6.2 PGOOD

The evaluation board includes a status LED (D2), that indicates all the regulators are operating and no faults have occurred. The FET, Q1, is required for signal inversion and to drive the LED current. The resistor, R26, limits the LED current.

The jumper (PGOOD_LED) disconnects the status LED for making efficiency and quiescent current measurements. The status LED is connected to the output of CH1 when the jumper is installed.

The test point PGOOD is the open drain output of the PGOOD pin. It is pulled up to VGREG by resistor R25.

6.3 Switch Nodes

The evaluation board includes test points for monitoring the switch nodes of DC/DC 1, 2 and 3. The test points are located close to the output inductors of each channel. The switch nodes can be used to measure switching frequency, duty cycle, phase, and switch times.

6.4 Power Input Voltage

The power input voltage for DC/DC1 (VIN1) is connected to the VIN1 terminal block. The VIN1 input is bypassed with bulk capacitors C27 and C28, and is connected to the IC input pin (VIN) by an RC filter, R2 and C20.

Power inputs for DC/DC 2, and DC/DC 3 (VIN2, and VIN3) can be connected to the AUX_IN terminal or the output of DC/DC 1. By setting the jumpers (VIN2, and VIN3) to position 2-3, each regulator can be powered from the AUX_IN. By setting the jumpers to position 1-2, each regulator can be powered from the output of DC/DC 1.

The power input voltage for the LDO (LDO_VIN) can be connected to the AUX_IN terminal or the output of DC/DC 3. By setting the jumper (LDO_VIN) to position 2-3, the LDO can be powered from the AUX_IN. By setting the jumper to position 1-2, the LDO can be powered from the output of DC/DC 3. The AUX_IN input is bypassed with bulk capacitors C30 and C31.

For single supply operation, set VIN2, VIN3 and LDO_VIN to position 1-2. This connects the input of DC/DC 2 and DC/DC 3 to the output of DC/DC 1 and the LDO input to the output of DC/DC 3.

For dual supply operation, set VIN2, and VIN3 to position 2-3. This connects the input of DC/DC 2 and DC/DC 3 to the AUX_IN terminal block. Set the LDO_VIN to either position depending on the application to connect the LDO input to the output of DC/DC 3 or the AUX_IN terminal.

If each regulator needs to be powered from a separate supply, two of the input power jumpers can be removed and an external supply connected directly to header position 2. Select

the regulators with the lowest output power to connect directly to the header pin. The other two regulators are powered from VIN1 and AUX_IN.

6.5 Enables and Cascaded Sequencing

The enable headers are currently configured for a simple enable/disable function. Setting the jumper to position 1-2 connects the enable pin to the VGREG output, enabling the respective regulator. Removing or setting the jumper to position 2-3 connects the enable pin to ground, disabling the respective regulator.

However, the board has provisions to add a resistor divider to each enable pin which allows cascaded sequencing. Resistors R11, R12, R15, and R17 are installed and are 10K Ohm. By installing resistors R13, R14, R16, and R18 a voltage divider is formed at each enable pin. By setting the resistor divider of each enable, the voltage of the enable pin has to reach its' threshold level before the regulator in the sequence is enabled. Note that the jumpers need to be removed and the output of the regulator in the previous sequence position be connected to pin 2 of the enable header. See the data sheet for more details on calculating the divider.

6.6 Leakage Current

DC/DC 2 and DC/DC 3 each have ~400uA of leakage current that can cause the output to float up if there is not enough load current in the application. 1K Ohm resistors are installed at R36 and R37 (located on the bottom side of the PC board) to prevent VOUT2 and VOUT3 from floating when these channels are disabled.

The 1K load can be removed if there is a minimum load of at least 4mA present on VOUT2 and VOUT3.

7 EVB Schematic

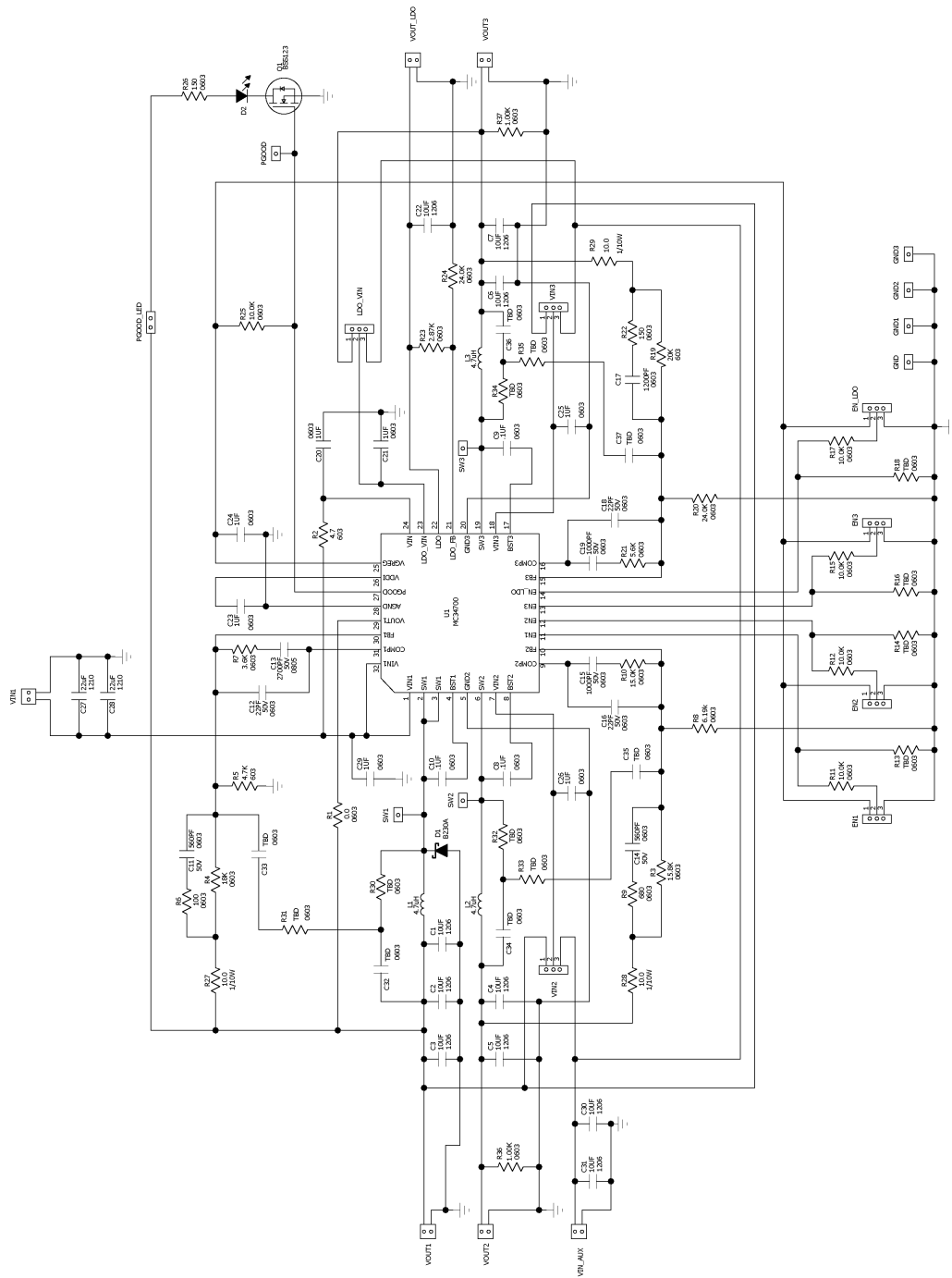


Figure 2. EVB Schematic

8 Board Layout

8.1 Assembly Layer Top

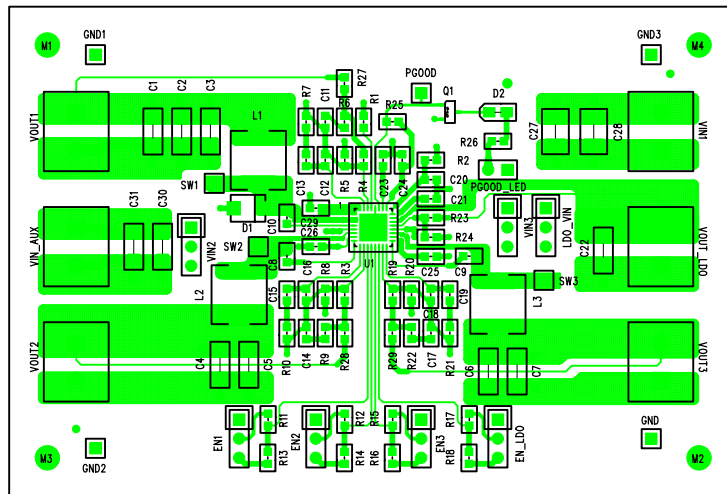


Figure 3. Assembly Layer Top

8.2 Assembly Layer Bottom

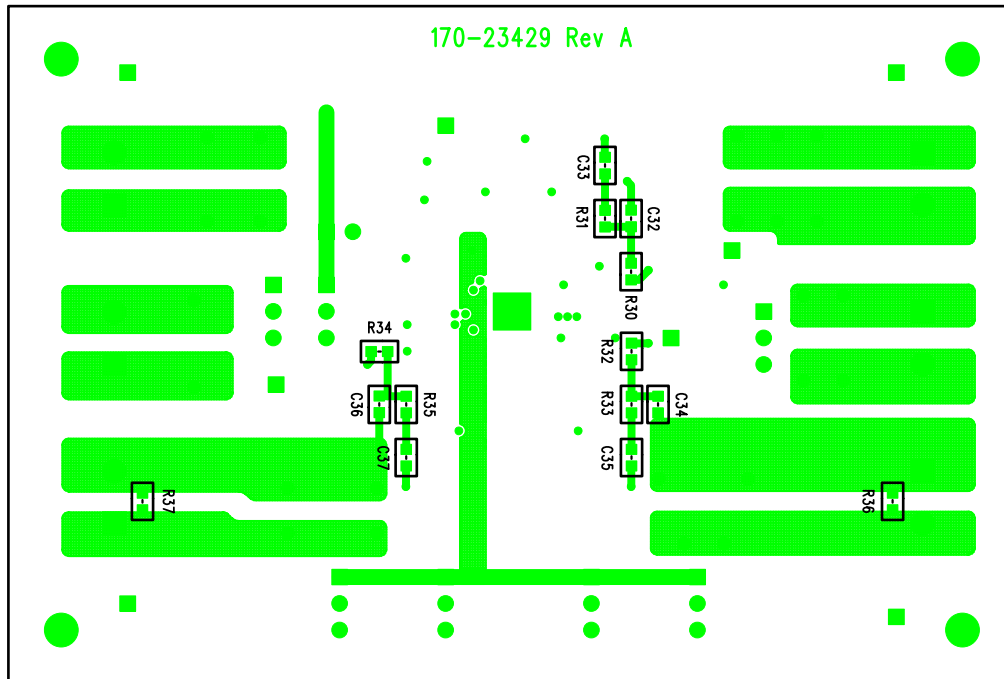


Figure 4. Assembly Layer Bottom

8.3 Top Layer Routing

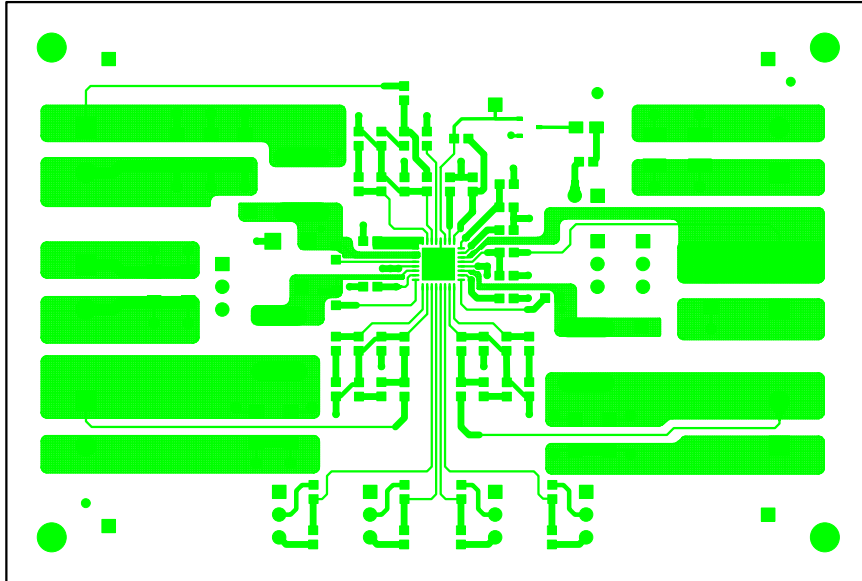


Figure 5. Top Layer Routing

8.4 Inner Layer 2 Routing

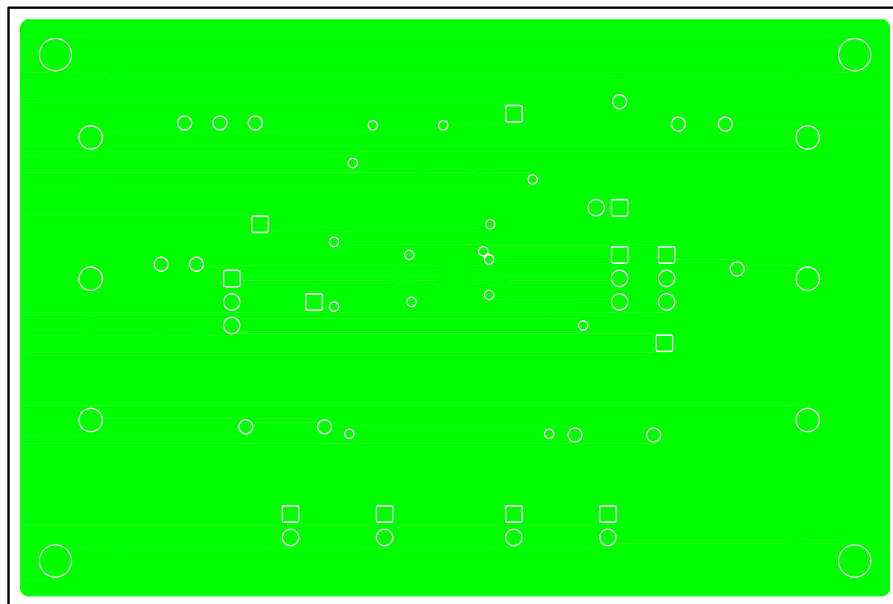


Figure 6. Inner Layer 2 Routing

8.5 Inner Layer 3 Routing

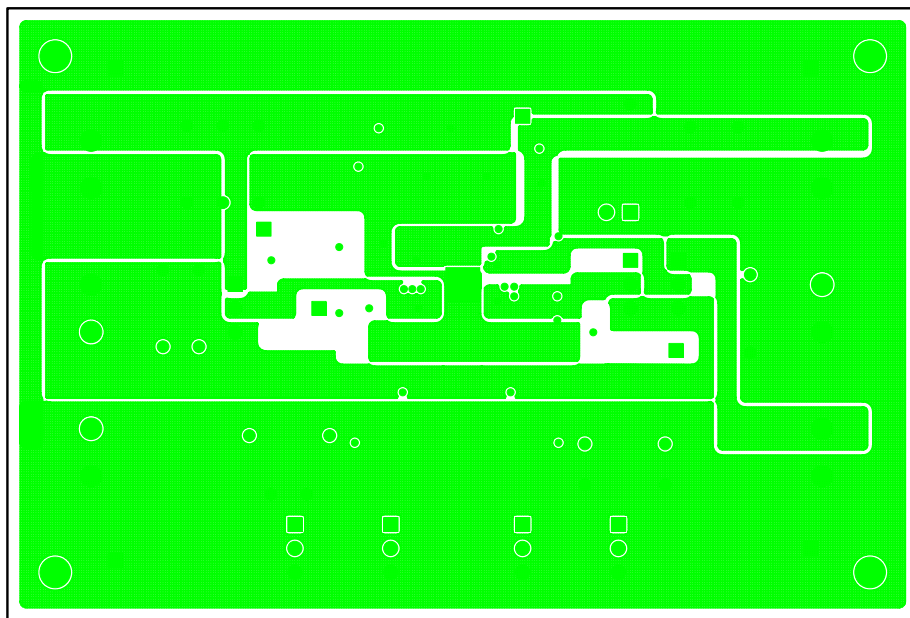


Figure 7. Inner Layer 3 Routing

8.6 Bottom Layer Routing

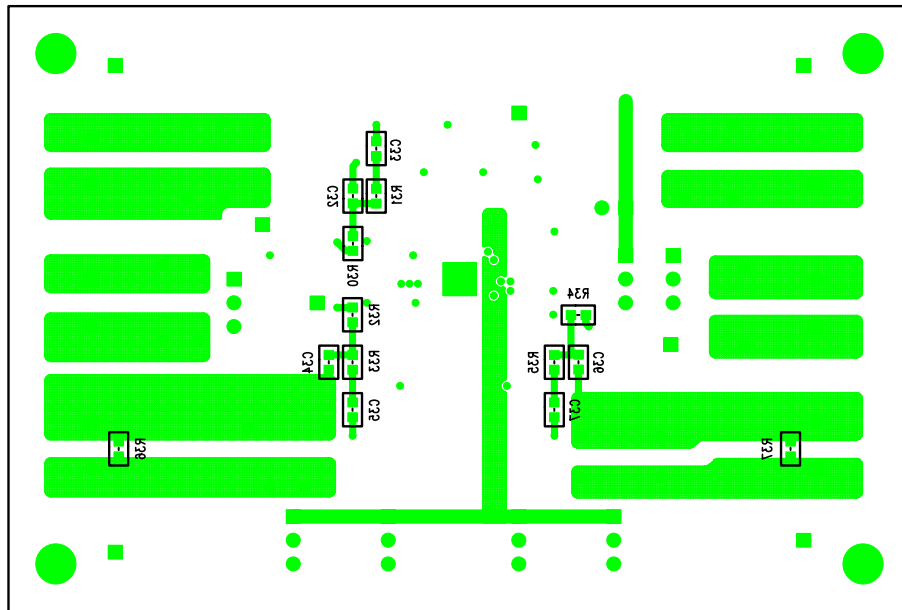


Figure 8. Bottom Layer Routing

8.7 Drill Location

NOTES: (UNLESS OTHERWISE SPECIFIED)

1. BOARD SUBSTRATE FR4 06 T_g IS GREATER THAN OR EQUAL TO 170 DEG C.
2. FINISHED BOARD THICKNESS 0.062" +/- 0.006".
3. PLATING:
GOLD IMMERSION
4. SOLDER MASK: USE LPI BOTH SIDES
MEDIUM GREEN, SEMI-GLOSS, HIGHLY TRANSPARENT.
5. BOARD FINISH ENIG.
6. CU WEIGHT 1.0 OZ ALL LAYERS
7. SILK LEGEND WHITE EPOXY INK BOTH SIDES
8. FINISHED DRILL HOLE DIAMETER +/- 0.003" FROM TRUE

| SIZE | QTY | SYM | PLATED | TOL |
|-------|-----|----------------|--------|----------|
| 15 | 32 | + ^B | YES | +/-0.003 |
| 128 | 4 | + ^F | NO | +/-0.0 |
| 37 | 31 | + ^G | YES | +/-0.0 |
| 11.81 | 9 | + ^H | YES | +/-0.0 |
| 60 | 12 | + ^I | YES | +/-0.0 |
| 28 | 25 | + ^J | YES | +/-0.0 |

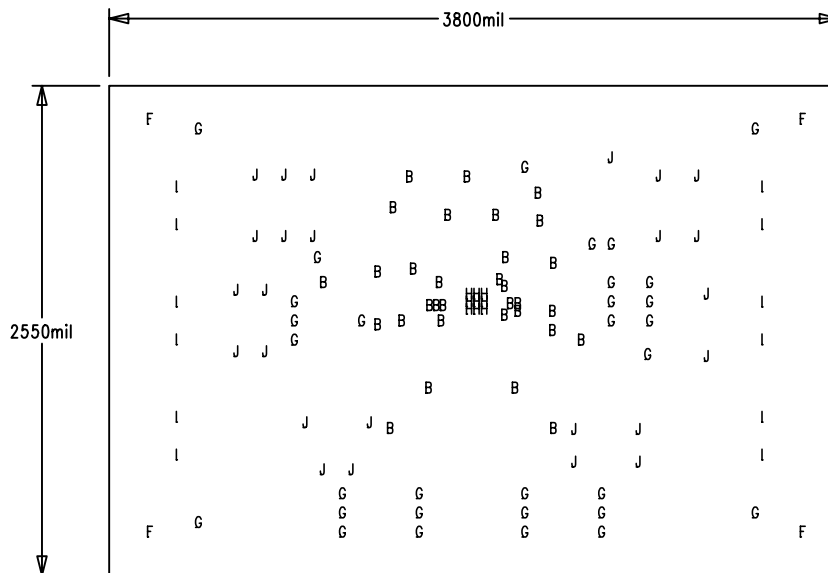
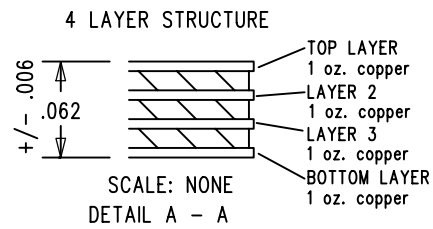


Figure 9. Drill Location

9 Bill of Material

| Reference Designation | Value | Qty | Description | Mfr | PN |
|---------------------------------|---------|-----|-----------------------------------|-------------|--------------------|
| Freescale Components | | | | | |
| U1 | MC34700 | | Four output, integrated regulator | Freescale | MC34700EP |
| Capacitors | | | | | |
| C1-C7, C22,C30, C31 | 10uF | 10 | CAP, CER, 10uF, 10V, X5R | TDK | C3216X5R1A106M |
| C8,C9, C10 | 0.1uF | 3 | CAP, CER, 0.1uF, 25V, X7R | TDK | C1608X7R1E104K |
| C11, C14 | 560pF | 2 | CAP, CER, 560pF, 50V, COG | Panasonic | ECJ-1VC1H561J |
| C12,C16, C18 | 22pF | 3 | CAP, CER, 22pF, 50V, COG | Panasonic | ECJ-1VC1H220J |
| C13 | 2.7nF | 1 | CAP, CER, 2700pF, 50V, X7R | Panasonic | ECJ-1VB1H272K |
| C15,C19 | 1000pF | 2 | CAP, CER, 1000pF, 50V, X7R | Panasonic | ECJ-1VB1H102K |
| C17 | 1.2nF | 1 | CAP, CER, 1200pF, 50V, X7R | Murata | GRM188R71H122KA01D |
| C20,C21, C23-C26, C29 | 1.0uF | 7 | CAP, CER, 1.0uF, 25V, X5R | Murata | GRM188R61E105KA12D |
| C27,C28 | 22uF | 2 | CAP, CER, 22uF, 25V, X5R | Murata | GRM32ER61E226KE15L |
| C32-C37 | | | Not Populated | | |
| Resistors | | | | | |
| R1 | 0 Ohm | 1 | RES, 0.0 Ohm, 1/10W, 5% | Vishay/Dale | CRCW06030000Z0EA |
| R2 | 4.7 Ohm | 1 | RES, 4.7 Ohm, 1/10W, 1% | Vishay/Dale | CRCW06034R70FNEA |
| R3 | 15.8K | 1 | RES, 15.8K Ohm, 1/10W, 1% | Yageo | RC0603FR-0715K8L |
| R4 | 18.0K | 1 | RES, 18.0K Ohm, 1/10W, 1% | Yageo | RC0603FR-0718K8L |
| R5 | 4.7K | 1 | RES, 4.70K Ohm, 1/10W, 1% | Yageo | RC0603FR-074K7L |
| R6 | 200 Ohm | 1 | RES, 200 Ohm, 1/10W, 1% | Yageo | RC0603FR-07200RL |
| R7 | 3.60K | 1 | RES, 3.60K Ohm, 1/10W, 1% | Yageo | RC0603FR-073K6L |
| R8 | 6.19K | 1 | RES, 6.19K Ohm, 1/10W, 1% | Yageo | RC0603FR-076K19L |
| R9 | 680 Ohm | 1 | RES, 680 Ohm, 1/10W, 1% | Yageo | RC0603FR-07680RL |
| R10 | 15.0K | 1 | RES, 680 Ohm, 1/10W, 1% | Yageo | RC0603FR-0715KL |
| R11,R12, R15,R17, R24,R25 | 10.0K | 6 | RES, 680 Ohm, 1/10W, 1% | Vishay/Dale | CRCW060310K0FKEA |
| R13,R14, R16,R18 | | | Not Populated | | |
| R19 | 20.0K | 1 | RES, 20.0K Ohm, 1/10W, 1% | Yageo | RC0603FR-0720KL |
| R20 | 24.0K | 1 | RES, 24.0K Ohm, 1/10W, 1% | Yageo | RC0603FR-0724KL |
| R21 | 5.60K | 1 | RES, 5.60K Ohm, 1/10W, 1% | Yageo | RC0603FR-075K6L |
| R22,R26 | 150 Ohm | 2 | RES, 150 Ohm, 1/10W, 1% | Vishay/Dale | CRCW0603150RFKEA |
| R23 | 2.87K | 1 | RES, 2.87K Ohm, 1/10W, 1% | Yageo | RC0603FR-072K87L |
| R27-R29 | 10 Ohm | 3 | RES, 150 Ohm, 1/10W, 1% | Vishay/Dale | CRCW060310R0FKEA |
| R30-R35 | | | Not Populated | | |
| R36, R37 | 1.00K | 2 | RES, 1.00K Ohm, 1/10W, 1% | Yageo | RC0603FR-071K00L |

| Reference Designation | Value | Qty | Description | Mfr | PN |
|---|--------|-----|---|--------------|----------------------------------|
| Connectors | | | | | |
| EN1-EN3, EN_LDO, VIN_LDO, VIN2,VIN3 | | 7 | HEADER, 3 x 1, single row, 2.54mm, gold flash, head = 0.230", tail = 0.120" | Sullins | PBC36SAAN |
| GND, PGOOD,S W1-SW3, GND1-GN D3 | | 8 | HEADER, 1 x 1, straight pin, 2.54mm, gold flash, head = 0.230", tail = 0.120" | Sullins | PBC36SAAN |
| PGOOD_ LED | | 1 | HEADER, 1 x 2, single row, 2.54mm, gold flash, head = 0.230", tail = 0.120" | Sullins | PBC36SAAN |
| VIN1, VIN_AUX VOUT1 - VOUT3, VOUT_ LDO | | 6 | TERMINAL BLOCK, 300V, 16A, 28-12AWG | Phoenix | MKSDN 1.5/2 |
| EN1-EN3, EN_LDO, VIN_LDO, VIN2,VIN3 PGOOD_ LED | | 8 | Shorting Jumper, gold flash | Sullins | SPC02SYAN |
| Misc. | | | | | |
| L1, L2,L3 | 4.7uH | 3 | INDUCTOR, 4.7uH, 2.9A, 35mOhm, 7.3 x 7.3 x 3.2mm | TDK Würth | RLF7030T-4R7M3R4 744 778 9004 |
| D1 | B230 | 1 | DIODE, Schottky, 30V, 2A, SMA | Diodes, Inc | B230A-13-F |
| D2 | LED | 1 | LED, Red, Vf = 1.8V, 30mA, 100mW | Lumex | SML-LXT0805SRW-TR |
| Q1 | BSS123 | 1 | N-MOSFET, BSS123, 100V, 170mA | Fairchild | BSS123 |

Freescale does not assume liability, endorse, or warrant components from external manufacturers that are referenced in circuit drawings or tables. While Freescale offers component recommendations in this configuration, it is the customer's responsibility to validate their application

10 References

Following are URLs where you can obtain information on other Freescale products and application solutions:

| Description | URL |
|--|--|
| Data Sheet - MC34700 | www.freescale.com/files/analog/doc/data_sheet/MC34700.pdf |
| Fact Sheet - MC34700FS | |
| Application Note - Low Power Management Unit with MC34700 AN3592 | www.freescale.com/files/microcontrollers/doc/app_note/AN3592.pdf |
| Application Note - Quad Flat Pack No-Lead (QFN) AN1902 | www.freescale.com/files/analog/doc/app_note/AN1902.pdf |
| Freescale's Web Site | www.freescale.com |
| Freescale's Analog Web Site | www.freescale.com/analog |
| Freescale's Power Management Web Site | www.freescale.com/powermanagement |

11 Revision History

| REVISION | DATE | DESCRIPTION OF CHANGES |
|----------|--------|---|
| 1.0 | 7/2008 | <ul style="list-style-type: none">Initial Release |

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Technical Information Center
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Japan:

Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
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support.japan@freescale.com

Asia/Pacific:

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