Freescale Semiconductor
Users Guide

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Using the 5.0 A 1.0 MHz Fully Integrated Dual Switch-Mode Power Supply (KIT34717EPEVBE)

1 Introduction

This User's Guide will help the designer get better acquainted with the 34717 IC and Evaluation board. It contains a procedure to configure each block of the 34717 in a practical way, which is based on a working Evaluation Board designed by Freescale (KIT34717EPEVBE).

2 34717 Specification

The 34717 is a highly integrated, space efficient, low cost, dual synchronous buck switching regulator with integrated N-channel power MOSFETs. It is a high performance dual point-of-load (PoL) power supply with many desired features for the 3.3 V and 5.0 V environments.

Both channels can provide up to 5.0 A of continuous output current capability with high efficiency and tight output regulation. The second channel has the ability to track an external reference voltage in different configurations.

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3 Application Diagram

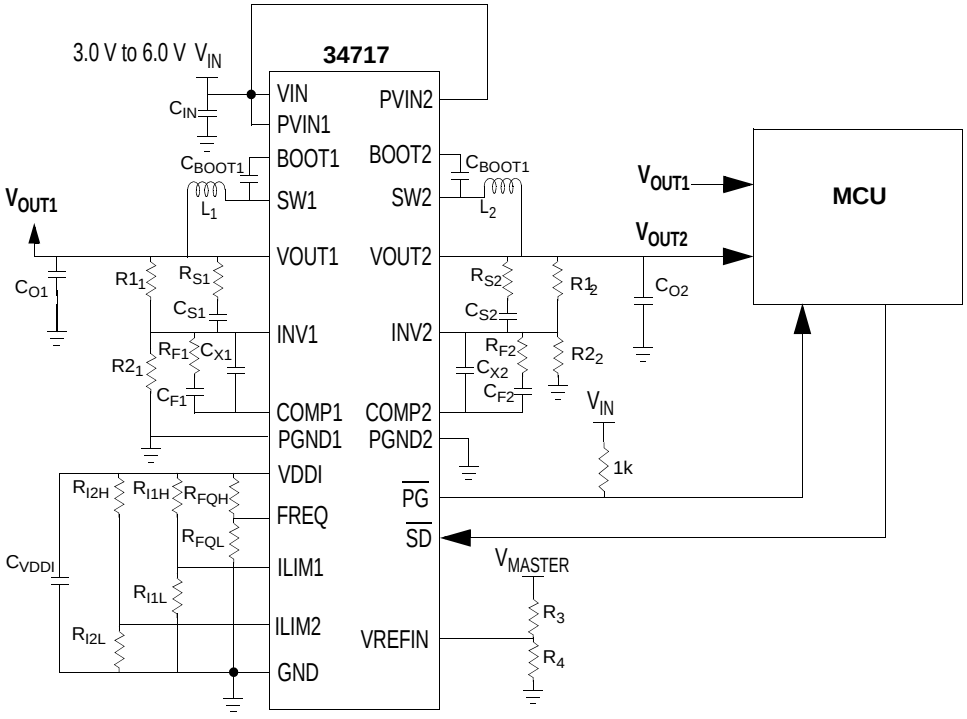

Figure 1. Application diagram for 34717

4 Board's Specifications

The Board was designed to have an operating range defined by:

Channel #1		Channel #2	
PV_{IN_MAX}	6.0 V	PV_{IN_MAX}	6.0 V
PV_{IN_MIN}	3.0 V	PV_{IN_MIN}	3.0 V
V_{OUT_MAX}	3.6 V	V_{OUT_MAX}	3.6 V
V_{OUT_MIN}	0.7 V	V_{OUT_MIN}	0.7 V
I_{OUT_MAX}	5.0 A	I_{OUT_MAX}	5.0 A
I_{OUT_MIN}	0.0 A	I_{OUT_MIN}	0.0 A

5 Component Selection for 34717 Eval Board

5.1 I/O Parameters:

VIN = P_{VIN1} = P_{VIN2} = 5.0V
FSW = 1 MHz
V_{OUT1} = 1.8 V
I_{OUT1} = 5.0 A
V_{OUT1} = 1.5 V
I_{OUT2} = 5.0 A
VREFIN =V_{OUT1}

5.2 Configuring the Output Voltage:

Both channels for the 34717 are General purpose DC-DC converter, the resistor divider to the INV node is the responsible for setting the output voltage. The equation is:

$$V_{OUT} = V_{REF}\left(\frac{R1}{R2}+1\right)$$

For channel 1: V_{REF} = V_{BG} = 0.7V.

For channel 2: The second channel of 34717 has an internal reference selector, thus V_{REF} can be either the voltage at the VREFIN terminal, or the internal reference voltage V_{BG}. The reference value is given by the following condition: V_{REF} = VREFIN if VREFIN is less than V_{BG} = 0.7V. Otherwise, V_{REF} = V_{BG}. Usually the output regulation voltage is calculated using the internal reference V_{BG}, and the condition V_{REF} = VREFIN is used for tracking purposes.

Then, for channel 1 at 1.8 V, we choose R1 = 20KΩ and R2 is calculated.

$$R2 = \frac{V_{REF}R1}{V_{OUT}-V_{REF}} = 12.78K\Omega$$

And for channel 2 at 1.5V and R1 = 20KΩ, R2 is calculated as follows:

$$R2 = \frac{V_{REF}R1}{V_{OUT}-V_{REF}} = 17.5K\Omega$$

5.3 Switching Frequency Configuration

The switching frequency will have a value of 1.0 MHz by connecting the FREQ terminal to the GND. If the smallest frequency value of 200 KHz is desired, then connect the FREQ terminal to VDDI. To program the switching frequency to another value, an external resistor divider will be connected to the FREQ terminal to achieve the voltages given by the Frequency Selection Table.

Frequency KHz	Voltage applied to pin FREQ [V]
200	2.341 – 2.500
253	2.185 - 2.340
307	2.029 - 2.184
360	1.873 - 2.028
413	1.717 – 1.872
466	1.561 – 1.716
520	1.405 - 1.560
573	1.249 - 1.404
627	1.093 - 1.248
680	0.936 - 1.092
733	0.781 - 0.936
787	0.625 - 0.780
840	0.469 - 0.624
893	0.313 - 0.468
947	0.157 - 0.312
1000	0.000 - 0.156

Table 1. Frequency Selection Table

The EVB frequency is set to 1 MHz, connecting the FREQ terminal directly to GND.

5.4 Selecting Inductor

Inductor calculation process is the same for both Channels. The equation is the following:

$$L = D'_{MAX} * T * \frac{(V_{OUT} + I_{OUT} * (Rds(on)\_ls + r\_w))}{\Delta I_{OUT}}$$

$D'_{MAX} = 1 - \frac{V_{OUT}}{Vin\_\max}$ Maximum Off time percentage

$T = 1\mu s$ Switching period

$Rds(on)\_ls = 45m\Omega$ Drain – to – source resistance of FET

$r\_w = 10m\Omega$ Winding resistance of Inductor

$\Delta I_{OUT} = 0.4 * I_{OUT}$ Output current ripple

$L1 = 0.72uH$ and $L2 = 0.75uH$

However, since channel 1 can serve as power supply for channel 2, we have to locate the LC poles at different frequencies in order to ensure that the input impedance of the second converter is always higher than the output impedance of the first converter and thus ensure system stability. To move the LC poles, we can select different values of “L” for each channel, for instance, L1 = 1.0μH and L2 = 1.5μH, to allow some operating margin for each channel.

5.5 Input Capacitors for PVIN1 and PVIN2

Input capacitor selection process is the same for both channels, and should be based on the current ripple allowed on the input line. The input capacitor should provide the ripple current generated during the inductor charge time. This ripple is dependent on the output current sourced by 34717 so that:

$$I_{RMS} = I_{OUT}\sqrt{D(1-D)}$$

Where:

$I_{RMS}$is the RMS value of the input capacitor current.

$I_{OUT}$is the output current,

D= V_{OUT}/Vinis the duty cycle.

For a buck converter, I_{RMS} has its maximum at PVIN = $2V_{OUT}$

Since

$$I_{RMS\_MAX} = \sqrt{\frac{P_{MAX}}{ESR}}$$

Where P_{MAX} is the maximum power dissipation of the capacitor and is a constant based on physical size (generally given in the datasheets under the heading AC power dissipation.). We derive that the lower the ESR, the higher would be the ripple current capability. In other words, a low ESR capacitor (i.e., with high ripple current capability) can withstand high ripple current levels without overheating.

Therefore, for greater efficiency and because the overall voltage ripple on the input line also depends on the input capacitor ESR, we recommend using low ESR capacitors.

$$Cin_{MIN} = \frac{0.5 * L * (I_{RMS})^2}{\Delta V_{OUT} * Vin}$$

For a ΔV_{OUT} = 0.5*Vin, Then Cin_{MIN} = 30.4µF

To ensure better performance on regulation, an array of low ESR ceramic capacitors were used to get a total of 300 µF in both input terminals.

5.6 Selecting the Output Filter Capacitor

For the output capacitor, the following considerations are most important and not the actual Farad value: the physical size, the ESR of the capacitor, and the voltage rating. Calculate the minimum output capacitor using the following formula:

$$C_0 = \frac{\Delta Iout}{8 * F_{SW} * \Delta Vout}$$

A more significative calculation must include the transient response in order to calculate the real minimum capacitor value and assure a good performance.

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Transient Response percentage	TR_%
Maximum Transient Voltage	TR_V_dip = V_{OUT}*TR_%
Maximum current step	$\Delta Iout\_step = \frac{(Vin\_\min - Vout) * D\_\max}{Fsw * L}$
Inductor Current rise time	$dt\_I\_rise = \frac{T * Iout}{\Delta Iout\_step}$
	$Co = \frac{Iout * dt\_I\_rise}{TR\_V\_dip}$

To find the Maximum allowed ESR, the following formula was used:

$$ESR_{\max} = \frac{\Delta Vout * Fsw * L}{Vout(1 - D\min)}$$

5.7 Bootstrap Capacitor

Freescale recommends a 0.1 μF for capacitor C_{BOOT1} and C_{BOOT2}.

5.8 Compensation Network

Compensation network is calculated exactly in the same way for both channels. Since we are using different values for L, the LC poles will be located at different frequencies to ensure stability of the system when converter 1 is supplying the power voltage of converter 2.

1. Choose a value for R1 (in this case, R1 = 20KΩ for both channels)

2. Using a Crossover frequency of 100 kHz, set the Zero pole frequency to Fcross/10

$$F_{P0} = \frac{1}{10} Fcross = \frac{1}{2\pi * R_1 C_F} \qquad C_F = \frac{1}{2\pi * R_1 F_{PO}}$$

3. Knowing the LC frequency, the Frequency of Zero 1 and Zero 2 in the compensation network are equal to F_{LC}

$$F_{LC} = \frac{1}{2\pi\sqrt{L_X Co_X}} = F_{Z1} = F_{Z2} \qquad F_{Z1} = \frac{1}{2\pi * R_F C_F} \qquad F_{Z2} = \frac{1}{2\pi * R_1 C_S}$$

$$R_F = \frac{1}{2\pi * C_F F_{Z1}} \qquad C_S = \frac{1}{2\pi * R_1 F_{Z2}}$$

4. Calculate R_S by placing the first pole at the ESR zero frequency.

$$F_{ESR} = \frac{1}{2\pi * Co_X * ESR} = F_{P1} \qquad F_{P1} = \frac{1}{2\pi * R_S C_S} \qquad R_S = \frac{1}{2\pi * F_{P1} C_S}$$

5. Set the second pole at Crossover Frequency to achieve a faster response and a proper phase margin.

$$F_{P2} = \frac{1}{2\pi * R_F \frac{C_F Cx}{C_F + C_x}} \qquad C_X = \frac{C_F}{2\pi * R_F C_F F_{P2} - 1}$$

For Channel 1	For Channel 2
FLC = 9.19 KHz F_{ESR} = 265.26 KHz (For ESR = 2.0mΩ) F_{CROSS} = 100 KHz F_{PO} = 10 KHz R1 = 20 KΩ C_F = 0.75 nF R_F = 22 KΩ C_S = 0.91 nF R_S = 0.560 KΩ C_X = 0.015 nF	FLC = 7.5 KHz F_{ESR} = 265.26 KHz (For ESR = 2.0mΩ) F_{CROSS} = 100 KHz F_{PO} = 10 KHz R1 = 20 KΩ C_F = 1.8 nF R_F = 15 KΩ C_S = 1 nF R_S = 300 KΩ C_X = 0.020 nF

5.9 Soft Start

Table 2 shows the voltage that should be applied to terminals ILIM1 and ILIM2 to get the desired configuration of the soft start. The voltage can be achieved by connecting a resistor divided from Output VDDI (2.5V) to the ILIM Terminals.

Soft Start [ms]	Voltage applied to ILIM
3.2	1.25 - 1.49V
1.6	1.50 - 1.81V
0.8	1.82 - 2.13V
0.4	2.14 - 2.50V

Table 2. Soft Start Configuration

ILIM1 and ILIM2 are directly connected to VDDI to achieve a soft start of 0.4ms on both outputs.

5.10 Tracking Configurations

This device allows two tracking configurations: Ratiometric and Co-incidental Tracking.

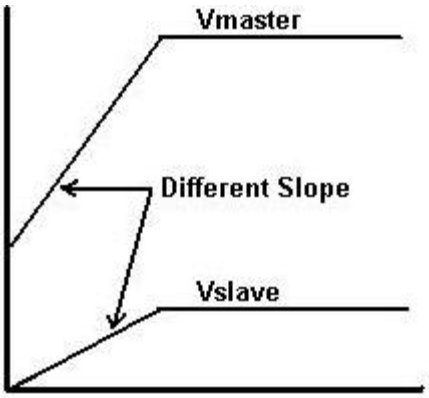

Figure 2. Radiometric Tracking

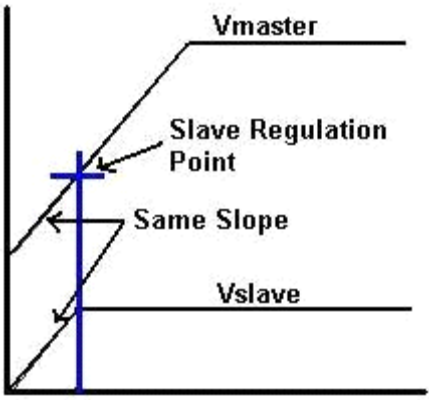

Figure 3. Co-incidental Tracking

5.10.1 Ratiometric Tracking

Circuit Configuration:

The master voltage feedback resistor divider network will be used in place of R_3 and R_4 as shown in Figure 4. The slave output is connected through its own feedback resistor divider network to the INV- terminal, resistors R_1 and R_2. All four resistors will affect the accuracy of the system and need to be 1% accurate resistors.

The master voltage must be connected in the way shown to achieve this tracking, and cannot be directly connected to the VREFIN terminal.

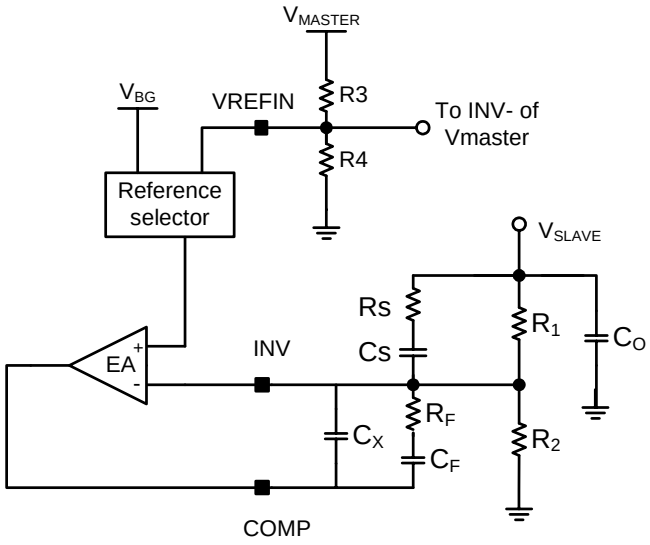

Figure 4. Radiometric Tracking Circuit Connections

Equations:

- $V_M = V_{BG\_M}(1+R_3/R_4)$
- $V_{REFIN} = V_M * R_4/(R_3+R_4)$
- $V_{REFOUT} = V_{REFIN}$
- $V_S = V_{REFOUT}(1+R_1/R_2) = V_M * R_4/(R_3+R_4)*(R_2+R_1)/R_2$, if $V_{REFOUT} < V_{BG\_S}$
- $V_S = V_{BG\_S}(1+R_1/R_2)$, if $V_{REFOUT} \geq V_{BG\_S}$

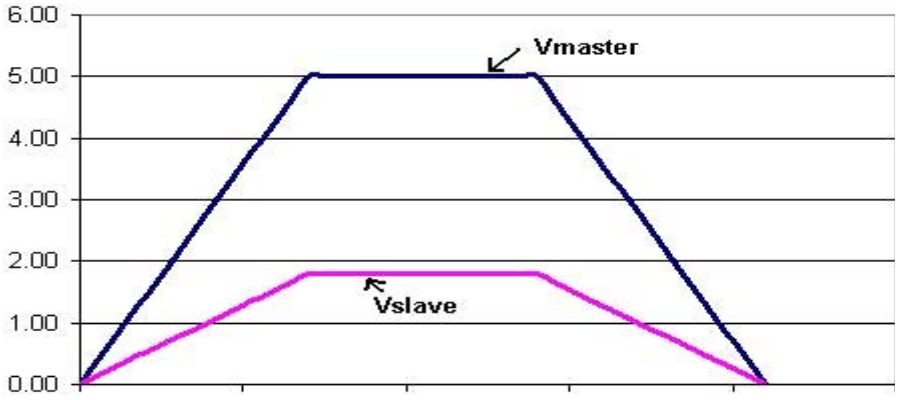

Figure 5. Radiometric Tracking Plot

5.10.2 Co-incidental Tracking

Circuit Configuration:

Connect a three resistor divider to the Master Voltage (V_M) and route the upper tap point of the divider to the VREFIN terminal, resistors R_3, R_4, and R_5 as shown in Figure 6. This resistor divider must be the same ratio as the slave output's (V_S) feedback resistor divider, which in turn connects to the INV- terminal, resistors R_1 and R_2 (**Condition: $R_1 = R_3$ and $R_2 = R_4 + R_5$**). The master's feedback resistor divider would be (R_3+R_4) and R_5. All five resistors will affect the accuracy of the system and must be 1% accurate resistors.

The master voltage must be connected in the way shown to achieve this tracking, and cannot be directly connected to the VREFIN terminal.

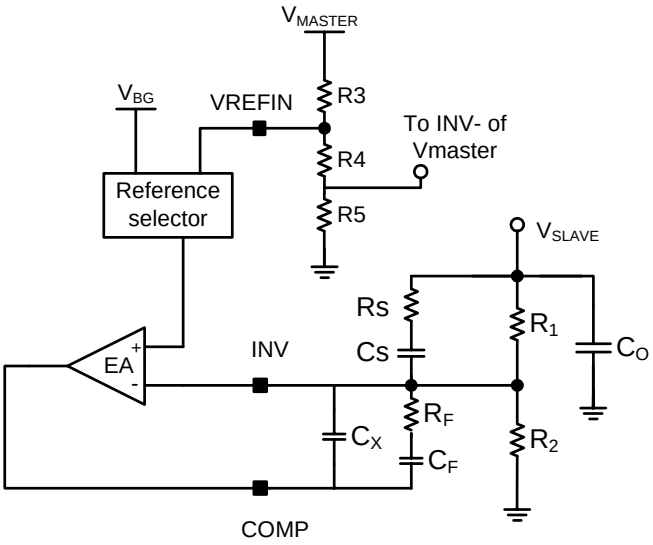

Figure 6. Co-incidental Tracking Circuit Connections

Equations:

- $V_M = V_{BG\_M}[1+(R_3+R_4)/R_5]$
- $V_{REFIN} = V_M*(R_4+R_5)/(R_3+R_4+R_5)$
- $V_{REFOUT} = V_{REFIN}$
- $V_S = V_{REFOUT}(1+R_1/R_2) = V_M*(R_4+R_5)/(R_3+R_4+R_5)*(R_2+R_1)/R_2 = V_M$ if $V_{REFOUT} < V_{BG\_S}$
- $V_S = V_{BG\_S}(1+R_1/R_2)$, if $V_{REFOUT} \geq V_{BG\_S}$

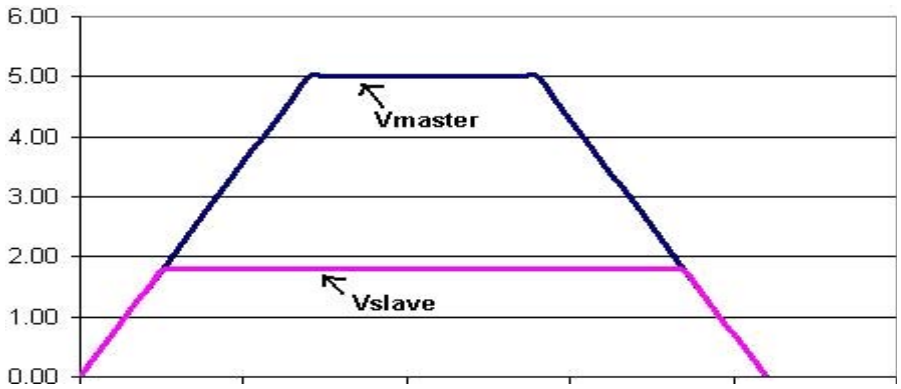

Figure 7. Co-incidental Tracking Circuit Connections

5.10.3 Non-DDR Mode (Source Only Mode)

This is the case when no tracking is needed. VREFIN should be connected to VDDI and the reference selection block will use the internal band gap voltage as the Error Amplifier's reference voltage.

A user can potentially apply a voltage to the VREFIN terminal directly, or through a resistor divider to get a buffered output for use in this application. The condition here is, the voltage applied on VREFIN terminal is larger than V_{BG}, to guarantee that the reference selection block will not switch back to the V_{REFOUT} voltage

The VREFIN pin on the EVB is **left opened,** so that the user can either connect directly to VOUT1 with a jumper, or use an external master voltage to track, in either of these configurations.

5.11 EVB Schematic Design

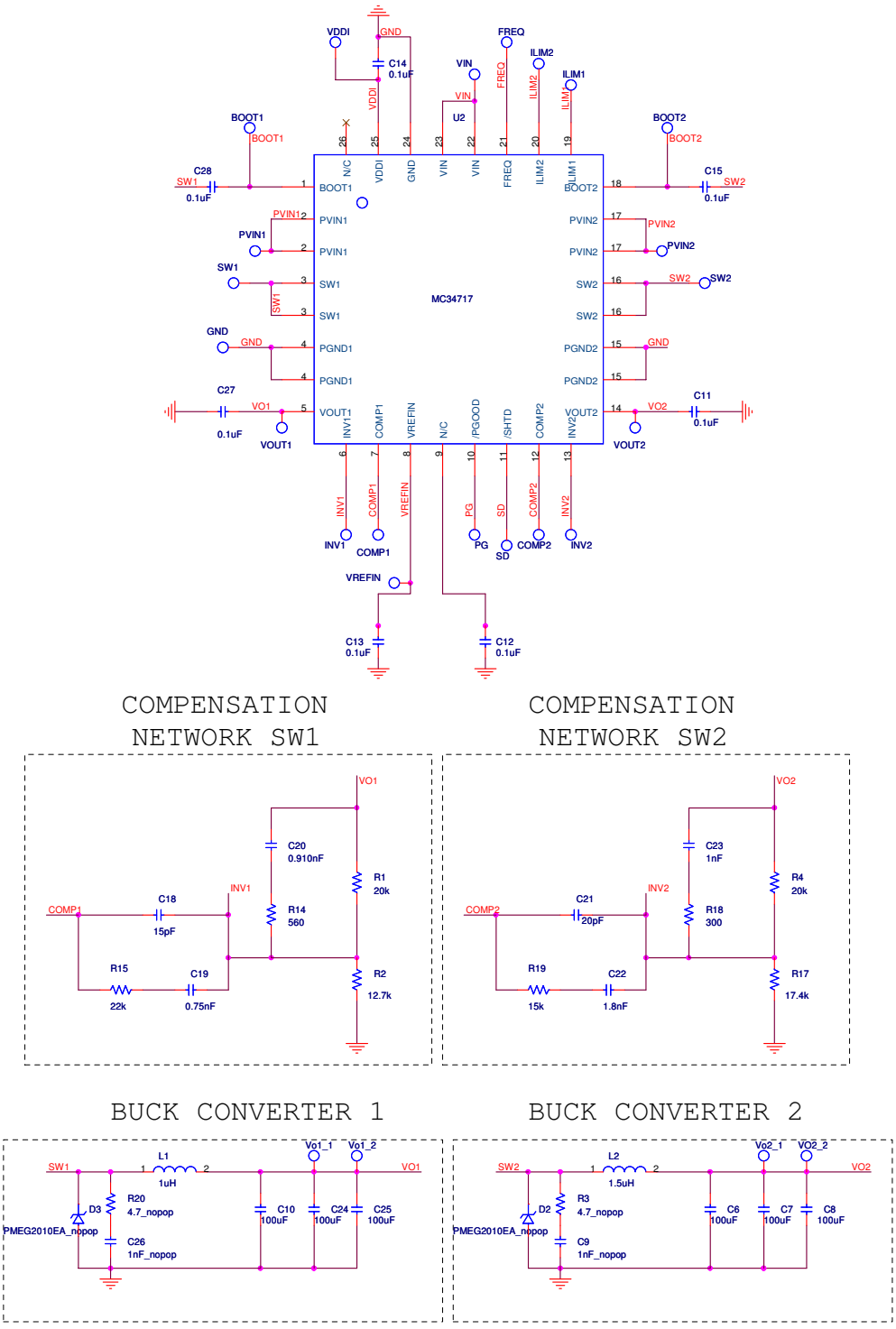

Figure 8. KIT34717EPEVBE Schematic Part 1

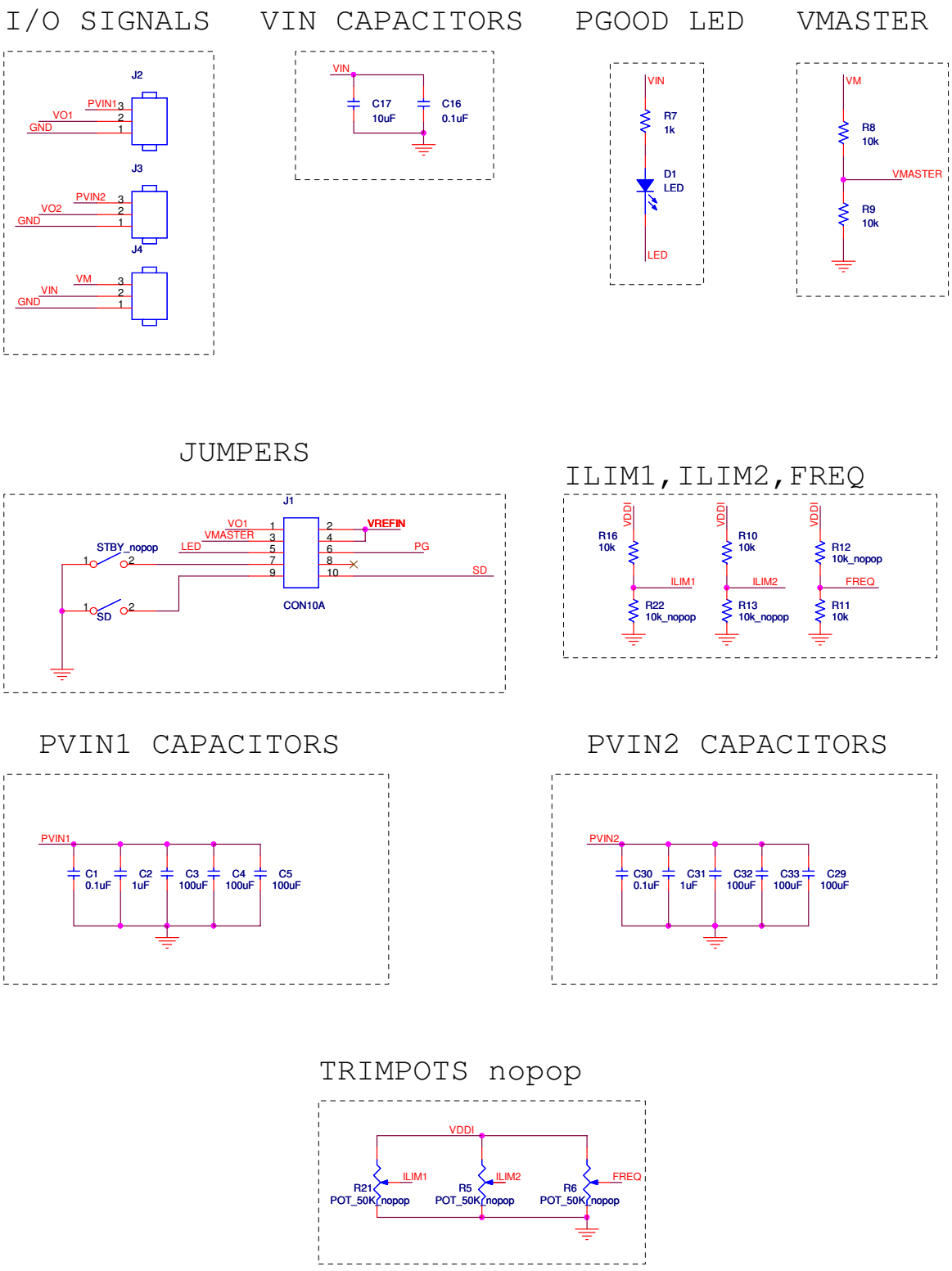

Figure 9. KIT34717EPEVBE Schematic Part 2

6 Layout Design

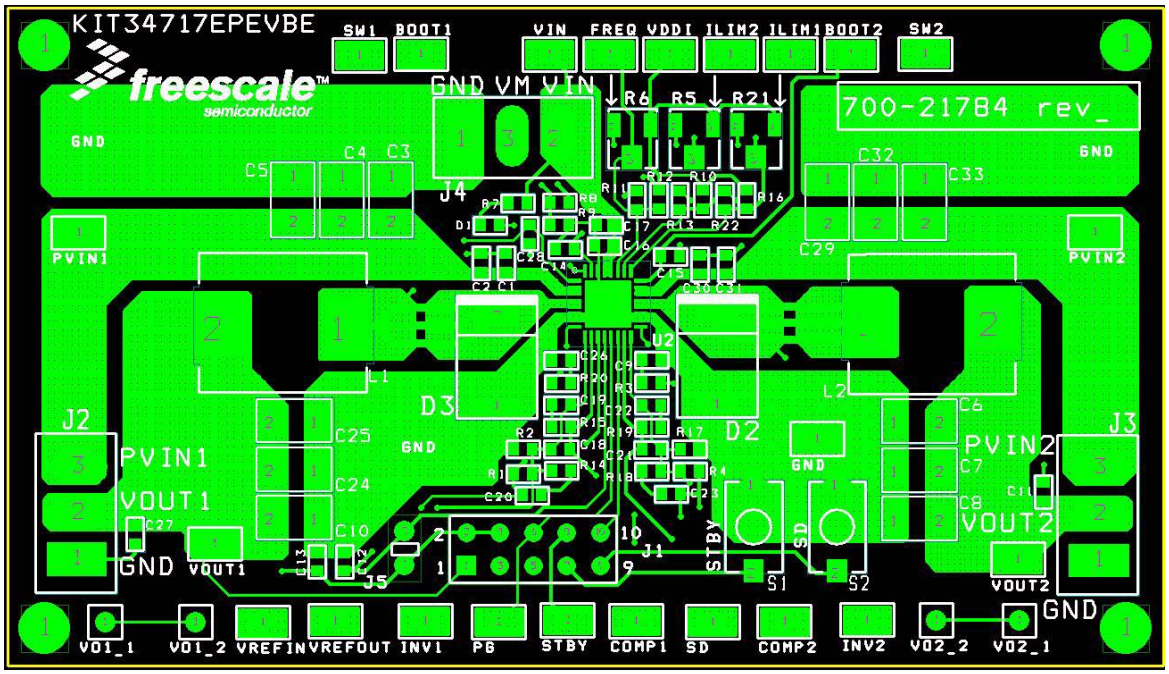

Figure 10. PCB Top View Layout Design

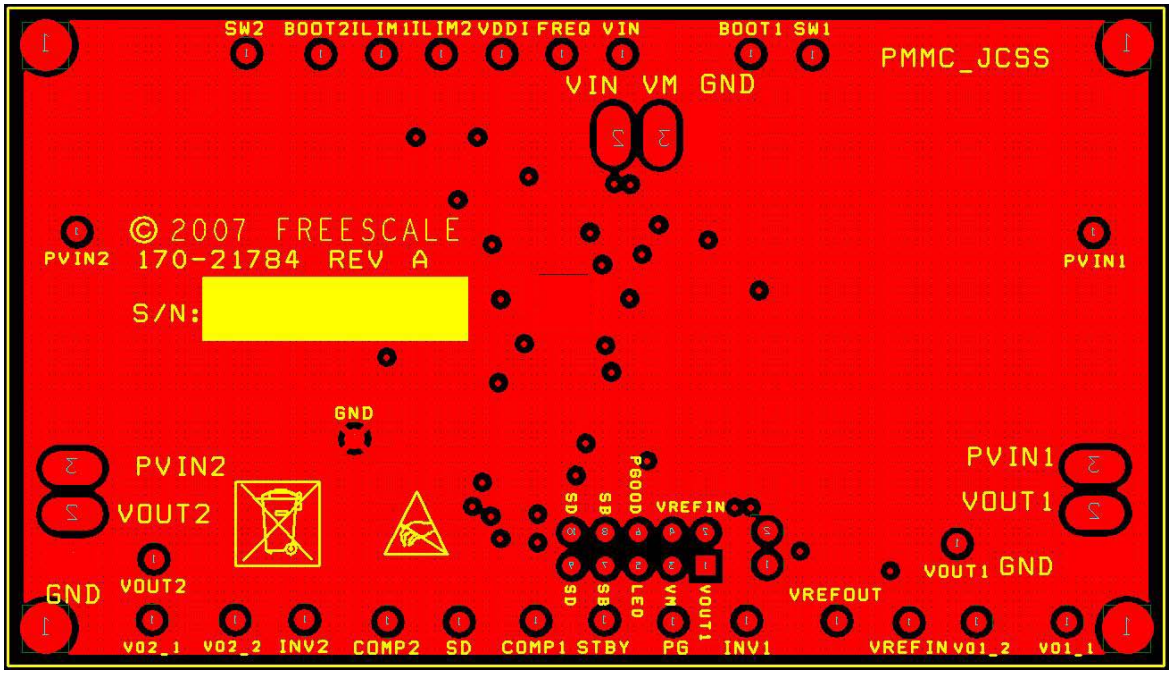

Figure 11. PCB Bottom View Layout Design

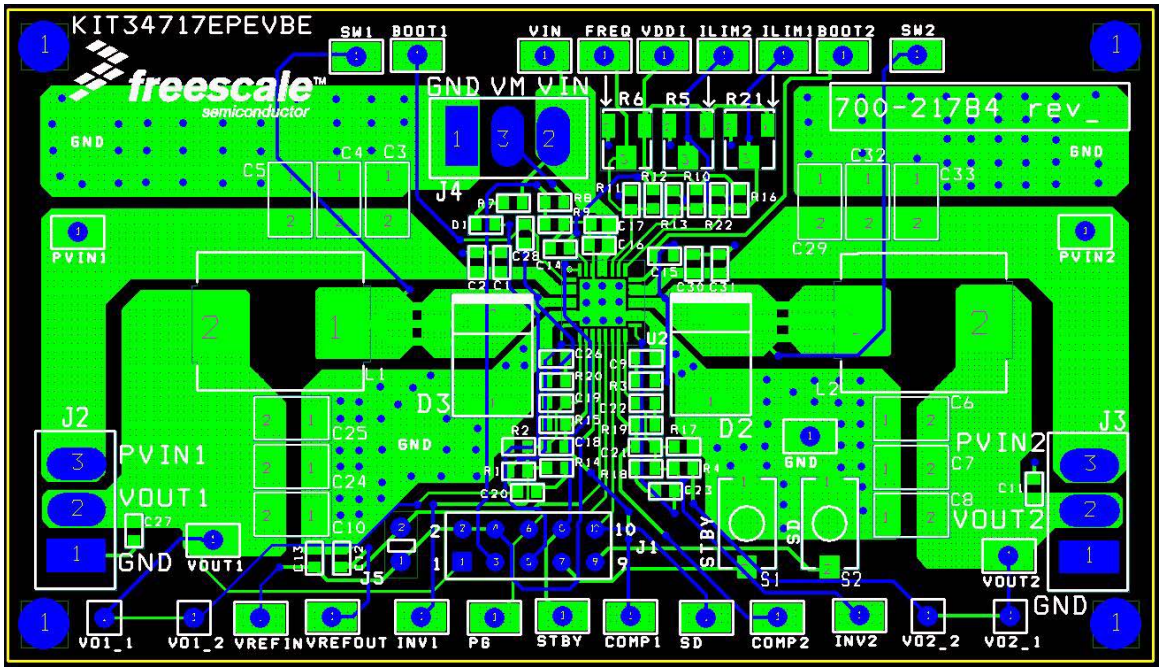

Figure 12. PCB Inner View Layout Design

6.1 PCB Layout Recommendations

- Place decoupling capacitors as close as possible to their corresponding pad(s)
- Try to place all components on just one Layer.
- Do not place a Ground Plane on component and routing side.
- Create a Ground plane layer and tie it to ground signals with vias.
- To effectively transfer heat from the center thermal pad on the top layer to the ground plane, vias need to be used in the center pad. Use 5 to 9 vias spaced evenly with a finished diameter of 0.3mm.
- Place Test vias as close as possible to the IC to ensure a good measurement value.
- PVIN, VIN, VOUT signals have to be tracked with a widely and straight copper area
- Never trace the Feedback signal in parallel to the SW signal.
- Ensure the SW Inductor is placed as close as possible to its pads.
- SW track has to be as thin and short as possible.
- Make sure the I/O connectors are capable to manage the Load current.

Note: Freescale does not recommend connecting the PGND pins to the thermal pad. The thermal pad is connected to the signal ground and should not be used to make the connection from the PGND pins to the ground plane. Doing so can cause ground bounce on the signal ground from the high di/dt switch current and parasitic trace inductance.

6.2 Bill of Materials

Table 3. BILL OF MATERIALS KIT34717

EVB Number: KIT34717EPEVBE

Item	Qty	Reference	Value	Description	Footprint
1	23	VOUT1,SW1,PVIN1,INV1,ILIM1,COMP1, BOOT1,VOUT2,SW2,PVIN2,INV2,ILIM2, COMP2,BOOT2,VREFOUT,VREFIN,VIN, VDDI,STBY,SD,PG,GND,FREQ	not populated	PC Test point miniature SMT	TP
2	2	C2,C31	1.0μF	Cap Cer 1.0 μF 6.3V 10% X5R 0603	SM/C_0603
3	12	C3,C4,C5,C6,C7,C8,C10,C24,C25,C29, C32,C33	100μF	Cap Cer 100 μF 6.3V 10% X5R 1210	SM/C_1210
4	2	C9,C26	not populated		
5	10	C1,C11,C12,C13,C14,C15,C16,C27,C28, C30	0.1μF	Cap Cer 0.1 μF 50V 10% X7R 0603	SM/C_0603
6	1	C17	10μF	Cap Cer 10 μF 6.3V 20% X5R 0603	SM/C_0603
7	1	C18	15pF	Cap Cer 15pF 50V 1% C0G 0603	SM/C_0603
8	1	C19	750pF	Cap Cer 750pF 50V 5% C0G 0603	SM/C_0603
9	1	C20	910pF	Cap Cer 910pF 50V 5% C0G 0603	SM/C_0603
10	1	C21	20pF	Cap Cer 20pF 50V 5% C0G 0603	SM/C_0603
11	1	C22	1.8nF	Cap Cer 1800pF 50V 5% C0G 0603	SM/C_0603
12	1	C23	1.0nF	Cap Cer 1000pF 25V 5% C0G 0603	SM/C_0603
13	1	D1	LED	LED Green 0603 SMD	SM/C_0603
14	2	D2,D3	not populated		
15	1	J1	Pin Header (2 x 5)	HDR 2X5 TH 100mil CTR 330H AU	0.1" (2.54mm)
16	3	100mils jumpers	Jumpers		100mils
17	3	J2,J3,J4	not populated		

18	1	J5	not populated		
19	1	L1	1.0μH	Inductor Power 1.0μH 7.5A SMD	B82464G
20	1	L2	1.5μH	Inductor Power 1.5μH 7.0A SMD	B82464G
21	2	R1,R4	20kΩ	Res MF 20kΩ 1/10W 1% 0603 SMD	SM/C_0603
22	1	R2	12.7kΩ	Res MF 12.7kΩ 1/10W 1% 0603 SMD	SM/C_0603
23	2	R3,R20	not populated		
24	3	R5,R6,R21	not populated		
25	1	R7	1kΩ	Res MF 1.0kΩ 1/10W 1% 0603	SM/C_0603
26	1	R10	10kΩ	Res MF 10kΩ 1/10W 1% 0603	SM/C_0603
27	3	R12,R13,R22	not populated		
28	4	R8,R9,R11,R16	10kΩ	Res MF 10kΩ 1/10W 1% 0603	SM/C_0603
29	1	R14	560Ω	Res MF 560Ω 1/10W 1% 0603	SM/C_0603
30	1	R15	22kΩ	Res MF 22kΩ 1/10W 5% 0603	SM/C_0603
31	1	R17	17.4kΩ	Res MF 17.4kΩ 1/10W 1% 0603	SM/C_0603
32	1	R18	300Ω	Res MF 300Ω 1/10W 5% 0603	SM/C_0603
33	1	R19	15kΩ	Res MF 15kΩ 1/10W 1% 0603	SM/C_0603
34	1	SD	Push_Button	Switch Tact Mini 200GF SLV Gwing	
35	1	STBY	not populated	Switch Tact Mini 200GF SLV Gwing	
36	1	U2	MC34717		QFN_26

Notes: Freescale does not assume liability, endorse, or warrant components from external manufacturers that are referenced in circuit drawings or tables. While Freescale offers component recommendations in this configuration, it is the customer's responsibility to validate their application.

7 Conclusion

With this User Guide, the user will be capable of configuring the 34717 as a double switching power supply for devices that can make use of some of the capabilities that the 34717 offers. The board is fully configured to work at any desirable input voltage within 3V and 6V. However, it is highly recommended to calculate all components for the specific application situation in order to assure a better efficiency and stability of the IC.

8 References

- 34717 Datasheet, 5A and 5A 1MHz fully integrated double switch-mode power supply, Freescale semiconductor, Inc.
- Application Note “AN1989 MC34701 and MC34702 Component Selection Guide”, Freescale Semiconductor, Inc.
- Sanjaya Maniktala, “*Switching Power Supplies A to Z*”, Newnes, 2006.

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