Littelfuse Technologies: Power Thyristors • Protection Arrays • Fuses • PTCs • Varistors • TVS Diodes • GDTs • ESD Suppressors • SIDACtor Devices

Introduction to Silicon Protection Arrays

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Updated 09/21/2010

Outline

CIRCUIT PROTECTION SOLUTIONS

- ESD Protection
  - Test Pulse Waveforms
  - Compare w/ Lightning
- Key Parameters
  - V_{RWM}
  - V_{BR} or V_R
  - V_C
  - Capacitance
  - V_{ESD}
  - I_P or I_{PP}
- Configurations
  - Grounded TVS Diode Arrays (SP03)
  - TVS Rail Clamp Diode Arrays (SP30xx, SP40xx)
  - TVS Arrays (SP10xx, SP050x)
  - SCR Array Rail Clamps (SP72x)
  - EMI Filter Arrays (SP60xx)
- PC Board Layout Issues
  - Close to the input
  - Avoiding stub traces
  - Paralleling channels
- Package Options
  - Micro Packages
  - MSOP Packages
  - Power Packages

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ElectroStatic Discharge Protection

CIRCUIT PROTECTION SOLUTIONS

Lightning

AC Power Contact

Sustained Overload

ESD is one of four major threats to electronic equipment.

Protecting equipment against ESD is a $500M market

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ESD is FAST!!

CIRCUIT PROTECTION SOLUTIONS

- AC Power Contact tests are measured in milliseconds
  - 1000 milliseconds = 1 second
- Lightning pulses are measured in microseconds
  - 1000 microseconds = 1 millisecond
- ESD pulses are measured in nanoseconds
  - 1000 nanoseconds = 1 microsecond

An object traveling at the speed of light can go:
- Around Earth more than 7 times in one second
- 186 miles or 300 km in one millisecond
- 1000 feet or 300 m in one microsecond
- 1 foot or 30 cm in one nanosecond

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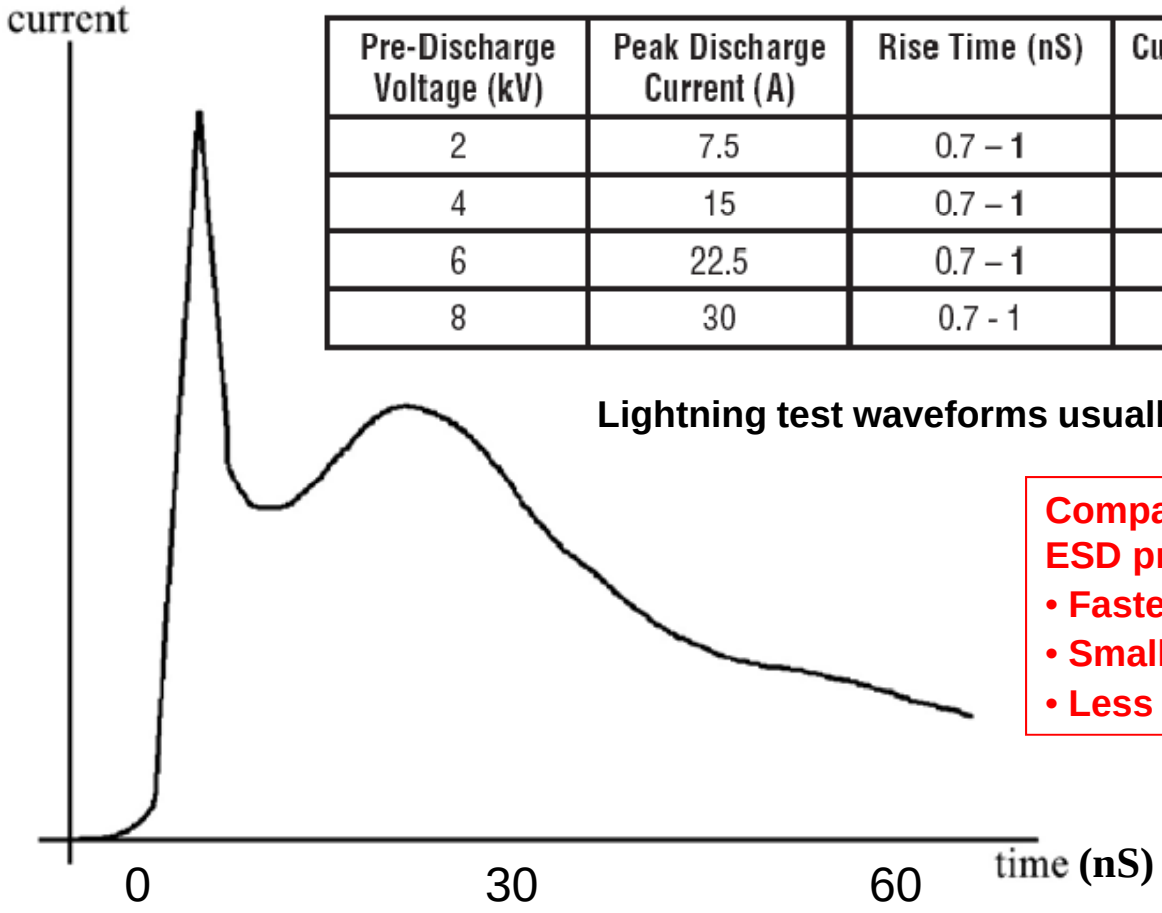
ESD Test Waveforms

IEC 61000-4-2

CIRCUIT PROTECTION SOLUTIONS



Pre-Discharge Voltage (kV)	Peak Discharge Current (A)	Rise Time (nS)	Current at 30 nS	Current at 60 nS
2	7.5	0.7 – 1	4	2
4	15	0.7 – 1	8	4
6	22.5	0.7 – 1	12	6
8	30	0.7 - 1	16	8

Lightning test waveforms usually peak at 100A – 500A.

Compared to lightning protectors, ESD protectors are:

- **Faster**
- **Smaller**
- **Less robust**

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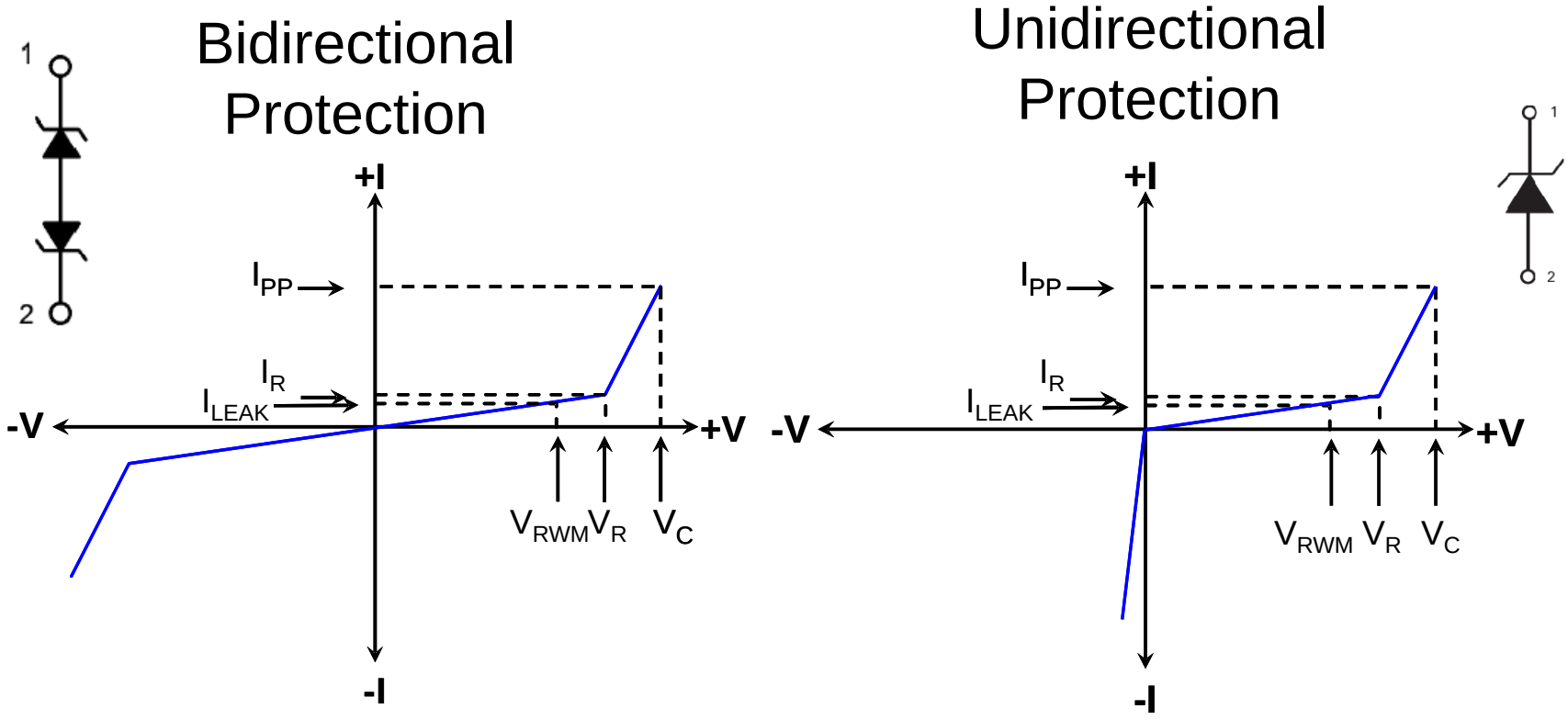
Bidirectional vs. Unidirectional

CIRCUIT PROTECTION SOLUTIONS



Voltage – Current (V-I) Curve

- Voltage is displayed left to right
- Current is displayed up and down

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Key Parameters: V_{RWM}

CIRCUIT PROTECTION SOLUTIONS

- The Reverse Standoff Voltage or V_{RWM} is the maximum voltage that can be applied to the ESD protector without activating the device.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Forward Voltage Drop	V_F	I_F=10mA	0.7	0.9	1.2	V
Reverse Voltage Drop	V_R	I_R=1mA	7.0	7.8	8.5	V
Reverse Standoff Voltage	V_{RWM}	I_R≤1µA			5.5	V
Reverse Leakage Current	I_{LEAK}	V_R=5V			0.5	µA
Clamp Voltage[1]	V_C	I_{PP}=1A, t_p=8/20µs, Fwd		8.0	11.0	V
		I_{PP}=2A, t_p=8/20µs, Fwd		9.7	13.0	V
Dynamic Resistance	R_{DYN}	$(V_{C2} - V_{C1}) / (I_{PP2} - I_{PP1})$		1.7		Ω
ESD Withstand Voltage[1,2]	V_{ESD}	IEC61000-4-2 (Contact)	±15			kV
		IEC61000-4-2 (Air)	±30			kV
Diode Capacitance[1]	C_D	Reverse Bias=0V		12		pF
		Reverse Bias=2.5V		8		pF
		Reverse Bias=5V		7		pF

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Key Parameters: V_R

CIRCUIT PROTECTION SOLUTIONS

- The Reverse Voltage Drop or V_R is the voltage at which the device will begin to break down and begin to protect.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Forward Voltage Drop	V_F	I_F=10mA	0.7	0.9	1.2	V
Reverse Voltage Drop	V_R	I_R=1mA	7.0	7.8	8.5	V
Reverse Standoff Voltage	V_{RWM}	I_R≤1µA			5.5	V
Reverse Leakage Current	I_{LEAK}	V_R=5V			0.5	µA
Clamp Voltage[1]	V_C	I_{PP}=1A, t_p=8/20µs, Fwd		8.0	11.0	V
		I_{PP}=2A, t_p=8/20µs, Fwd		9.7	13.0	V
Dynamic Resistance	R_{DYN}	$(V_{C2} - V_{C1}) / (I_{PP2} - I_{PP1})$		1.7		Ω
ESD Withstand Voltage[1,2]	V_{ESD}	IEC61000-4-2 (Contact)	±15			kV
		IEC61000-4-2 (Air)	±30			kV
Diode Capacitance[1]	C_D	Reverse Bias=0V		12		pF
		Reverse Bias=2.5V		8		pF
		Reverse Bias=5V		7		pF

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Key Parameters: V_C

CIRCUIT PROTECTION SOLUTIONS

- The Clamp Voltage or V_C is the maximum voltage that will appear across the device during the specified surge event.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Forward Voltage Drop	V_F	I_F=10mA	0.7	0.9	1.2	V
Reverse Voltage Drop	V_R	I_R=1mA	7.0	7.8	8.5	V
Reverse Standoff Voltage	V_{RWM}	I_R≤1µA			5.5	V
Reverse Leakage Current	I_{LEAK}	V_R=5V			0.5	µA
Clamp Voltage[1]	V_C	I_{PP}=1A, t_p=8/20µs, Fwd		8.0	11.0	V
		I_{PP}=2A, t_p=8/20µs, Fwd		9.7	13.0	V
Dynamic Resistance	R_{DYN}	$(V_{C2} - V_{C1}) / (I_{PP2} - I_{PP1})$		1.7		Ω
ESD Withstand Voltage[1,2]	V_{ESD}	IEC61000-4-2 (Contact)	±15			kV
		IEC61000-4-2 (Air)	±30			kV
Diode Capacitance[1]	C_D	Reverse Bias=0V		12		pF
		Reverse Bias=2.5V		8		pF
		Reverse Bias=5V		7		pF

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Key Parameters: Capacitance

CIRCUIT PROTECTION SOLUTIONS

Electrical Characteristics (T_{OP}=25°C)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Reverse Standoff Voltage	V_{RWM}	$I_R \leq 1\mu A$			6.0	V
Reverse Leakage Current	I_{LEAK}	V_R=5V, Any I/O to GND		0.1	0.5	µA
Clamp Voltage[1]	V_C	I_{PP}=1A, t_p=8/20µs, Fwd		10.8		V
		I_{PP}=2A, t_p=8/20µs, Fwd		12.3		V
Dynamic Resistance	R_{DYN}	$(V_{C2} - V_{C1}) / (I_{PP2} - I_{PP1})$		1.5		Ω
ESD Withstand Voltage[1]	V_{ESD}	IEC61000-4-2 (Contact)	±8			kV
		IEC61000-4-2 (Air)	±15			kV
Diode Capacitance[1]	$C_{I/O-GND}$	Reverse Bias=0V		0.45		pF

- Capacitance adversely affects high data rate signals. Lower capacitance s always better.
- Capacitance may be specified at various bias voltages or between various pins.

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Key Parameters: V_{ESD}

CIRCUIT PROTECTION SOLUTIONS

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Forward Voltage Drop	V_F	I_F=10mA	0.7	0.9	1.2	V
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Reverse Standoff Voltage	V_{RWM}	I_R≤1µA			5.5	V
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		I_{PP}=2A, t_p=8/20µs, Fwd		9.7	13.0	V
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Diode Capacitance[1]	C_D	Reverse Bias=0V		12		pF
		Reverse Bias=2.5V		8		pF
		Reverse Bias=5V		7		pF

- V_{ESD} is a measure of the robustness of the device. It is the maximum test voltage that can be sustained without damaging the device. The test conditions are specified.

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Key Parameters: I_P or I_{PP}

CIRCUIT PROTECTION SOLUTIONS

Absolute Maximum Ratings

Symbol	Parameter	Value	Units
I_P	Peak Current (t_p=8/20µs)	4.5	A
T_{OP}	Operating Temperature	-40 to 85	°C
T_{STOR}	Storage Temperature	-50 to 150	°C

- The Peak Current or I_P (or sometimes I_{pp}) is the maximum peak current that can be applied to the ESD protector without damaging the device. The surge waveform conditions are always specified. Sometimes, several surge waveforms are specified:

Absolute Maximum Ratings

Parameter	Rating	Units
Peak Pulse Current (8/20µs)	150	A
Peak Pulse Power (8/20µs)	2800	W
IEC 61000-4-2, Direct Discharge, (Level 4)	8	kV
IEC 61000-4-2, Air Discharge, (Level 4)	15	kV
IEC 61000-4-5 (8/20µs)	100	A
Bellcore GR 1089 (Intra-Building) (2/10µs)	100	A
ITU K.20 (5/310µs)	40	A

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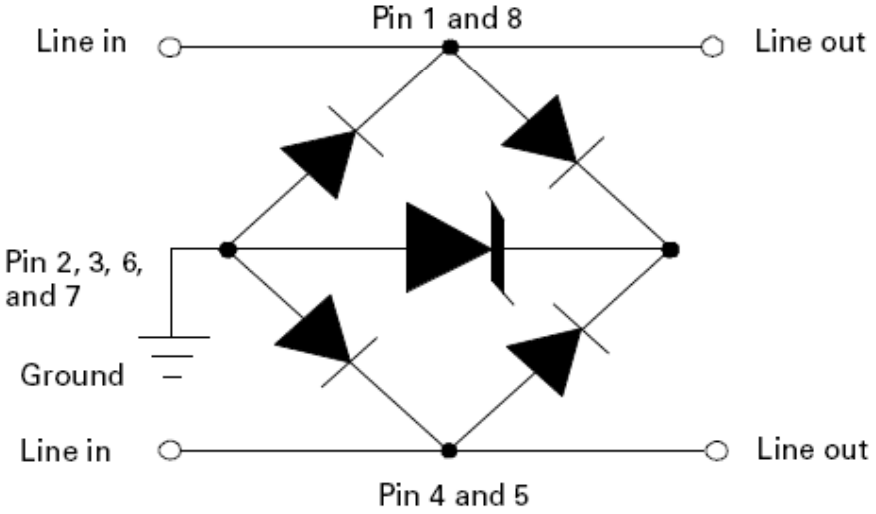
Grounded TVS Diode Arrays (SP03)

CIRCUIT PROTECTION SOLUTIONS



Capacitance Range: 8pF-16pF (typical)

ESD Range: 30kV (contact discharge)

Lightning Range: 100-150A

Applications: Broadband Protection (i.e. 10/100/1000 Base T Ethernet)

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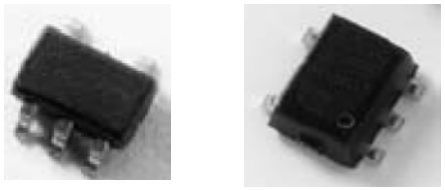
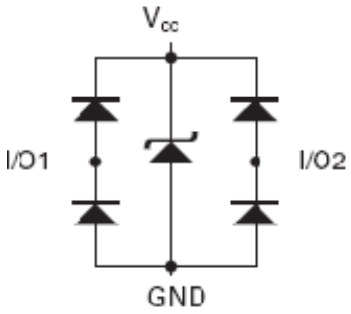
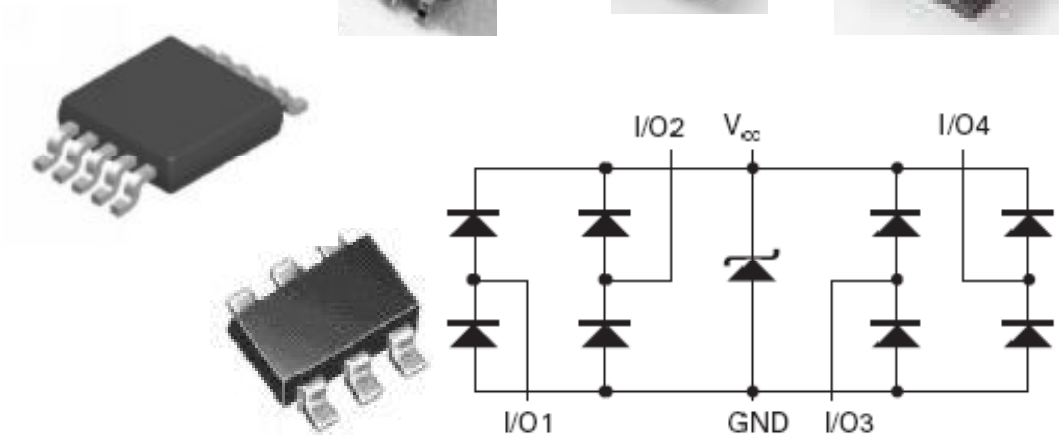
TVS Rail Clamp Diode Arrays (SP30xx, SP40xx)

CIRCUIT PROTECTION SOLUTIONS







Capacitance Range: 0.40pF-2.4pF (typical)

ESD Level: ±8-30kV (contact discharge)

Lightning Range: 2.5-10A

Applications: HDMI, USB2.0/3.0, and Ethernet PHY protection

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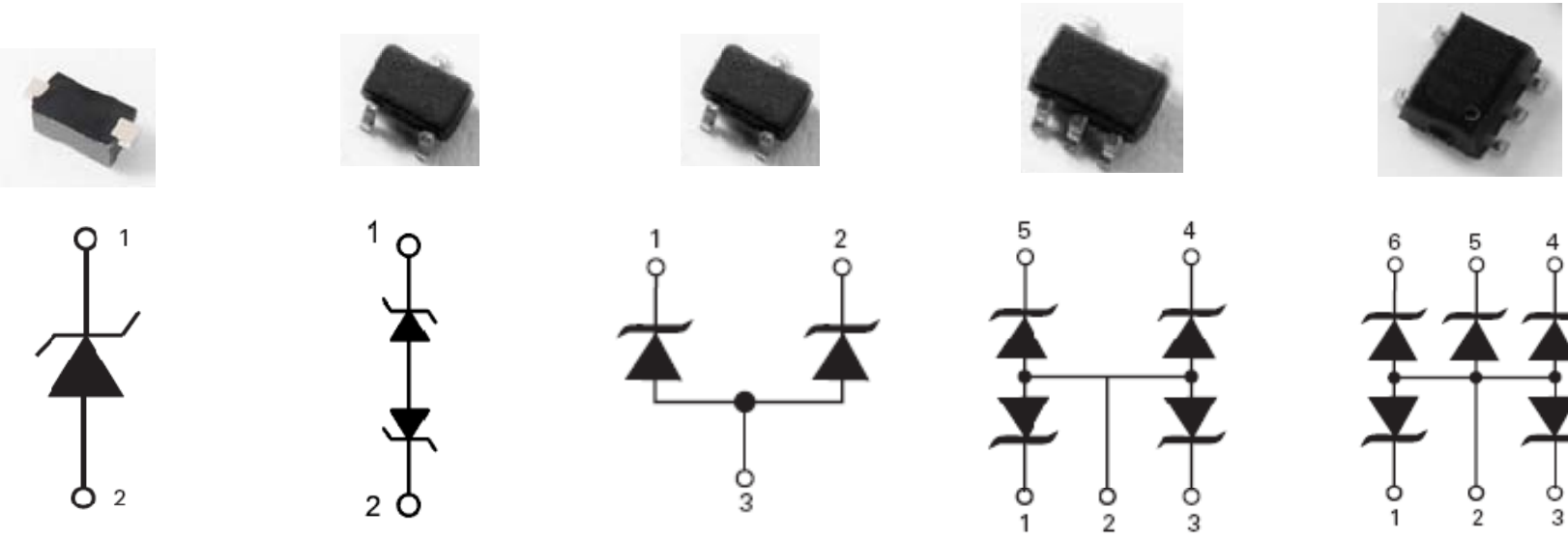
TVS Arrays (SP10xx, SP050x)

CIRCUIT PROTECTION SOLUTIONS



Capacitance Range: 3.5pF-30pF (typical)

ESD Level: ±8-30kV (contact discharge)

Lightning Range: 2-10A

Applications: Keypads, audio lines, and general low-speed bus protection

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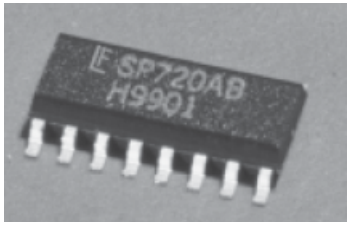
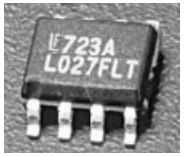
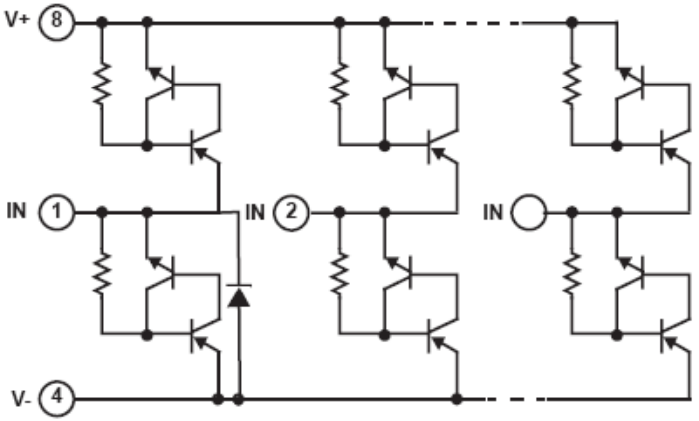
SCR Array Rail Clamps (SP72x)

CIRCUIT PROTECTION SOLUTIONS







Capacitance Range: 3pF-5pF (typical)

ESD Level: ±4-8kV (contact discharge)

Lightning Range: 3-14A

Applications: µP Logic Inputs and general low-speed bus protection

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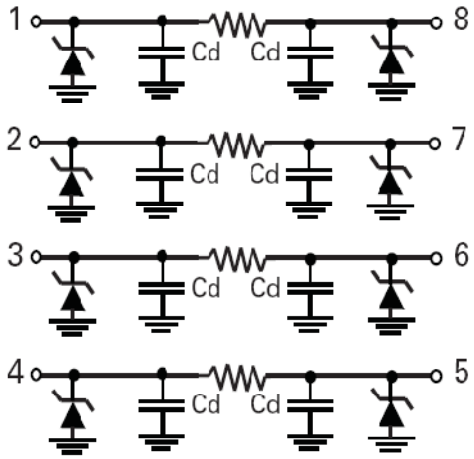
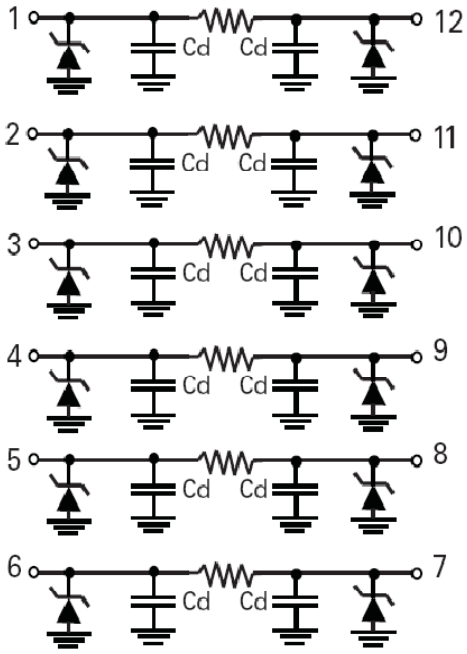
EMI Filter Arrays (SP60xx)

CIRCUIT PROTECTION SOLUTIONS



EMI Filter Arrays not only provide ESD protection, but also serve as low-pass filters to get rid of unwanted high-frequency signals (i.e. cellular band from 800MHz-2GHz).



Capacitance Range: 7pF-15pF (typical single Cd)

ESD Level: ±15-30kV (contact discharge)

Applications: Keypad and display interfaces for portable/mobile devices

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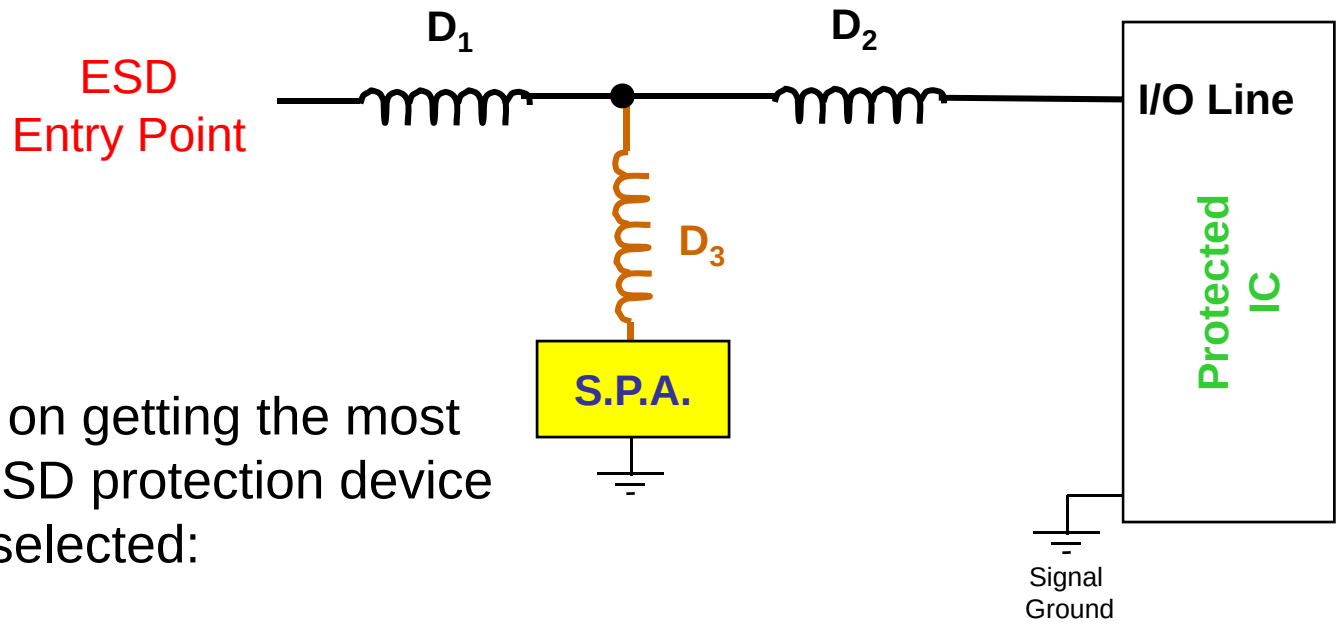
PC Board Layout Considerations

CIRCUIT PROTECTION SOLUTIONS



Some tips on getting the most from the ESD protection device you have selected:

- **Minimize D1** – Place protection near entry connector
- **Maximize D2** – For best coordination with on-chip ESD protection
- **Minimize D3** – Stub traces should be avoided

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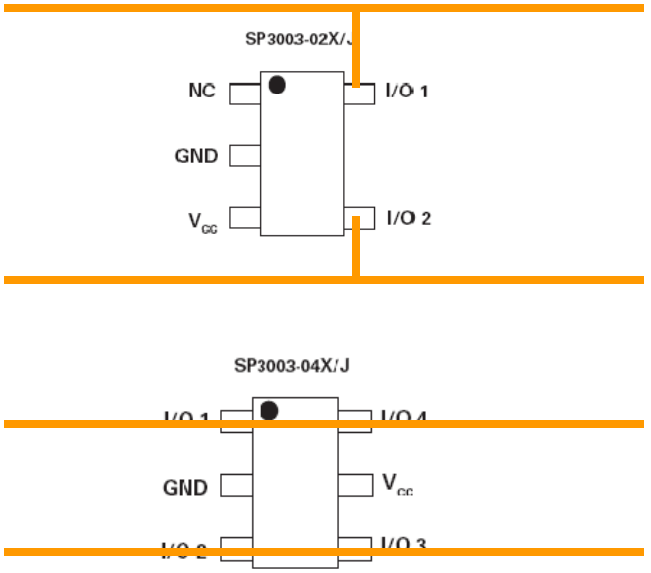
Combining Protection Channels

It is possible to combine protection channels to achieve higher surge capability:

For example, a customer loves the SOT553 package of the SP3003-02XTG, but needs a bit more V_{ESD} capability. You could use an SP3003-04XTG and combine the four channels into two. (As a bonus, the package becomes stub-less through-line!)

Of course the capacitance will double, but this may be acceptable.

A further benefit is the clamping voltage for a particular test waveform will be lower when channels are combined.



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Micro Packages

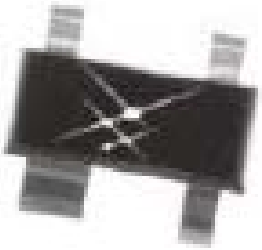
CIRCUIT PROTECTION SOLUTIONS

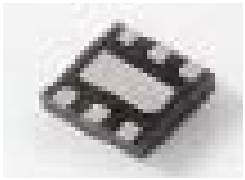
SC70 SOT5x3 SOT23 SOT143 SOD723 uDFN









Available in Series: SP10xx, SP30xx, SP050x, SP60xx

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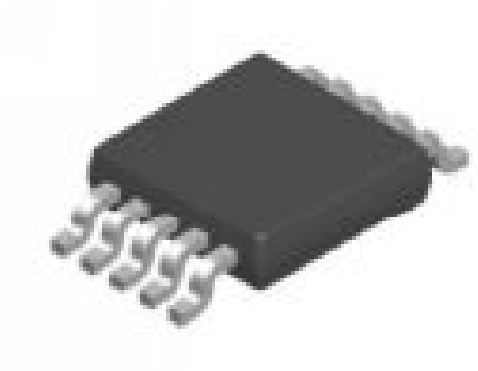
MSOP Packages

CIRCUIT
PROTECTION
SOLUTIONS

MSOP-8

MSOP-10



Available in Series: SP050x, SP30xx, SP40xx

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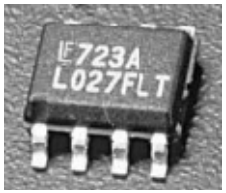
Power Packages

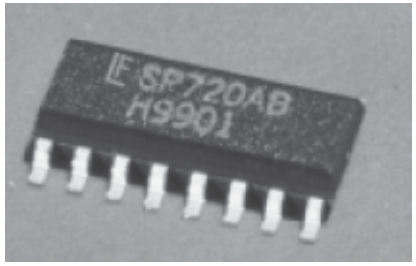
CIRCUIT
PROTECTION
SOLUTIONS

PDIP-8

PDIP-16



SOIC-8



SOIC-16

Available in Series: SP72x, SP03-x

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PROTECTION
SOLUTIONS

Thank You!

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