Board designers today are confronted with a multitude of choices for ESD protection. Often the designer is constrained by certain limits such as the amount of parasitic capacitance his/her application can withstand or the required ESD level the board must pass without fail. More often than not, the constraints do not narrow down the available number of ESD devices to a manageable list. This white paper will provide guidance to the designer that will help him/her in choosing an ESD device that will give the best chance of a successful first pass design.

Before getting into the selection criteria, let us review a few basic ESD topologies and their typical "turn-on" characteristics. *(Note: Throughout this paper the ESD threat/pulse referenced is defined by the IEC61000-4-2 standard shown below in Figure 1.)*

Figure 1
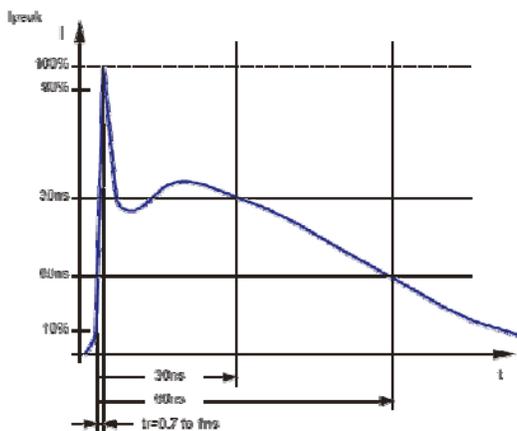
Background

There are several types of ESD suppression devices on the market today. Examples include MLV's (Multi-Layer Varistors), polymer ESD suppressors, and silicon diodes or arrays. For simplicity this paper will only focus on silicon devices as their performance tends to be superior in terms of ESD clamping capability. Nevertheless, the points discussed hereafter can be applied generically to any ESD device regardless of its technology.

The two most common silicon protection devices are TVS/Zener diodes (Figure 2) and Diode/Rail Clamps (Figure 3) which are both intended to present a low resistance shunt path to GND during an ESD event. (The main difference between the two is the amount of parasitic capacitance each structure will add to the I/O under protection.)

Each structure is intended to steer both positive and negative ESD pulses away from the IC being protected. For positive transients the TVS/Zener of Figure 2 will "turn-on" after a voltage V_Z (typically 6-8V) is reached and provide a resistive shunt to GND. Likewise the diode array in Figure 3 will steer a positive current through the "upper" diode and into the internal TVS device when a voltage V_F+V_Z is reached (typically 6-8V). For negative ESD pulses, both structures behave the same in that they each will conduct when $-V_F$ (typically 0.6-0.8V) is exceeded or the bus being protected falls one diode drop below GND. With this basic understanding in mind, let us examine the electrical characteristics typically given by ESD vendors on their device datasheets.
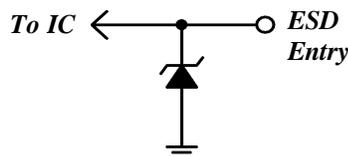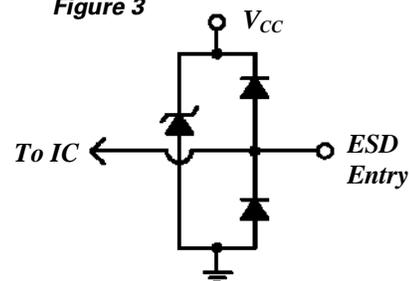
Figure 2

Figure 3

Electrical Characteristics

The majority of TVS/Zener ESD devices (Figure 2) are specified with four main characteristics: ESD Level, Reverse Standoff Voltage/Leakage, Capacitance, and Breakdown Voltage. (There is a fifth characteristic that is not as prevalent, which we'll discuss later.)

The ESD level only tells the designer what level of ESD the device itself can withstand before damage occurs. It gives no guarantee that the IC being protected will survive the same level of ESD given on the device's datasheet. Additionally, the breakdown voltage is usually between 6V-8V at 1mA or 10mA. This only gives the designer a data point to ensure the ESD device remains inactive during normal circuit operation. It gives no indication about the shunt resistance or clamping voltage he/she can expect under an ESD strike. The other two characteristics relate to the device's "parasitics" and again offer no insight about the ESD device's performance during an ESD transient.

Similarly, the rail clamp or diode array structure in Figure 3 is usually specified with the same four characteristics: ESD Level, Reverse Standoff Voltage/Leakage, Capacitance, and Breakdown Voltage. The breakdown voltage of the internal TVS diode is usually given (i.e. 6-7V) but there is no mention how the steering diodes plus TVS will behave or clamp during an ESD pulse.

In summary, the electrical characteristics mentioned above provide characterization data on the ESD protector only, and give the designer no information about the effectiveness of the ESD device under stress. We will revisit the electrical characteristics later but for now let us examine some of the common plots/graphs found in ESD device datasheets.

Characteristic Plots

A board designer can find many waveforms in an ESD device datasheet. The following list only names a few of the more common plots:

[1] Capacitance vs. Reverse Bias
[2] Power Derating Curve
[3] Insertion Loss (S21), and
[4] ESD Response or Clamp

The first three do not give any information about the ESD device's effectiveness to clamp an ESD pulse. The last plot "ESD Response" appears to be the most helpful, but there are a couple of unknowns.

First of all, some datasheets state that the input pulse is 8kV, the maximum level given per the IEC61000-4-2 standard, but others give no such indication. Most all board designers want to meet at a minimum the 8kV level so it's important to understand what ESD level the protection device was measured against. An example of this datasheet waveform is shown in Figure 4 which has the same shape of the input pulse (Figure 1), but it's a dampened or clamped version of it.

Figure 4
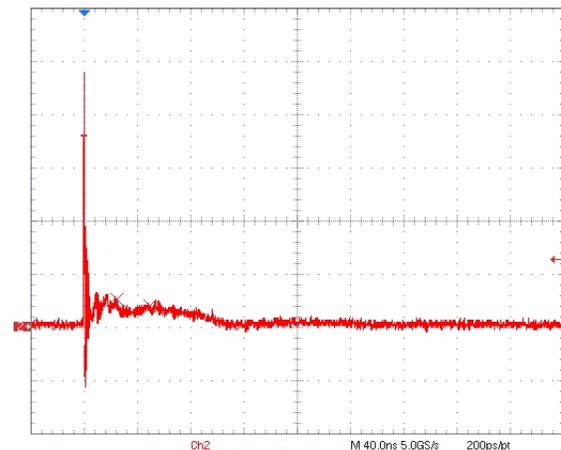
Secondly, there is seldom any mention about the setup these waveforms were captured under. To give the best results, the ESD strike would need to be applied right at the pin of the ESD device to limit the voltage spike generated by any parasitic trace inductance or

$$V_{LP} = L_P \cdot \frac{di}{dt}.$$

These setup conditions are very ideal which rarely occurs in the real world. Correctly designed boards would try to place the ESD device as close as possible to the ESD point of entry, but in any event, there is almost always some distance of PCB trace between the two. *(Note: As little as 1nH of inductance can induce a 30V spike on the PCB trace which is in addition to the actual clamping voltage obtained by the ESD device).*

Lastly, many of the ESD Response waveforms fail to mention the external attenuation or attenuator size that was used to protect the oscilloscope while the measurement was being made. Some datasheets point out the attenuator size used (such as 10x or

100x) which one can easily use to calculate the true clamping voltage; however, some datasheet's give no indication. Therefore, the designer must be cautious of this and never take the "screenshot" voltage as the final clamping voltage he/she can expect from the ESD device.

Outside of the aforementioned electrical characteristics and waveforms, the board designer has very little information to decide which ESD device will give him/her the best performance. The following section will identify a key parameter that can be universally applied to put all ESD devices on equal ground.
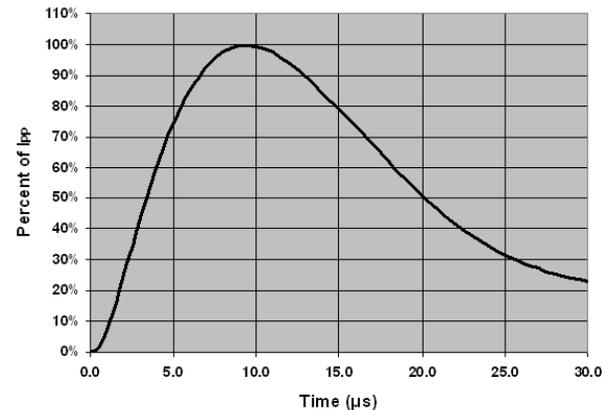
Dynamic Resistance

As mentioned earlier, the ultimate goal of a protection device is to provide the lowest resistance shunt path to GND under an ESD event. Ideally, all current would be steered into the ESD device so that the protected IC would not have to dissipate any of the energy input into the circuit. Figure 5 depicts the ESD protection device as a variable resistor which will be high impedance (low leakage) during normal circuit operation and low impedance during any EOS (Electrical Over Stress) or ESD event.

Figure 5

To IC ← •——○ **ESD Entry**
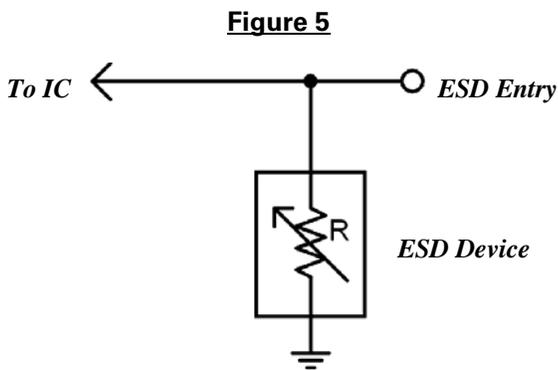
R **ESD Device**

To compare ESD devices and evaluate their effective resistance during an ESD pulse, it is pertinent to remove all outside factors or variables some of which were previously discussed. To that end, there is another standard, IEC61000-4-5, that defines a current pulse (Figure 6) with a much slower leading edge than an ESD pulse. This waveform has an 8µs risetime in comparison to the 1ns risetime of an ESD pulse. This allows any lead or trace inductance to be mitigated so test setups cannot affect the test data, and quite often no external attenuator is needed.

Most ESD vendors include the results of this test on their datasheets either in the electrical table or by means of a plot. Most designers tend to overlook these data points since they are either unfamiliar with the "-4-5" test or believe that an "8/20µs current pulse" is outside the scope of their design.

Figure 6

No matter how the data is presented (electrical table or plot) calculating the dynamic resistance is a simple exercise. First, find two points which include a clamping voltage and current level. It is usually advisable to select the two lowest current levels where internal device heating has the smallest effect. Next, just do the math. The example below uses data taken from the electrical table of Littelfuse's SP3001 series datasheet which is a low capacitance (0.65pF) diode/rail clamp array. In the table, a parameter called "Clamping Voltage" can be found that lists input currents of 1A and 2A which (typically) gives a 9.5V and 10.6V clamp voltage, respectively. Therefore:

$$R_{DYNAMIC} = \frac{10.6V - 9.5V}{2A - 1A} = 1.1\Omega$$

This value is essentially the shunt resistance the ESD device will provide under an ESD pulse. With this simple calculation, the board designer can now effectively evaluate any ESD device on equal ground irrespective of the possible datasheet differences.

Important Considerations

It is usually common practice to think of an ESD pulse in terms of a current pulse. As can be seen in Figure 7, a simplified model of an ESD generator, the voltage on the capacitor (i.e. 8kV) is discharged through a 330Ω resistor into an ESD protection device. The ESD device is typically <10Ω so the "output" of the ESD generator more closely resembles a current pulse as opposed to a voltage spike.

Figure 7
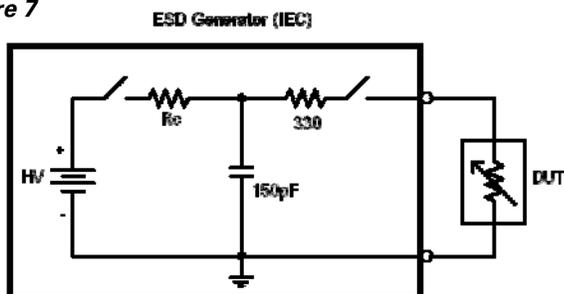
And now going back to Figure 1, an ESD pulse reaches its highest voltage in the first nanosecond and is quickly dissipated thereafter in under 100ns. Table 1 shows the (IEC61000-4-2 specified) relation between the two.

Table 1

IEC Level	Voltage (kV)	Peak Current ±10% (A)	Current @ 30ns (A)	Current @ 60ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

This background was given to help illustrate the point below, that the dynamic resistance can only be used in relative terms or for comparison purposes. For example, take two TVS/Zener ESD devices with the same breakdown voltage (V_Z) but each with a different dynamic resistance. For arguments sake, let's say Device A=1.0Ω and Device B=2.0Ω. Device B will clearly give a higher peak clamping voltage to an 8kV ESD strike.

$$Clamp_A = V_Z + I_{PEAK} * R_{DYN,A} = 6V + 30A * 1.0\Omega = 36V$$

$$Clamp_B = V_Z + I_{PEAK} * R_{DYN,B} = 6V + 30A * 2.0\Omega = 66V$$

These values may not mean much to the board designer as these peak voltages only exist on the data line or input pin for a few nanoseconds. Often the board designer only knows what DC voltage he/she cannot exceed without causing irreparable damage to the IC. So while it's unclear if the very brief existence of 66V on the input will cause damage, it's apparent that Device A will give him/her a far better chance at achieving a successful first pass design.

Conclusions

This paper has given an overview of a couple of ESD topologies and explained the difficulties a designer may face in choosing the correct ESD component for his/her application. Time and again limiting criteria such a parasitic capacitance, standoff voltage, ESD withstand, etc. are not enough to sort through and vet all the possible choices for a suitable protection device.

Using the sometimes overlooked "Clamping Voltage" or "t_P=8/20µs" specification, the board designer can quickly calculate the dynamic resistance of each device to see which one offers him/her the lowest shunt resistance to GND.

Citations/References:
[1] Figure 1 was recreated from the IEC61000-4-2 specification.
[2] Figure 6 was recreated from the IEC61000-4-5 specification.
[3] Figure 7 was recreated from the IEC61000-4-2 specification.
[4] Table 1 was recreated from the IEC61000-4-2 specification.

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