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Application Note:

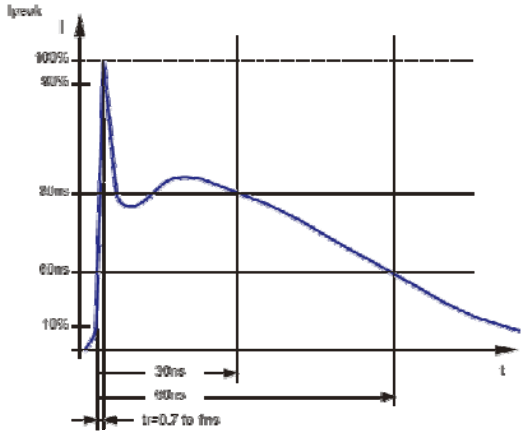
Tips for Enhancing ESD Protection

In the previous white paper, *Selecting an Appropriate ESD Device*, we focused solely on the idea that an ESD device's main goal was to provide the lowest resistance shunt path to GND. And from that idea, we gave the board designer a method from which he/she could calculate the effective resistance of a protection device during an ESD transient. This resistance, or dynamic resistance, could be used to compare and choose the best device from the myriad of ESD parts in the market today. We concluded the paper with the simple premise that the device with the lowest dynamic resistance would give the designer the best chance of a successful first pass design after all other parasitic effects were taken into account.

In this white paper we'll address various techniques a board designer can employ to help him/her attain the ESD level required for their design should the chosen ESD protection devices fail in-system ESD testing.

(Note: Throughout this paper the ESD threat/pulse referenced is defined by the IEC61000-4-2 standard shown below in Figure 1.)

Figure 1



Background

Many of the chipsets today used in modern electronics from LCD TV's to mobile phones are developed in state of the art technologies well below 130nm. These technologies have a minimal tolerance to DC voltages over 3.3V so an ESD pulse can be catastrophic for such a device. Furthermore, requirements for "on-board" or "on-chip" ESD protection have been lowered to 500V, well below the typical field requirement of 8kV.

Therefore, board designers not only need external ESD protection, but they also need to make sure it's robust enough given the vulnerability of the small geometry chipsets. As mentioned in the previous paper, placing an 8kV rated ESD device on the data lines or I/O pins being protected does not guarantee the chipset itself will pass 8kV during in-system testing.

Often times, the ESD device does not provide enough protection by itself causing a premature failure of the chipset. This paper will give a few guidelines the designer can use to enhance his/her on-board ESD protection.

Device Placement and Layout

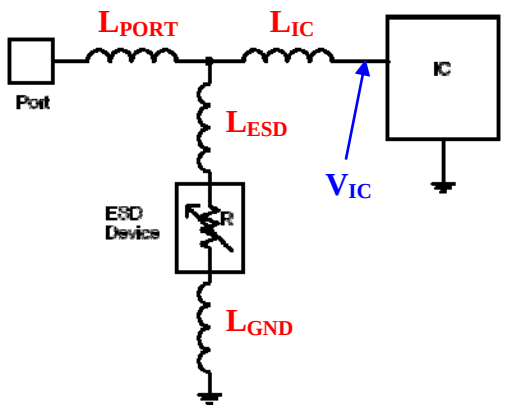
Device location and layout is crucial in getting the maximum effectiveness from an ESD protector. To that end, it's good for the designer to understand the effects that the various parasitic inductances have at the board level. A special focus is given to inductances because an 8kV ESD strike (i.e. 30A) through just 1nH will generate a 30V spike on the PCB trace via the relation:

$$V_{L,Parasitic} = L_{Parasitic} \cdot \frac{di}{dt}.$$

(NOTE: This discussion assumes all ESD threats enter the system through the port seen in Figure 2.)

Four parasitic inductances, L_{ESD}, L_{GND}, L_{IC}, and L_{PORT}, should be considered when deciding on the placement of the ESD device and Figure 2 shows their location.

Figure 2



L_{ESD} and L_{GND} have the effect of increasing the clamping voltage (or V_{IC}) while L_{IC} and L_{PORT} can work to the designer's advantage. We'll start with the two detrimental inductances.

L_{ESD} and L_{GND}

Sometimes a board's layout will not permit an ESD device to be placed directly atop the PCB trace. The reasons vary, but ultimately placing an ESD component even one centimeter away from the data line being protected can translate into tens of volts very quickly. The same is true for GND buses. In some designs the ESD device's GND must pass through multiple vias and even take a circuitous path to reach the GND plane. Both of these inductances create voltage spikes in addition to the voltage created by the ESD current flowing through the ESD device (i.e. I_{PEAK} * $R_{DYNAMIC}$).

The following simplified example will show the effect L_{ESD} and L_{GND} can have on V_{IC}. Before we give that example, it should be pointed out that common PCB manufacturing processes give approximately 3nH/cm for a typical microstrip traces (assuming certain widths, thicknesses, and dielectric constants).

With that in mind, let's assume for this example an 8kV ESD pulse and an ESD device with a dynamic resistance of 1Ω. Furthermore, let's look at two different layouts, Layout A and Layout B, with L_{ESD}=L_{GND}=1.5nH (0.5cm each) and L_{ESD}=L_{GND}=3.0nH (1.0cm each), respectively.

Layout A

$$V_{IC} = L_{ESD} * \frac{dI}{dt} + L_{GND} * \frac{dI}{dt} + I_{PEAK} * R_{DYNAMIC}$$

$$V_{IC} = 3nH * \frac{30A}{1ns} + 30A * 1.0\Omega = 120V$$

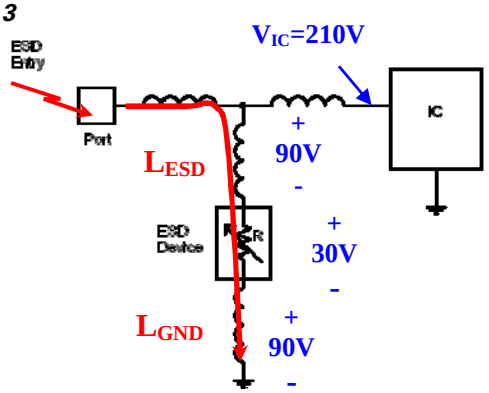
Layout B

$$V_{IC} = L_{ESD} * \frac{dI}{dt} + L_{GND} * \frac{dI}{dt} + I_{PEAK} * R_{DYNAMIC}$$

$$V_{IC} = 6nH * \frac{30A}{1ns} + 30A * 1.0\Omega = 210V$$

Therefore, just increasing the trace lengths (i.e. L_{ESD} and L_{GND}) from 0.5cm to 1cm can translate in a 75% increase of V_{IC}! Figure 3 shows Layout B, and the voltages associated with each element.

Figure 3

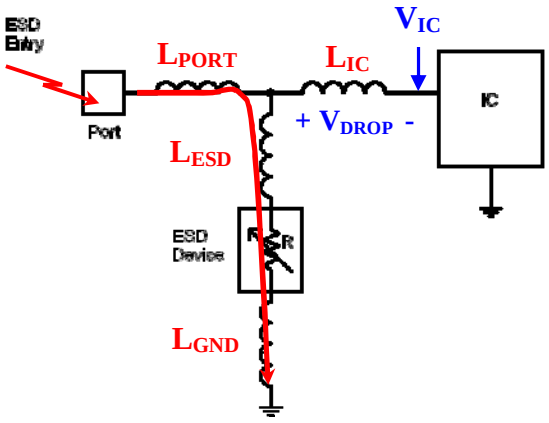


L_{IC} and L_{PORT}

In many ESD device datasheets, it's often stated to put the device as close as possible to the point of ESD entry. This is done so that the ratio of L_{PORT} to L_{IC} is as small as possible (i.e. L_{IC}>>L_{PORT}). The inductance of L_{PORT} will not necessarily affect the overall ESD performance but the inductance of L_{IC} most certainly will.

The non-linearity of L_{IC} will act as a buffer to the initial peak current of the ESD pulse by providing a substantial voltage drop "toward" the IC. As this inductance gets smaller (i.e. the ESD device is located closer and closer to the IC) the voltage drop continually decreases to the point were no additional advantage is gained. So it's in the designer's best interest to make the ratio of L_{PORT} to L_{IC} as small as possible to take advantage of the parasitic nature of the PCB trace. Figure 4 shows the voltage drop we are referring to.

Figure 4



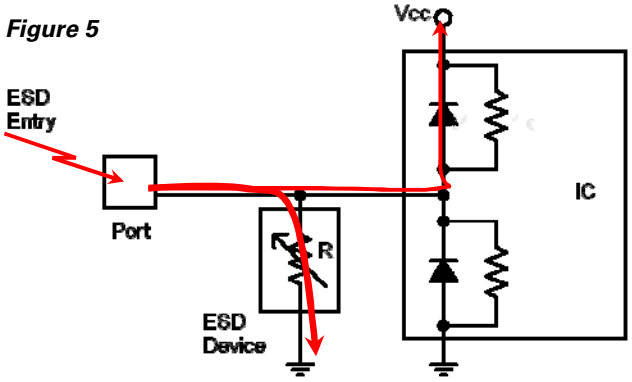
Taking advantage of L_{IC} and L_{PORT}, are straightforward ways to improve the overall ESD performance. There are designs, however, that will still fail prematurely no matter how low the aforementioned ratio is made. In other words, the value of L_{IC} does not provide a sufficient buffer to the peak ESD current.

Buffer Resistors

Occasionally, employing the previous techniques is not enough to get the maximum ESD protection for a given board design. The reason is that the "on-chip" ESD structures see too much current and they become damaged shorting the I/O to GND or V_{CC}.

Figure 5 helps to make this clearer in showing that the ESD device and the IC being protected actually share the current load from an ESD pulse. The figure (minus trace inductances) is shown for a positive ESD pulse where the protection device takes the majority of the current, but it's essentially a resistive divider with the IC. *(Note: The IC is shown to have diode clamps to the two rails, but the on-chip protection could be any other ESD structure such an SCR. The intent is to show that any on-chip ESD structure has some equivalent resistance in parallel with the ESD device.)*

Figure 5



As Figure 5 shows, the rail diode on the IC is responsible for steering the remaining or "let-through" current into V_{CC} (which typically returns to GND through a bypass capacitor). It's hard to determine what the equivalent resistance will be for the IC's ESD protection, but it's undoubtedly much higher than the on-board ESD device.

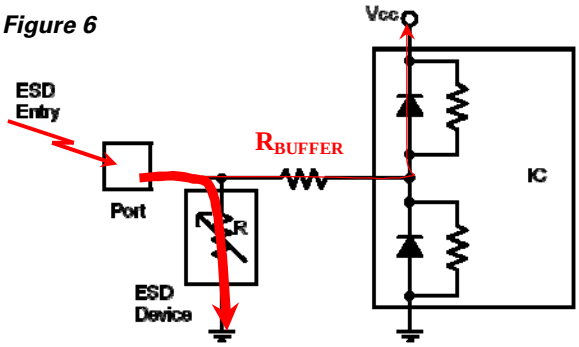
If, for example, the resistance was 10Ω for the on-chip protection (R_{CHIP}), and the $R_{DYNAMIC}$ for the external ESD protector was 1Ω, the peak current seen by the IC would be:

$$I_{IC} = \frac{R_{DYNAMIC}}{R_{DYNAMIC} + R_{CHIP}} * I_{PEAK} = \frac{1\Omega}{1\Omega + 10\Omega} * 30A$$

$$I_{IC} = 2.73A$$

To help decrease the peak current flow into the IC, resistors can be added in series between the external ESD device and the IC as in Figure 6 below.

Figure 6



By adding a 10Ω buffering resistance, the peak current flowing into the IC can be reduced by almost 50% (for this example).

$$I_{IC} = \frac{R_{DYNAMIC}}{R_{DYNAMIC} + R_{BUFFER} + R_{CHIP}} * I_{PEAK}$$

$$I_{IC} = \frac{1\Omega}{1\Omega + 10\Omega + 10\Omega} * 30A$$

$$I_{IC} = 1.43A$$

Obviously, the resistance could be increased beyond 10Ω to further reduce the let-through current, and often the maximum resistance will be determined by the particulars of the application.

It should also be noted that extra care must be taken when employing this technique in some of the high-speed applications such as HDMI™ and USB3.0. The R_{BUFFER} resistor would disturb the line impedance and attenuate the signal beyond the two standard's compliance specifications, but careful board design can compensate for any ill effects. Nevertheless, board designers should keep this technique in their tool box and apply it in situations where the board or in-system ESD level falls below their requirement.

Conclusions

Modern chipsets are more susceptible today than ever before to damage from ESD transients. Due to their small geometry technologies, these IC's need robust, external ESD solutions to survive in-system ESD testing.

This paper has given four strategies or procedures a board designer can use to optimize their ESD solution.

1. Reduce the length of the parasitic "stub" trace or L_{ESD}.
2. Reduce the length of the GND trace and/or number of vias used to decrease L_{GND}.
3. Make the ratio of L_{IC} and L_{PORT} as small as possible on a given design.
4. Use buffering resistors between the ESD device and IC if 1-3 above are not sufficient.

All of these practices aim to reduce the voltage seen by the IC, as well as, limit the amount of current the on-chip ESD structures must handle. Following these simple rules will give the board designer a more robust ESD solution capable of exceeding industry standards.

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Citations/References:

[1)] Figure 1 was recreated from the IEC61000-4-2 specification.

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