APPLICATION
NOTES

Protecting the Universal Serial Bus from Over Voltage and Overcurrent Threats

This application note addresses the various requirements for protecting the Universal Serial Bus (USB) from overcurrent and over voltage environmental threats. The solutions presented cover both USB 1.1 and the higher speed USB 2.0 circuitry. Specific emphasis is placed on USB 2.0 with information directed at hot connection over current conditions and electrostatic discharge (ESD) induced in the USB system.

The USB Standard

The USB specification provides a uniform protocol for the addition and configuration of computer peripherals. USB is designed around one uniform port size and a matching connector. It uses the concept of a single host and multiple hubs designed to provide uniform and simple methods for adding and connecting various peripherals. The goal of USB is to reduce the number of cable connections and configurations. A single USB port has the capability of driving up to 127 USB peripherals such as mice, modems and keyboards (see Figure 1). Additionally, a single hub permits the connection of several USB devices by providing power through the communication cable itself, eliminating the need for individually powered peripherals. It also allows mixed high-speed communications between USB and other protocols such as Ethernet, DSL, ISDN or satellite communications

USB is an external bus standard that supports data transfer rates of up to 12Mbps for USB 1.1 and 480Mbps for the new USB 2.0 standard. USB also supports Plug-and-Play installation and hot plug operation.

USB 2.0 addresses the evolution to higher data transmission rates between computers and peripherals or networked LAN or WAN systems. Recent data protocols now reach millions to billions of characters per second.

The integrated circuits required to support this high-speed technology become increasingly complex, shrinking feature size and making them more susceptible to over current and over voltage occurrences.

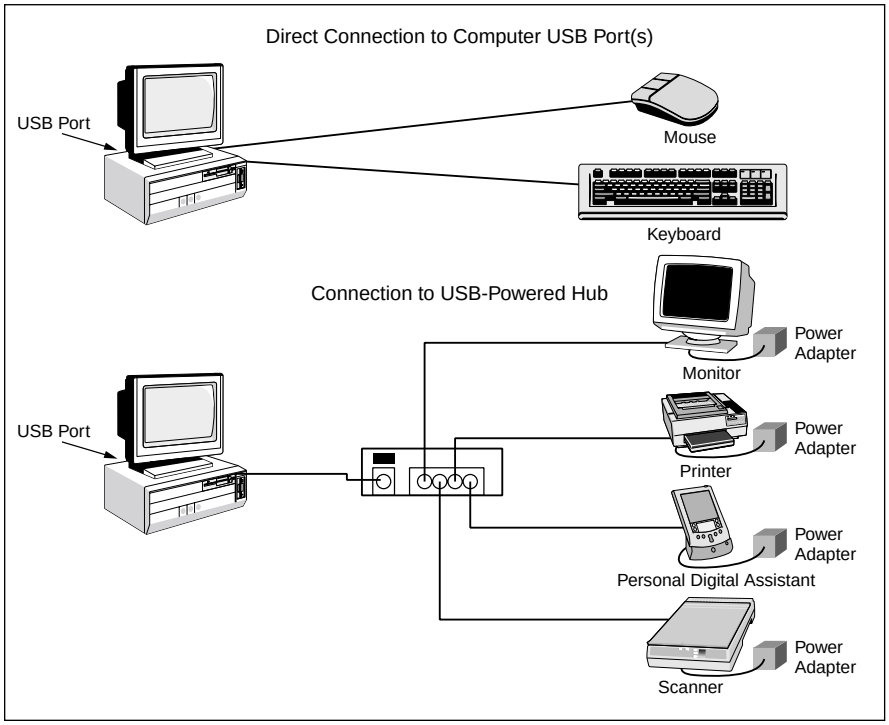

Figure 1. Typical USB communication structures.

Over current Protection for USB Power Rails

The USB port consists of four lines - two data lines (D+ and D-), Vbus and GND. which connect the USB Hub to the USB peripheral. Overcurrent protection is not normally required on the two data lines or GND.

USB ports can be configured two different ways: As Self-powered ports or Bus-powered ports. A Self-powered USB Hub must have the capability to source up to 500mA on Vbus on all of its ports. A Bus-powered Hub does not draw power from the USB stream, but may utilize up to 100ma from upstream devices or hubs to allow for functionality of the hub when it is powered down.

Bus-powered Hubs can draw up to 500mA from an upstream self-powered connection. Typically 100mA is available for functions and processors internal to the hub. External ports in a Bus-powered Hub can supply up to 100mA per port, with a maximum of 4 ports per hub.

USB Bus Transceiver ICs or Power Management ICs may include current limiting functions that satisfy USB requirements, however, when the ICs do not include current limiting features, are cost prohibitive, or supplemental protection is required, the circuit designer may choose external passive current limiting elements for Vbus.

There is a choice of two low cost technologies for developing over current protection circuitry. The traditional fuse and the Polymer-based PTC (positive temperature coefficient) device are the most common. Understanding differences between these two components facilitates choosing the best protection device for a specific application.

Fuses are "one time" devices, since they provide protection from the overload by opening only once, after which they must be replaced. The heart of a traditional fuse is a metal element, which is heated to its melting point by the excessive current. The circuit current flow drops to zero as the element melts open.

The PTC also reacts to excessive current, but it is self "re-settable". The conductive polymer inside the device increases in resistance when heated by the overload, thereby limiting the circuit current.

PTC Protection Function

The PTC functions by limiting potentially damaging over currents if they exceed the specified device rating. Heat caused by the over current condition produces thermal expansion in the polymer material. As the polymer expands, it becomes more resistive thereby reducing and limiting the current flowing through it to a safe level. The increase in resistance is non-linear and occurs when the operating current exceeds the "trip point." Once the PTC has reached its trip point, its resistance will remain high until the power source is removed. Figure 2 illustrates a typical resistance vs. temperature curve of PTC devices. The PTC element usually cuts the current to the circuit as a result of a very small change in temperature. The current limiting function occurs at the point when the resistance of the PTC element matches the impedance of the circuit. This is also the peak of the power dissipated in the PTC element.

PTC's are offered in many different sizes, operating voltages and amperage ratings. The Littelfuse 1812L Series, measuring only 0.179" x 0.127", is the size of choice for most computer designers. Littlefuse has recently released its 1206L series of PTCs. This product allows designers to provide single–port protection for ratings up to 1.5A while utilizing 1/3 of the onboard space of an 1812L PTC[1]. The 3425L Series of PTCs are also used by computer manufacturers due to their surface mount packaging and cost competitiveness relative to other solutions for USB power management.

[1]The 1206L series is available in ratings ranging from .5A to 1.5A. Samples are available by contacting electronics@littlefuse.com. (UL,CSA,TÜV approvals pending.)

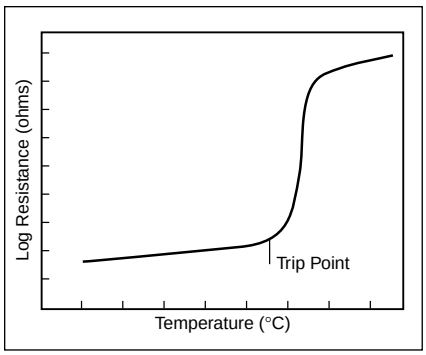

Figure 2. PTC's resistance as a function of temperature.

Protection of USB Power Rails with a PTC

Various manufacturers implement designs for USB power management using PTCs. Some manufactures use a lower amperage device for individual protection of each port. This individual-port solution provides excellent protection since each single port can be isolated. Other manufacturers protect multiple ports on a bus with a single higher amperage device, thereby creating a lower-cost solution. The higher amperage solution will be somewhat less sensitive to marginal over current conditions than the individually protected port solutions.

Figure 3 illustrates the placement of the PTC element (1206L OR 1812L Series). (The over voltage suppression devices are shown on the same figure and will be described in a later section.)

When designing these USB ports, the engineer must insure that the voltage drop does not fall below 4.75V for a Self-powered Hub port or 4.40V for a Bus-powered Hub port. The upstream voltage supplied to a Bus-powered Hub is 4.75. To demonstrate that Littelfuse® PTC devices meet these requirements, voltage drop calculations are shown on the Sample Calculations page of this document for several USB port protection applications.

The calculations for bus-powered hubs include a resistance budget for the connecting cable. The USB specification specifies that the connection cables for host to hub and peripherals have a maximum length of 5 meters and a maximum resistance of 190mohms. The circuit trace was assumed to be 4 inches with a trace resistance of 5mohms/inch. Bus-powered circuits include control logic circuitry, which enables software control of bus power and port reset capabilities. The voltage drop for over current protection with PTC devices easily meets the requirements in the USB specifications.

Overcurrent circuit protection scenarios for the Self-powered hubs and Bus-powered hubs depict individual port and multiple (ganged) port protection (Figures 4-7) Individual port protection offers advantages over ganged port protection; if one port fails, the other ports are unaffected. Additionally, knowledge of the time-to-trip parameter allows the design engineer to eliminate false circuit trips due to power-on-currents.

Over voltage Suppression of the USB Power Rails

Transient over-voltage suppression of the USB power supply rails (Vbus and Signal GND) is achieved in these circuits with the addition of two multilayer varistors (MLVs) and is illustrated as ML1,2 in Figure 3. Figures 4-7 also depict a varistor in several port configurations for the protection of Vbus. A Littelfuse V5.5MLA0603 MLV is shown in all examples.

Data signal ground (GND) and Vbus transients must be suppressed. Good layout practices prescribe that data signal ground

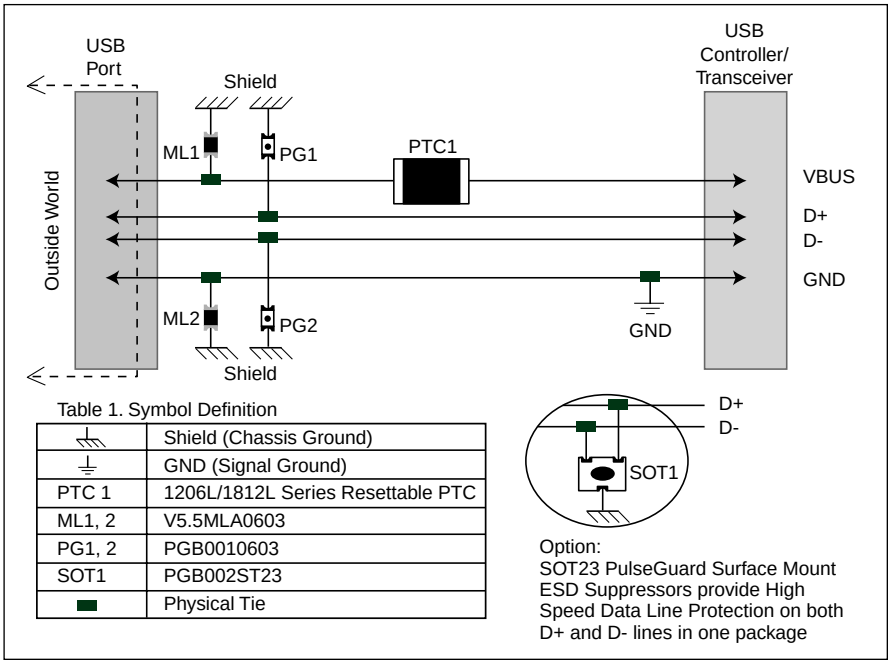

Table 1. Symbol Definition

⏚	Shield (Chassis Ground)
⏚	GND (Signal Ground)
PTC 1	1206L/1812L Series Resettable PTC
ML1, 2	V5.5MLA0603
PG1, 2	PGB0010603
SOT1	PGB002ST23
▬	Physical Tie

Figure 3. USB 2.0 port protection reference design.

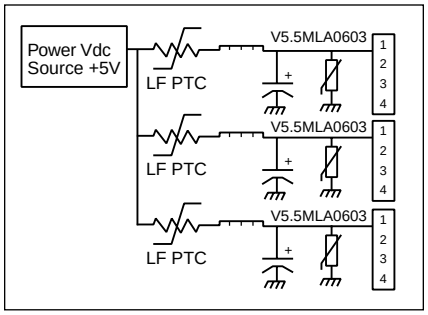

Figure 4. Self powered hub individual port protection.

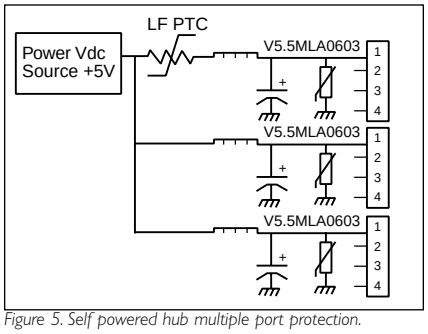

Figure 5. Self powered hub multiple port protection.

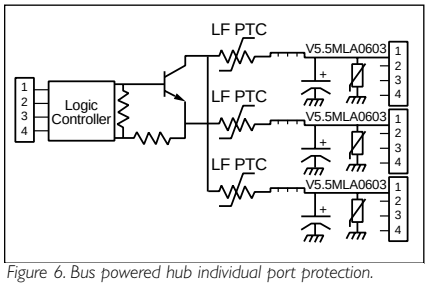

Figure 6. Bus powered hub individual port protection.

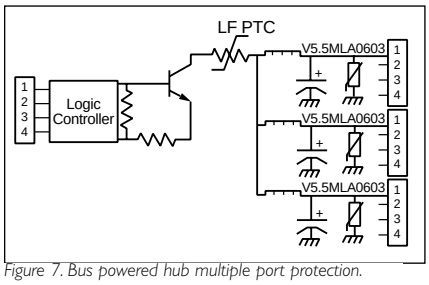

Figure 7. Bus powered hub multiple port protection.

and chassis ground should not be tied together at the board level. This may allow transients to propagate via signal ground with respect to chassis ground, especially while the board is being handled or when a USB cable is inserted.

The V5.5MLA0603 device was chosen for transient suppression of the Vbus and GND for several reasons. First, since board real estate is always a consideration, a small 0603 size device was chosen. This device has a continuous DC voltage rating of 5.5Vdc, consistent with the 5V USB power supply. The MLVs are fully cable of handling ESD transients or higher energy threats (EFT, lightning remnants, etc). Since we are protecting a dc bus, added capacitance is useful. The V5.5MLA0603 device has a typical capacitance of 660pF.

ESD Protection of USB Data Lines

ESD protection should be an integral part of the USB design process. While USB Transceiver ICs will have some level of protection on the chip, additional protection is required to augment immunity. While many ICs are specified to ESD levels of 1-4kV per Mil-STD-883, Method 3015, they may have little or no capability to the Human Body Model (HBM) standard IEC-61000-4-2. The two standards have very different test methods. Additionally, ESD discharge transients are very fast events, which may reach peak voltages in sub nanosecond time frames, and peak voltages and currents can reach 25kV and 100A, respectively. Transients of this magnitude or lower can cause gate oxide ruptures or other silicon damage, transmission signal degradation, loss of stored data and equipment latch-up.

An ESD suppressor is a circuit protection component that reduces the ESD transient to a level which prevents damage to electronic components. The suppressor is installed from line to ground and shunts most of the ESD energy to ground. The remaining energy is either dissipated within the suppressor or is reflected back towards the source of the ESD event. Figure 3 illustrates how an ESD suppressor is incorporated into USB data line circuitry.

The Littelfuse PulseGuard® ESD suppressor utilizes a polymer composite voltage-variable material exhibiting a highly nonlinear resistance response to applied voltage. Under normal circuit operating conditions, the ESD suppressor exhibits a high resistance and remains transparent to the circuit. When an ESD transient develops, the suppressor resistance drops sharply. This low resistance path redirects most of the ESD energy away from the circuit. After the energy is dissipated, the suppressor automatically returns to its normal high-resistance state.

USB 2.0, 480Mbps waveforms can be distorted by any added capacitance. Littelfuse PulseGuard® surface mount ESD suppressors present almost no capacitive loading to the circuit with a typical capacitance of 0.05pF. Higher capacitance surge suppression devices distort the data waveform rounding the leading and trailing edges. Figure 10 illustrates how a digital wave shape is altered during its transition between high and low logic states if the capacitance of the surge suppression element is too large.

Data recorded for Figures 8-10 illustrate the effect capacitance has on a digital waveform similar to a USB signal. Figures 8 and 9 show the effect on a digital pulse train at 6MHz and 240MHz, respectively. Since USB utilizes a differential pair, a bit change can occur as often as every half cycle, therefore, a square wave at frequencies of 6MHz and 240MHz were used to generate the data. Figure 10 shows the effect capacitance has on a typical USB rise time.

Each figure shows five curves representing different loads - No load, PulseGuard suppressor (0.05pF), 1pF Capacitor, 10pF Capcitor, and a Multilayer Varistor (660pF). As can be expected, the device with the lowest capacitance, the Pulse Guard suppressor, provides the lowest level of signal distortion. The benefit of Pulse Guard suppressors are more apparent at the

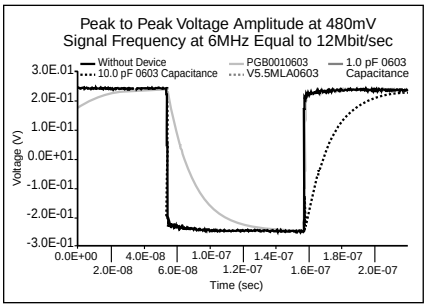

Figure 8. Capacitive loading effects on USB 1.1 signal.

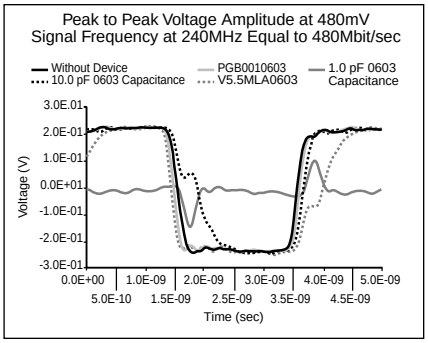

Figure 9. Capacitive loading effects on USB 2.0 signal.

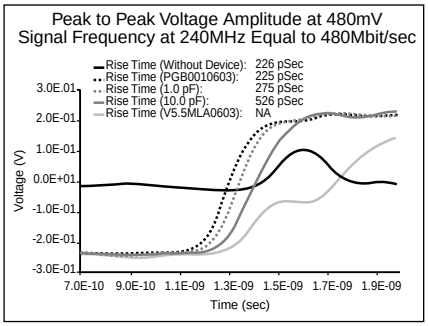

Figure 10. 10-90% USB signal rise time response of several loads.

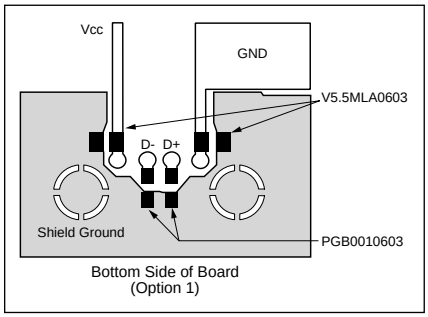

Figure 11a: Option 1 layout for 0603 case style PulseGuard Supressor and MLVs.

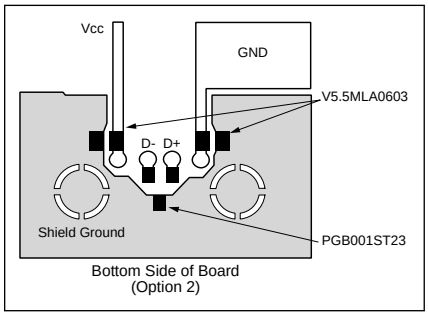

Figure 11b. Option 2 layout for SOT-23 case style PulseGuard Suppressor and MLVs.

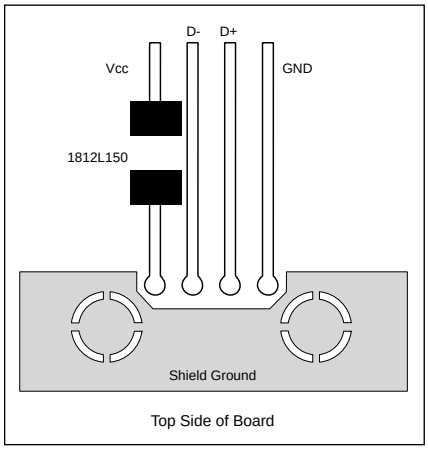

Figure 12. Top view of Layout showing Polymer PTC pads.

higher USB 2.0 rates (480Mbps) as there is almost no effect to the waveform or rise time. Low capacitance TVS (Transient Voltage Suppression) diodes in the 3-60pF range would show appreciable capacitive loading effects.

Off-state leakage currents are another consideration when choosing an ESD suppressor. This is especially important in portable applications where batteries are used to supply circuit power. The ESD suppressor leakage currents must be minimized for maximum battery life. The leakage current for a PulseGuard® ESD suppressor is <1 nA, which is much less than the amount for a TVS (Transient Voltage Suppression) diode (0.1-20microamp).

The chassis or shield ground of the system is the recommended ESD surge suppressor ground return (see Figure 3.), not the signal ground (GND). The design objective is to force the ESD currents flowing on the data or GND directly to the chassis and or shield. By returning the ESD currents to the chassis ground we effectively accomplish the following:

* Any ESD event entering the shield of the USB cable, the USB device housing, or connector will be shunted to the external shielding of the USB host or possibly to the shield of the computer containing the USB port preventing current from coupling into the data lines.
* Lowers the likelihood of an ESD generated upset.
* Electric fields resulting from the ESD event do not reach internal circuitry.
* Energy in the ESD transient gets reflected back towards the ESD generator (i.e., the human or other charged structure).

Figure 11 shows two possible printed circuit board structures. The first uses the 0603 PulseGuard® suppressor case style and the second uses the SOT-23 case style. Both options show the pad layout for the MLVs.

Figure 12 shows the physical layouts for the top of the USB port.

Summary

The USB standards present a means to improve serial data communication. As with any bus architecture, the threat from fault currents and induced voltage transients exist. Littelfuse offers a variety of technologies to address these situations. Highlighted in this note is Littelfuse PTCs for over current and Pulseguard® suppressors for ESD.

The Polymer PTCs and Zinc Oxide MLVs have been shown to effectively reduce over current and transient over voltage events, respectively, on the USB Power Rails.

In order to maintain the signal integrity on the high-speed USB 2.0 data lines, the designer must take into consideration the addition of any inserted capacitance. Littelfuse PulseGuard® suppressors provide the necessary ESD suppression while at the same time have negligible capacitance of their own.

Bibliography and References

1. Jim Colby, The ESD Problem
2. Hyatt, et al, ESD Symposium paper 1, 2000
3. Hyatt et al, ESD Symposium paper 2, 2000
4. Littelfuse, Protecting Universal Serial Bus (Reference design)
5. Hyatt, ESD Symposium (resistive phase paper)
6. Littelfuse Suppression Products Databook, DB450.5
7. Littelfuse, Electronic Designer's Guide, EC101-F

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FORM NO. EC606 Printed in U.S.A. MARCH 2001