Features

- ESD Protect for 1 Line with Uni-directional
- Provide ESD protection for the protected line to
  IEC 61000-4-2 (ESD) ±30kV (air/contact)
  IEC 61000-4-4 (EFT) 80A (5/50ns)
  IEC 61000-4-5 (Lightning) 4A (8/20μs)
  Cable Discharge Event (CDE)
- Ultra-small SOD-523 package saves board space
- Protect one I/O line or one power line
- Fast turn-on and Low clamping voltage
- For low operating voltage applications: 3.3V maximum
- Solid-state silicon-avalanche and active circuit triggering technology
- Green Part

Applications

- Hand Held Portable Applications
- Computer Interfaces Protection
- Microprocessors Protection
- Serial and Parallel Ports Protection
- Control Signal Lines Protection
- Power lines on PCB Protection
- Latchup Protection

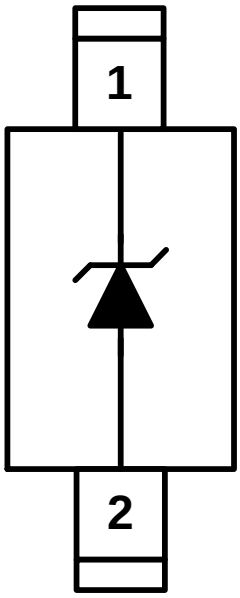
Description

AZ5013-01H is a design which includes a unidirectional surge rated clamping cell to protect one power line, or one control line, or one low speed data line in an electronic systems. The AZ5013-01H has been specifically designed to protect sensitive components which are connected to power and control lines from over-voltage damage and latch-up caused by Electrostatic Discharging (ESD), Electrical Fast Transients (EFT), Lightning, and Cable Discharge Event (CDE).

AZ5013-01H is a unique design which includes proprietary clamping cell in a single package. During transient conditions, the proprietary clamping cell prevents over-voltage on the power line or control/data lines, protecting any downstream components.

AZ5013-01H may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 (±15kV air, ±8kV contact discharge)

Circuit Diagram / Pin Configuration



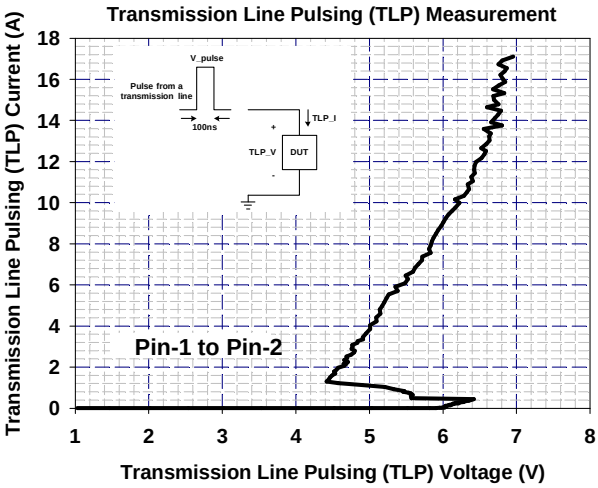
SOD-523 (Top View)

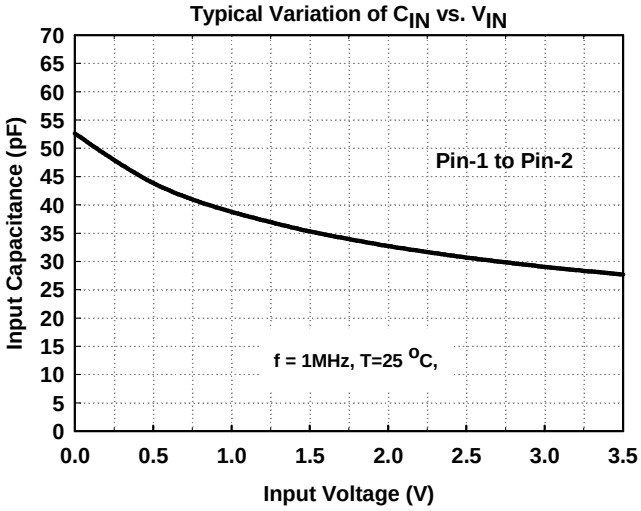
SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS			
PARAMETER	**PARAMETER**	**RATING**	**UNITS**
Peak Pulse Current (tp =8/20us)	I_{PP}	4	A
Operating Supply Voltage (pin-1 to pin-2)	V_{DC}	3.8	V
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD}	±30 ±30	kV
Lead Soldering Temperature	T_{SOL}	260 (10 sec.)	°C
Operating Temperature	T_{OP}	-55 to +85	°C
Storage Temperature	T_{STO}	-55 to +150	°C

ELECTRICAL CHARACTERISTICS						
PARAMETER	**SYMBOL**	**CONDITIONS**	**MINI**	**TYP**	**MAX**	**UNITS**
Reverse Stand-Off Voltage	V_{RWM}	T=25 °C.			3.3	V
Reverse Leakage Current	I_{Leak}	V_{RWM} = 3.3V, T=25 °C.			1	μA
Reverse Breakdown Voltage	V_{BV}	I_{BV} = 1mA, T=25 °C.	4.5		6.5	V
Forward Voltage	V_F	I_F = 15mA, T=25°C.	0.6	0.85	1	V
ESD Clamping Voltage	V_{ESD_CL}	IEC 61000-4-2 +6kV, T=25 °C, Contact mode.		7		V
Channel Input Capacitance	C_{IN}	V_R= 0V, f = 1MHz, T=25 °C		55	65	pF

Typical Characteristics





Applications Information

The AZ5013-01H is designed to protect one line against System ESD/EFT/Lightning pulses by clamping them to an acceptable reference.

The usage of the AZ5013-01H is shown in Fig. 1. Protected lines, such as data lines, control lines, or power lines, are connected at pin 1. The pin 2 should be connected directly to a ground plane on the board. All path lengths connected to the pins of AZ5013-01H should be kept as short as possible to minimize parasitic inductance in the board traces.

In order to obtain enough suppression of ESD induced transient, good circuit board is critical. Thus, the following guidelines are recommended:

- Minimize the path length between the protected lines and the AZ5013-01H.
- Place the AZ5013-01H near the input terminals or connectors to restrict transient coupling.
- The ESD current return path to ground should be kept as short as possible.
- Use ground planes whenever possible.
- NEVER route critical signals near board edges and near the lines which the ESD transient easily injects to.

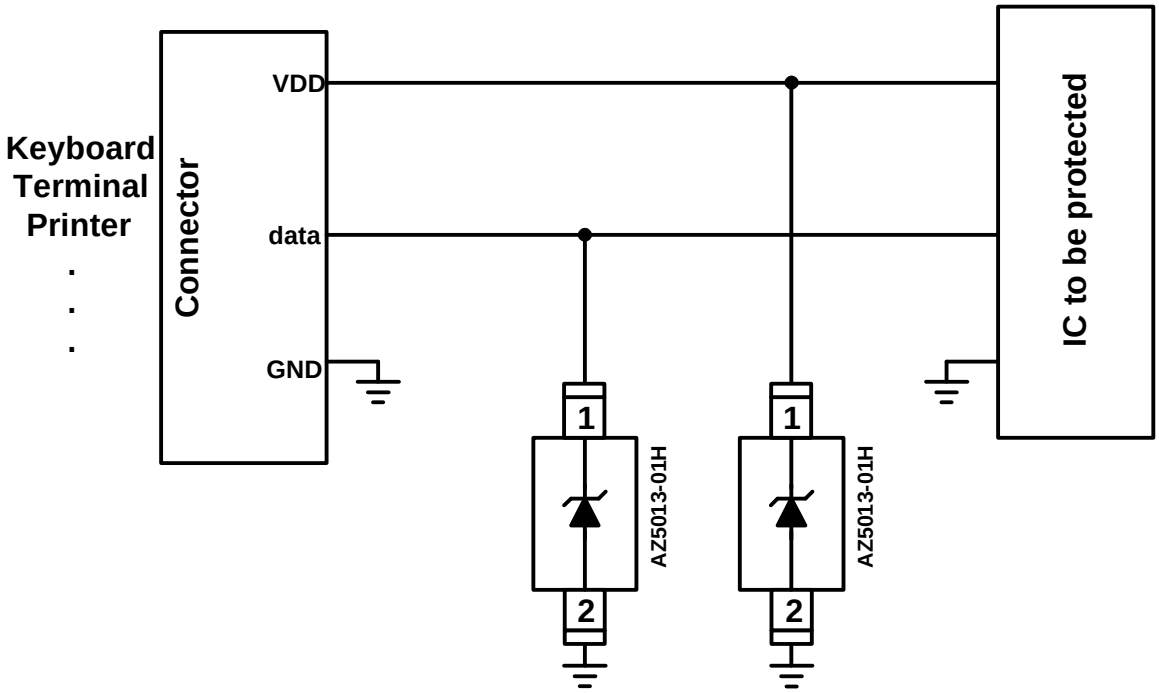


Fig. 1

Fig. 2 shows another simplified example of using AZ5013-01H to protect the control lines, low speed data lines, and power lines from ESD transient stress.

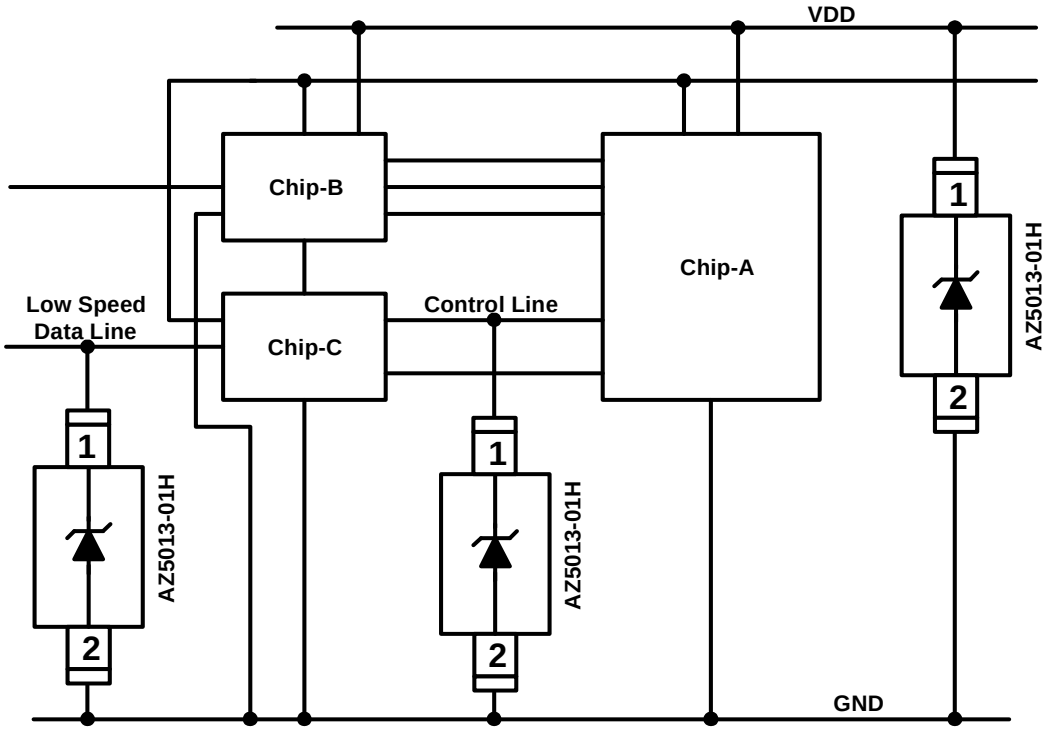
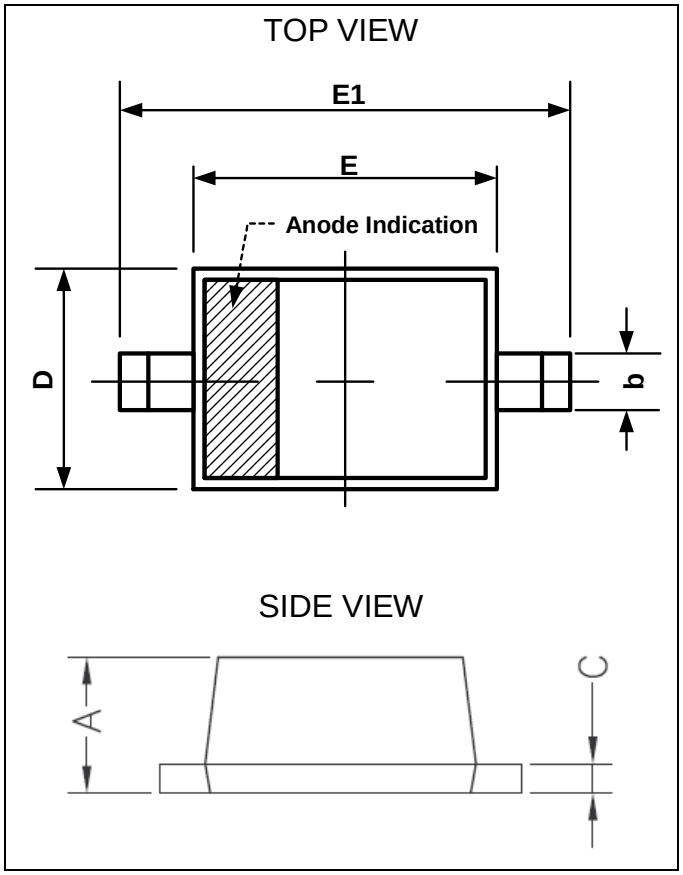


Fig. 2

Mechanical Details

SOD-523

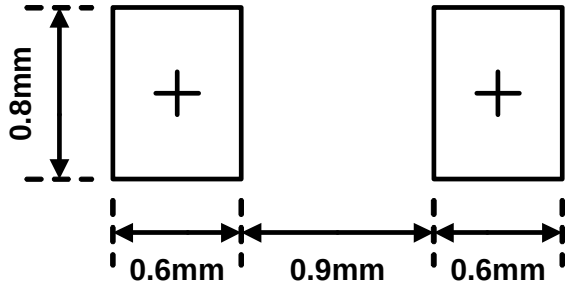
PACKAGE DIAGRAMS



PACKAGE DIMENSIONS

Symbol	Millimeters		Inches	
	MIN.	MAX.	MIN.	MAX.
A	0.5	0.77	0.020	0.030
B	0.25	0.35	0.010	0.014
C	0.08	0.2	0.003	0.008
D	0.7	0.9	0.028	0.035
E	1.1	1.3	0.043	0.051
E1	1.5	1.7	0.059	0.067

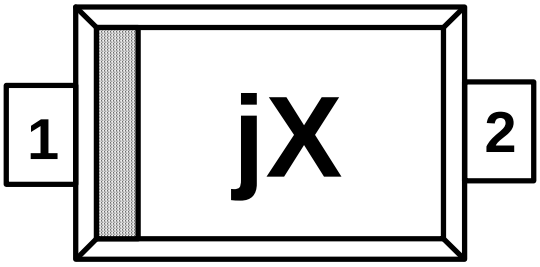
LAND LAYOUT



Notes:

This LAND LAYOUT is for reference purposes only. Please consult your manufacturing partners to ensure your company's PCB design guidelines are met.

MARKING CODE



j = Device Code
X = Date Code

Part Number	Marking Code
AZ5013-01H	jX

Revision History

Revision	Modification Description
Revision 2010/02/10	Formal Release.
Revision 2010/02/17	Update the PACKAGE DIMENSIONS.