

Features

- ESD Protect for 2 Lines with Bi-directional
- Provide ESD protection for the protected line to IEC 61000-4-2 (ESD) $\pm 15\text{kV}$ (air), $\pm 15\text{kV}$ (contact) IEC 61000-4-4 (EFT) 40A (5/50ns) Cable Discharge Event (CDE)
- Small SOT23-3L package saves board space
- Protect two I/O lines or two power lines
- Fast turn-on and Low clamping voltage
- Low operating voltage: 5V
- Solid-state silicon-avalanche and active circuit triggering technology
- Green Part

Applications

- Computer Interfaces Protection
- Microprocessors Protection
- Serial and Parallel Ports Protection
- Control Signal Lines Protection
- Power lines on PCB Protection
- Latchup Protection

Description

AZ5125-02S is a design which includes two bi-directional ESD rated clamping cells to protect two power lines, or two control lines, or two low speed data lines in an electronic systems. The AZ5125-02S has been specifically designed to protect sensitive components which are connected to power and control lines from over-voltage damage and latch-up caused by Electrostatic Discharging (ESD), Electrical Fast Transients (EFT), and Cable Discharge Event (CDE).

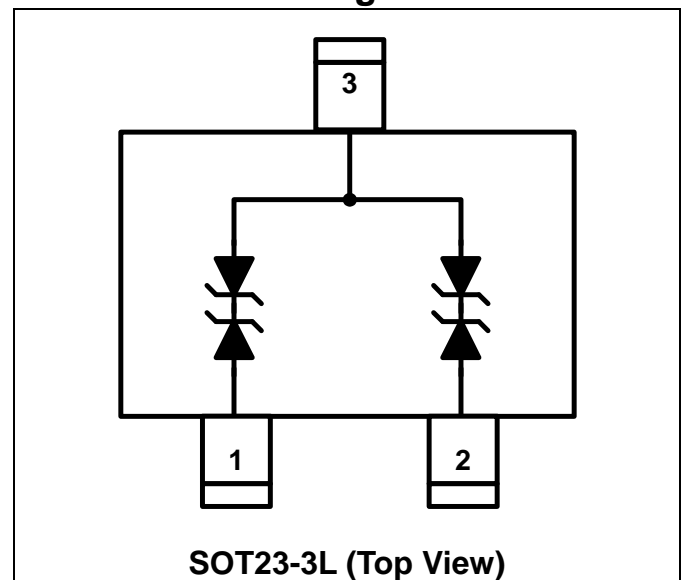
AZ5125-02S is a unique design which includes proprietary clamping cells in a single package. During transient conditions, the proprietary clamping cells prevent over-voltage on the power

lines or control/data lines, protecting any downstream components.

AZ5125-02S is bi-directional and may be used on lines where the signal swings above and below ground.

AZ5125-02S may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 ($\pm 15\text{kV}$ air, $\pm 8\text{kV}$ contact discharge).

Circuit Diagram / Pin Configuration

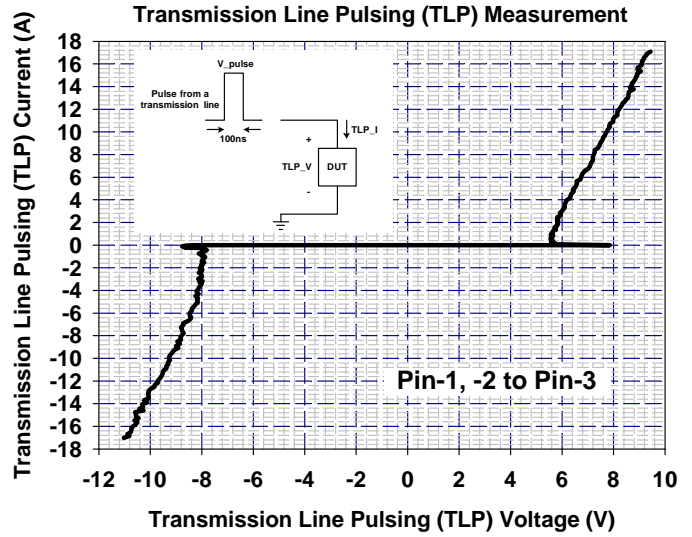
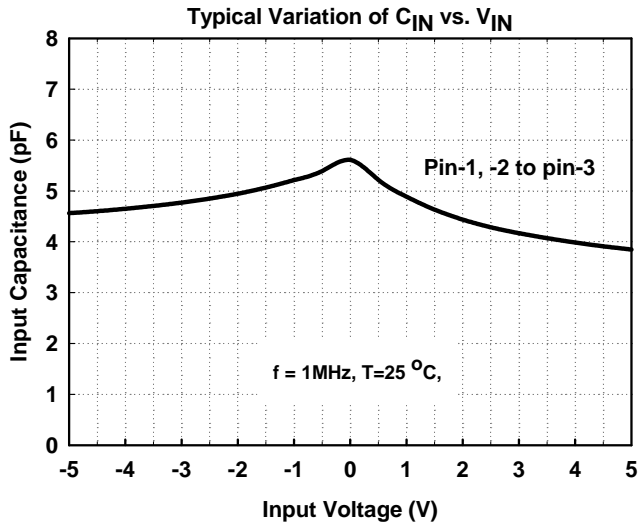


SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS			
PARAMETER	PARAMETER	RATING	UNITS
Operating Supply Voltage (pin-1,-2 to pin-3)	V_{DC}	± 5.8	V
ESD per IEC 61000-4-2 (Air)	V_{ESD}	± 15	kV
ESD per IEC 61000-4-2 (Contact)		± 15	
Lead Soldering Temperature	T_{SOL}	260 (10 sec.)	$^{\circ}C$
Operating Temperature	T_{OP}	-55 to +85	$^{\circ}C$
Storage Temperature	T_{STO}	-55 to +150	$^{\circ}C$

ELECTRICAL CHARACTERISTICS						
PARAMETER	SYMBOL	CONDITIONS	MINI	TYP	MAX	UNITS
Reverse Stand-Off Voltage	V_{RMM}	$T=25^{\circ}C$	-5		5	V
Reverse Leakage Current	I_{Leak}	$V_{RMM} = \pm 5V, T=25^{\circ}C.$			1	μA
Reverse Breakdown Voltage	V_{BV}	$I_{BV} = 1mA, T=25^{\circ}C.$	5.8		9	V
ESD Clamping Voltage	V_{ESD_CL}	IEC 61000-4-2 +6kV, $T=25^{\circ}C,$ Contact mode		11.5		V
Channel Input Capacitance	C_{IN}	$V_R = 0V, f = 1MHz, T=25^{\circ}C.$		6	8	pF

Typical Characteristics



Applications Information

The AZ5125-02S is designed to protect two lines against System ESD/EFT/Cable-Discharging pulses by clamping them to an acceptable reference. It provides bi-directional protection.

The usage of the AZ5125-02S is shown in Fig. 1. Protected lines, such as data lines, control lines, or power lines, are connected at pin 1 and pin 2 respectively. The pin 3 is connected to a ground plane on the board. In order to minimize parasitic inductance in the board traces, all path lengths connected to the pins of AZ5125-02S should be kept as short as possible.

In order to obtain enough suppression of ESD induced transient, good circuit board is critical.

Thus, the following guidelines are recommended:

- Minimize the path length between the protected lines and the AZ5125-02S.
- Place the AZ5125-02S near the input terminals or connectors to restrict transient coupling.
- The ESD current return path to ground should be kept as short as possible.
- Use ground planes whenever possible.
- NEVER route critical signals near board edges and near the lines which the ESD transient easily injects to.

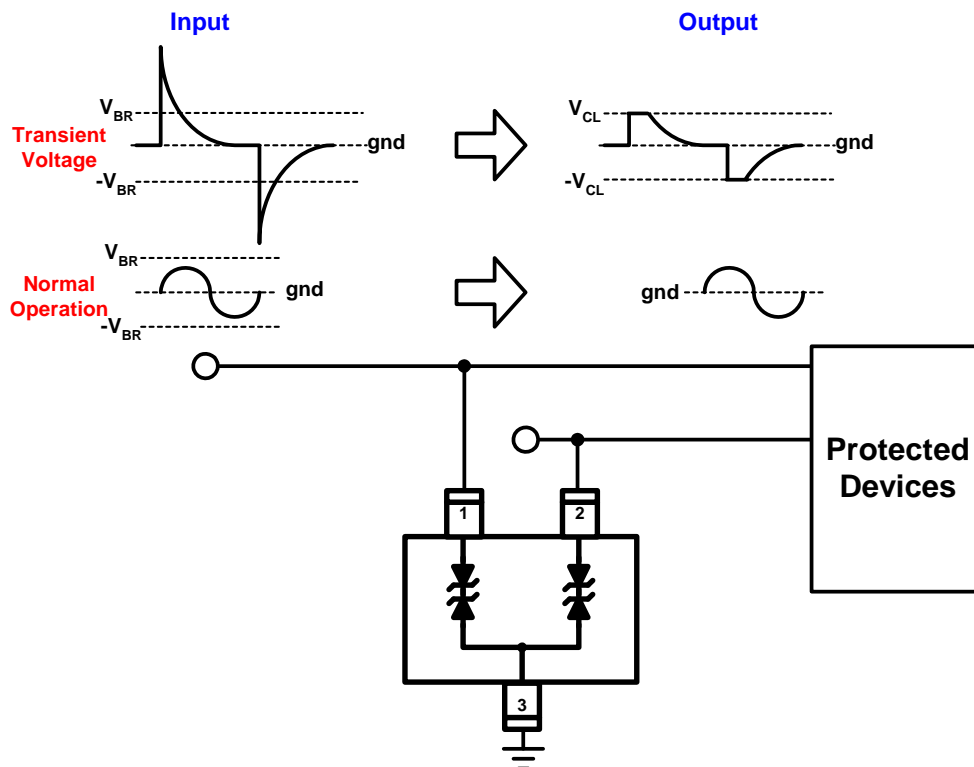
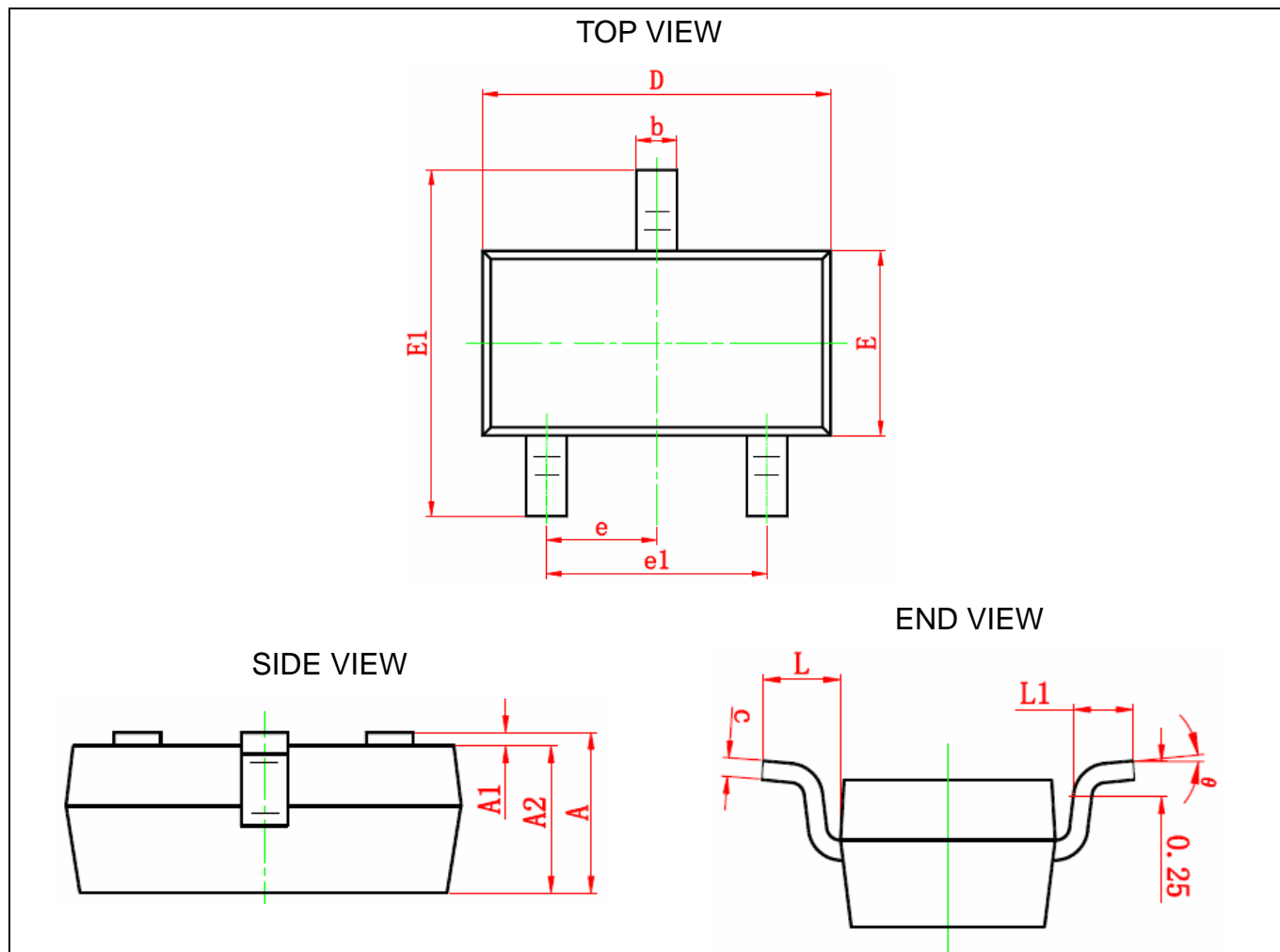


Fig. 1

Mechanical Details

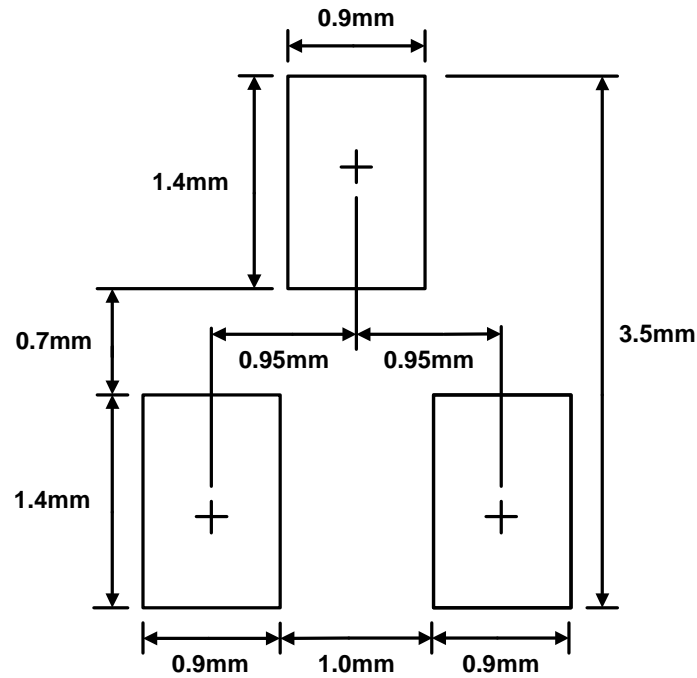
SOT23-3L PACKAGE DIAGRAMS



PACKAGE DIMENSIONS

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.900	1.150	0.035	0.045
A1	0.000	0.100	0.000	0.004
A2	0.900	1.050	0.035	0.041
b	0.300	0.500	0.012	0.020
c	0.080	0.150	0.003	0.006
D	2.800	3.000	0.110	0.118
E	1.200	1.400	0.047	0.055
E1	2.250	2.550	0.089	0.100
e	0.950 TYP		0.037 TYP	
e1	1.800	2.000	0.071	0.079
L	0.550 REF		0.022 REF	
L1	0.300	0.500	0.012	0.020
θ	0°	8°	0°	6°

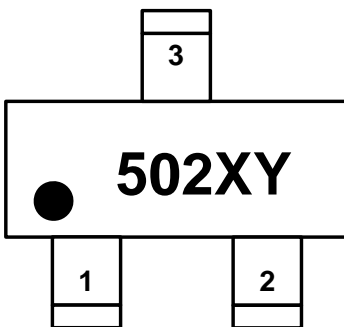
LAND LAYOUT



Notes:

This LAND LAYOUT is for reference purposes only. Please consult your manufacturing partners to ensure your company's PCB design guidelines are met.

MARKING CODE



502 = Device Code
X = Date Code
Y = Control Code

Part Number	Marking Code
AZ5125-02S	502XY

Revision History

Revision	Modification Description
Revision 2009/04/22	Preliminary Release.
Revision 2009/08/19	Formal Release.