



Features

- ESD Protect for 1 Line with Unidirectional.
- Provide ESD protection for each line to **IEC 61000-4-2 (ESD) $\pm 18\text{kV}$ (air/contact)**
IEC 61000-4-4 (EFT) 60A (5/50ns)
- Suitable for, **12V and below**, operating voltage applications
- Ultra Small package saves board space
- Protect one I/O line or one power line
- Fast turn-on and Low clamping voltage
- Solid-state silicon-avalanche and active circuit triggering technology
- **Green part**

Applications

- Battery Contacts
- Power Manager System
- PDA's
- Portable Devices
- Digital Cameras
- Digital Frames
- Cellular Handsets and Accessories
- Notebooks, desktops, and servers
- Microprocessor-based equipment
- Peripherals

Description

AZ4012-01L is a design which includes a unidirectional ESD rated clamping cell to protect one power line, or one control line, or one low speed data line in an electronic systems. The AZ4012-01L has been specifically designed to protect sensitive components which are connected to power and control lines from over-voltage damage and latch-up caused by Electrostatic

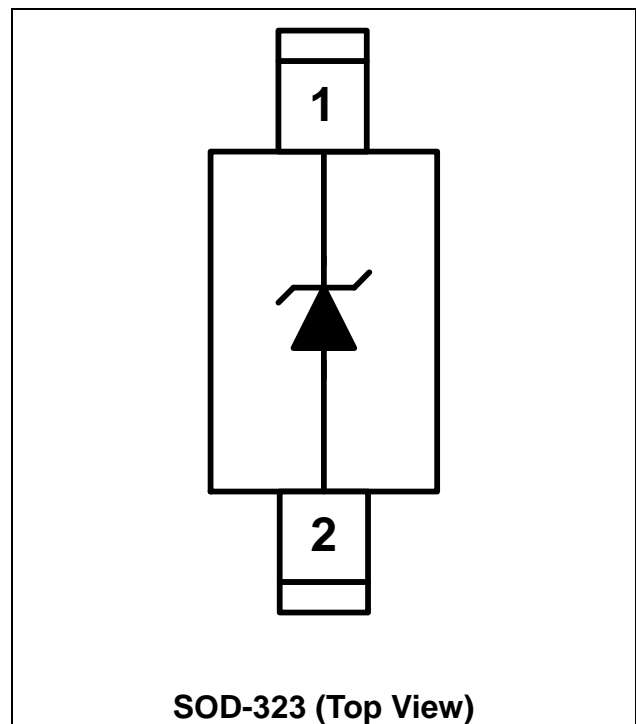
Discharging (ESD), Electrical Fast Transients (EFT), and Cable Discharge Event (CDE).

AZ4012-01L is a unique design which includes proprietary clamping cell in a single package.

During transient conditions, the proprietary clamping cell prevents over-voltage on the power line or control/data lines, protecting any downstream components.

AZ4012-01L may be used to meet the ESD immunity requirements of IEC61000-4-2, Level 4 ($\pm 15\text{kV}$ air, $\pm 8\text{kV}$ contact discharge).

Circuit Diagram / Pin Configuration





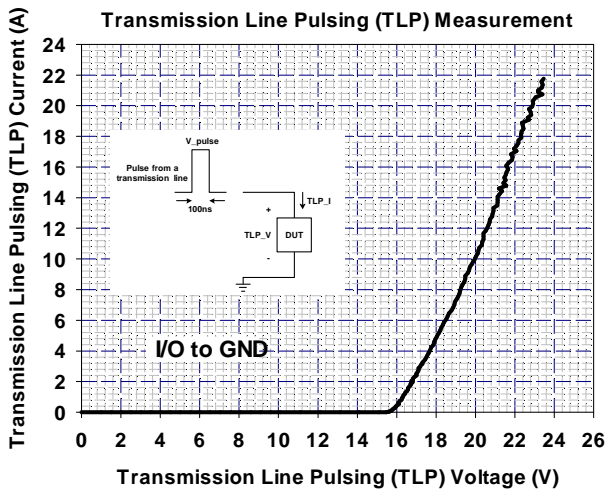
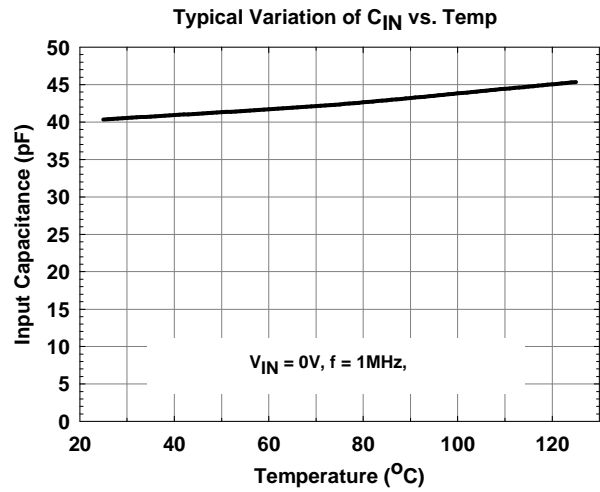
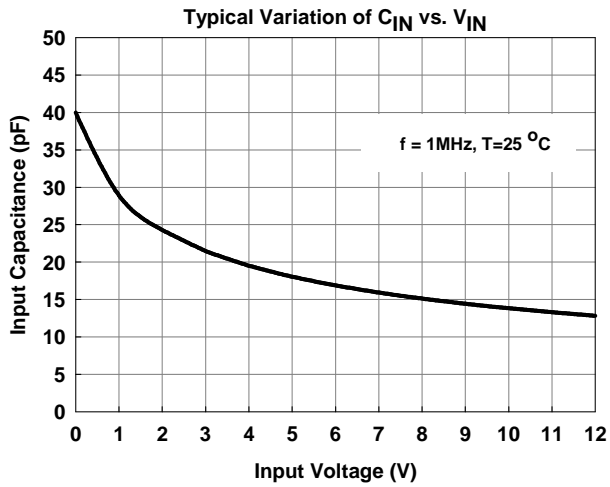
SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS			
PARAMETER	PARAMETER	RATING	UNITS
Operating Supply Voltage (pin-1 to pin-2)	V_{DC}	13	V
pin-1 to pin-2 ESD per IEC 61000-4-2 (Air) (Contact)	V_{ESD}	± 18	kV
Lead Soldering Temperature	T_{SOL}	260 (10 sec.)	$^{\circ}C$
Operating Temperature	T_{OP}	-55 to +125	$^{\circ}C$
Storage Temperature	T_{STO}	-55 to +150	$^{\circ}C$

ELECTRICAL CHARACTERISTICS						
PARAMETER	SYMBOL	CONDITIONS	MINI	TYP	MAX	UNITS
Reverse Stand-Off Voltage	V_{RWM}	pin-1 to pin-2, $T=25^{\circ}C$.			12	V
Reverse Leakage Current	I_{Leak}	$V_{RWM} = 12V$, $T=25^{\circ}C$, pin-1 to pin-2.			1	μA
Reverse Breakdown Voltage	V_{BV}	$I_{BV} = 1mA$, $T=25^{\circ}C$, pin-1 to pin-2	13.5		18	V
Forward Voltage	V_F	$I_F = 15mA$, $T=25^{\circ}C$, pin-2 to pin-1	0.6	0.8	1	V
ESD Clamping Voltage	V_{clamp}	IEC 61000-4-2 +6kV, $T=25^{\circ}C$, Contact mode, pin-1 to pin-2.		22		V
ESD Dynamic Turn-on Resistance	$R_{dynamic}$	IEC 61000-4-2 0~+6kV, $T=25^{\circ}C$, Contact mode, pin-1 to pin-2.		0.34		Ω
Channel Input Capacitance	C_{IN}	$V_R = 0V$, $f = 1MHz$, $T=25^{\circ}C$, pin-1 to pin-2.		40	50	pF



Typical Characteristics



Applications Information

ESD Protection for Battery Contact

The AZ4012-01L can be used to protect the Battery Contact. The ESD protection scheme for typical Li-ion battery pack is shown in Fig. 1. In the Fig. 1, the pin 2 of AZ4012-01L should be connected directly to a ground plane (Pack- terminal) on the board. The pin1 of AZ4012-01L connected to the terminal of Pack+.

All the path lengths connected to the pins of AZ4012-01L should be kept as short as possible to minimize parasitic inductance in the board traces.

In order to obtain enough suppression of ESD induced transient, good circuit board is critical. Thus, the following guidelines are recommended:

- Minimize the path length between the protected lines and the AZ4012-01L.
- Place the AZ4012-01L near the input terminals or connectors to restrict transient coupling.
- The ESD current return path to ground should be kept as short as possible.
- Use ground planes whenever possible.
- NEVER route critical signals near board edges and near the lines which the ESD transient easily injects to PCB internal circuit.

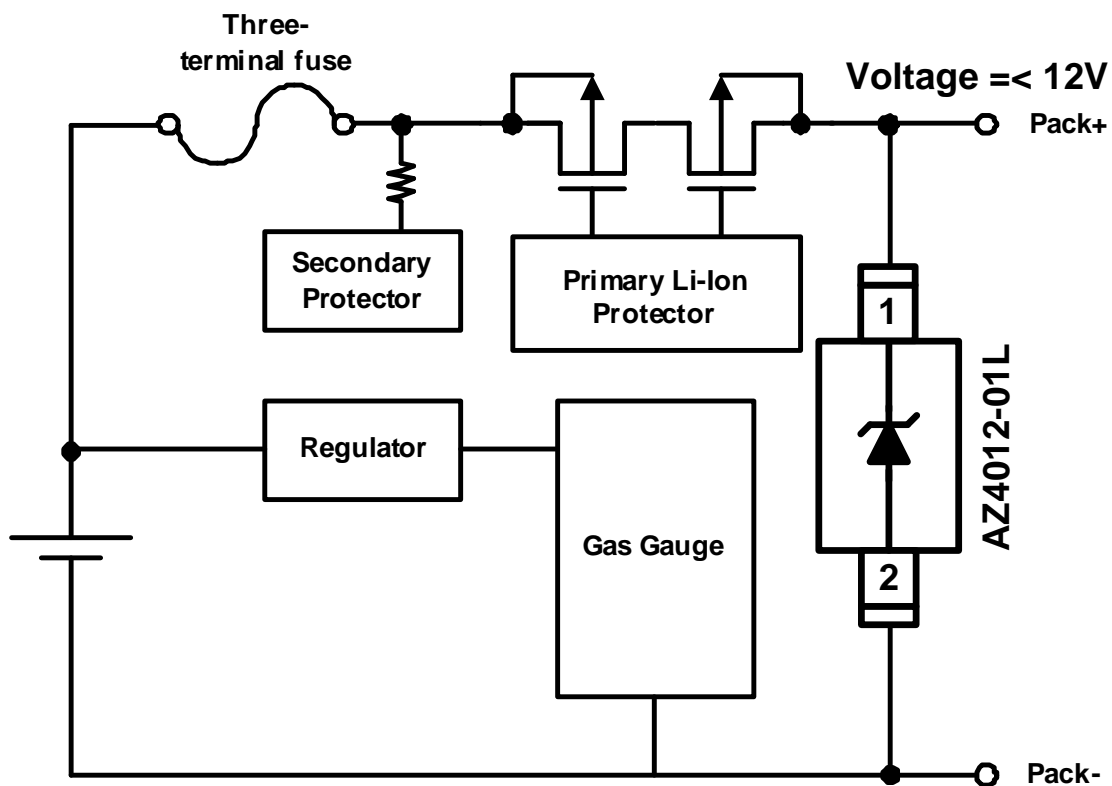


Fig. 1 ESD protection scheme for a typical Li-ion battery pack by using AZ4012-01L.



ESD Protection for Low-Speed Data Line

low speed data lines, and power lines of PCB internal circuits from ESD transient stress.

Fig. 2 shows another simplified example of using AZ4012-01L to protect the control lines,

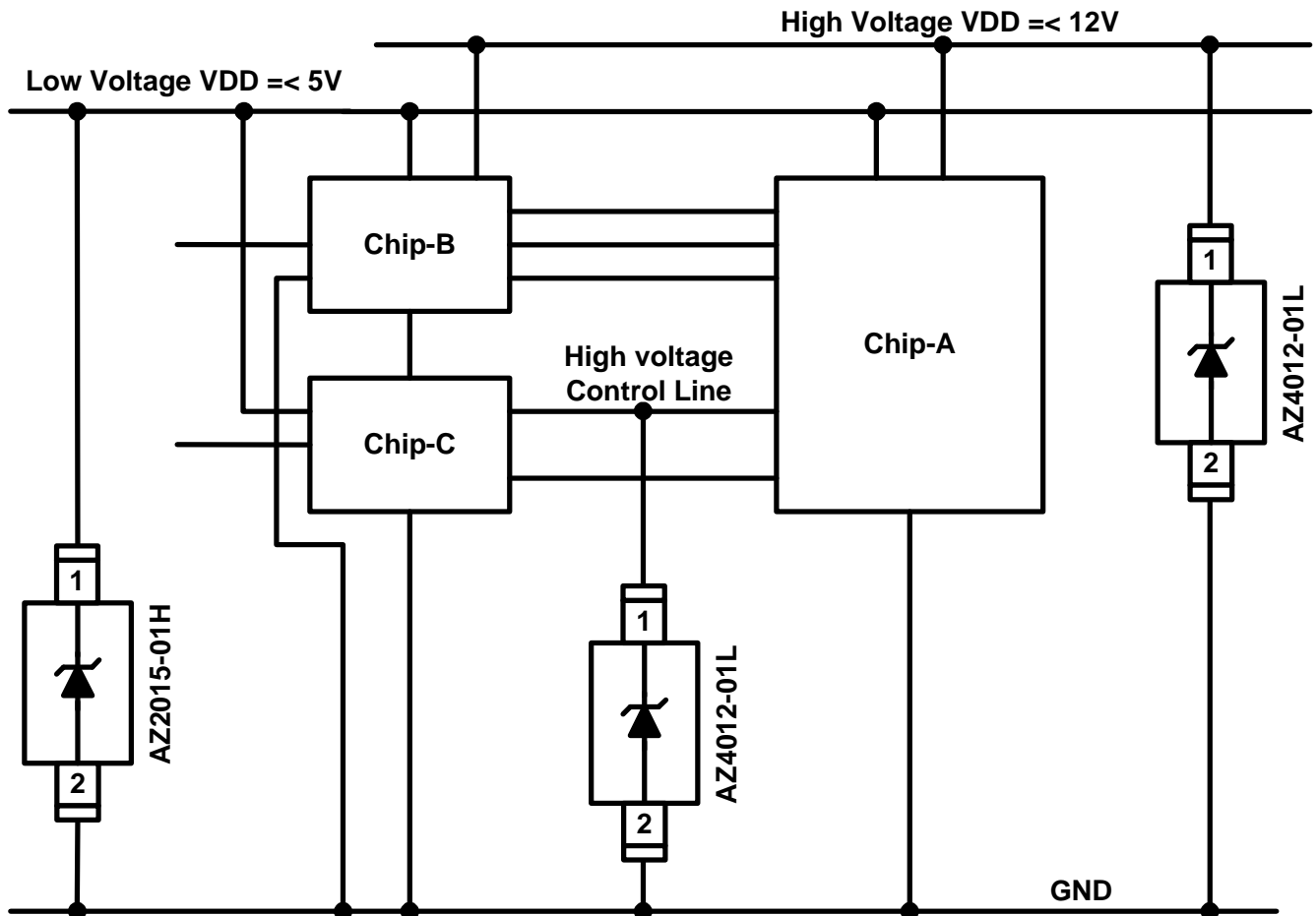


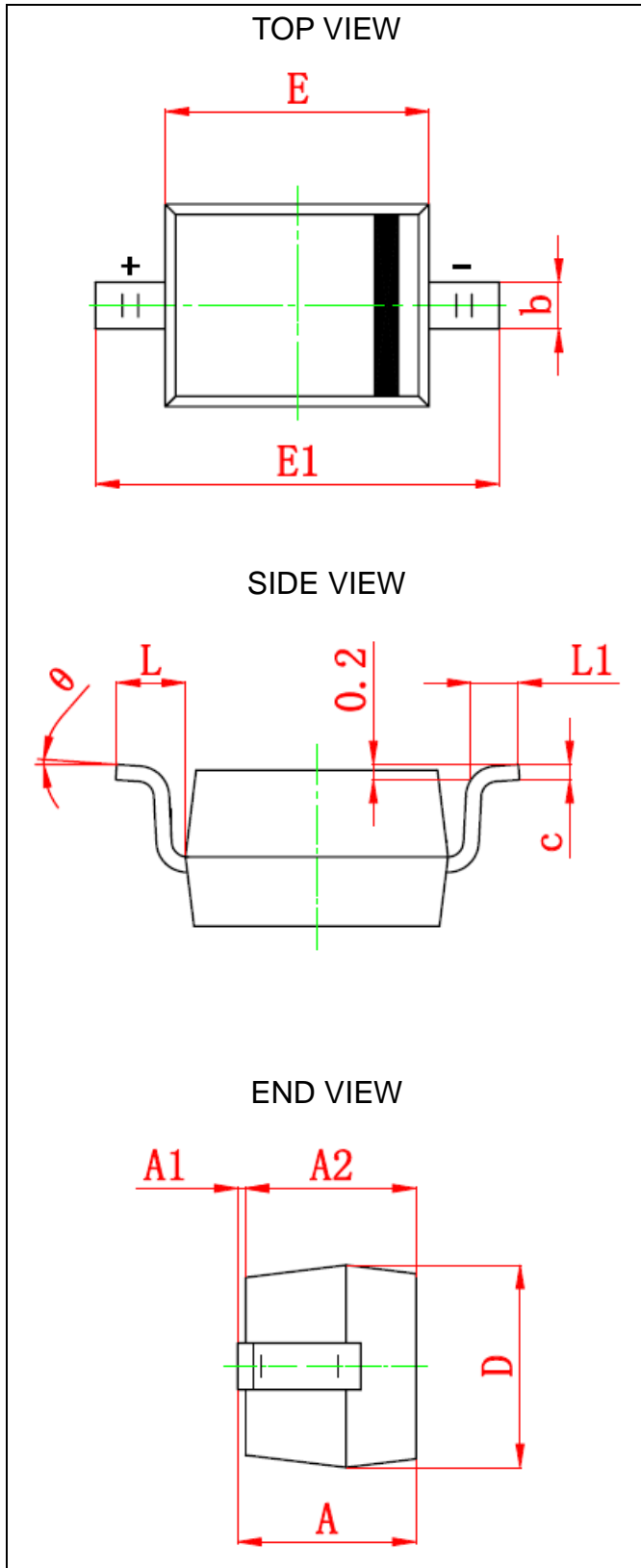
Fig. 2 ESD protection scheme for internal PCB circuits by using AZ4012-01L.



Mechanical Details

SOD-323

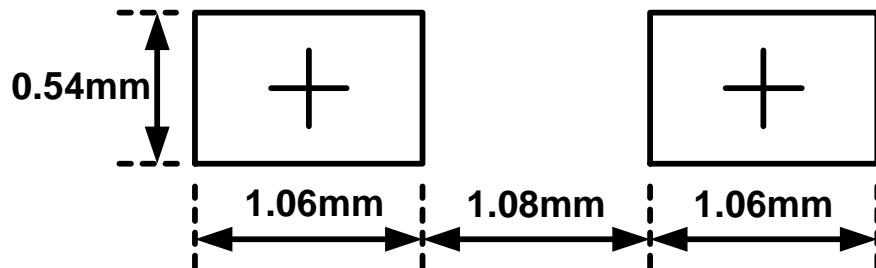
PACKAGE DIAGRAMS



PACKAGE DIMENSIONS

Symbol	Millimeters		Inches	
	MIN.	MAX.	MIN.	MAX.
A	0.8	1.0	0.031	0.039
A1	0	0.1	0.000	0.004
A2	0.8	0.9	0.031	0.035
b	0.25	0.35	0.010	0.014
C	0.08	0.15	0.003	0.006
D	1.2	1.4	0.047	0.055
E	1.6	1.8	0.063	0.071
E1	2.5	2.7	0.098	0.106
L	0.475REF		0.019 REF	
L1	0.25	0.4	0.010	0.016
θ	0°	8°	0°	8°

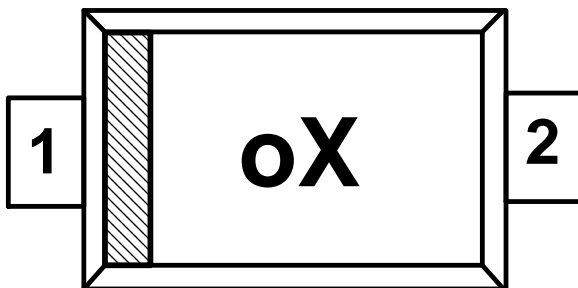
LAND LAYOUT



Notes:

This LAND LAYOUT is for reference purposes only. Please consult your manufacturing partners to ensure your company's PCB design guidelines are met.

MARKING CODE



o = Device Code
 X = Date Code

Part Number	Marking Code
AZ4012-01L	oX

Ordering Information

PN#	Material	Type	Reel size	MOQ/internal box	MOQ/carton
AZ4012-01L.R7G	Green	T/R	7 inch	4 reel=12,000/box	6 box=72,000/carton



Revision History

Revision	Modification Description
Revision 2011/11/10	Formal Release.