Features

- ESD Protect for 2 Lines with Unidirectional
- ESD Protect for 1 Line with Bidirectional
- Provide ESD protection for each line to
  IEC 61000-4-2 (ESD) ±30kV (air), ±22kV (contact)
  IEC 61000-4-4 (EFT) 80A (5/50ns)
  IEC 61000-4-5 (Lightning) 16A(8/20μs)
- For low operating voltage applications: 5V, 4.2V, 3.3V, 2.5V
- Fast turn-on and Low clamping voltage
- Array of surge rated equivalent TVS diodes
- Small package saves board space
- Solid-state silicon-avalanche and active circuit triggering technology

Applications

- Notebooks, Desktops, Servers
- Hand Held Portable Applications
- Serial and Parallel Ports
- Power Lines and Low Speed Data Lines of Electronic Systems.

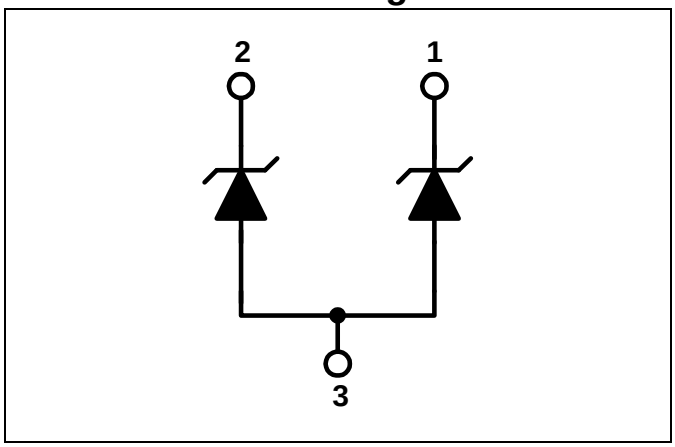
Description

AZ2015-02S is a design which includes surge rated clamping cell arrays to protect the power lines or control lines in an electronic systems. The AZ2015-02S has been specifically designed to protect sensitive components which are connected to power and control lines from over-voltage caused by Electrostatic Discharging (ESD), Electrical Fast Transients (EFT), and Lightning.

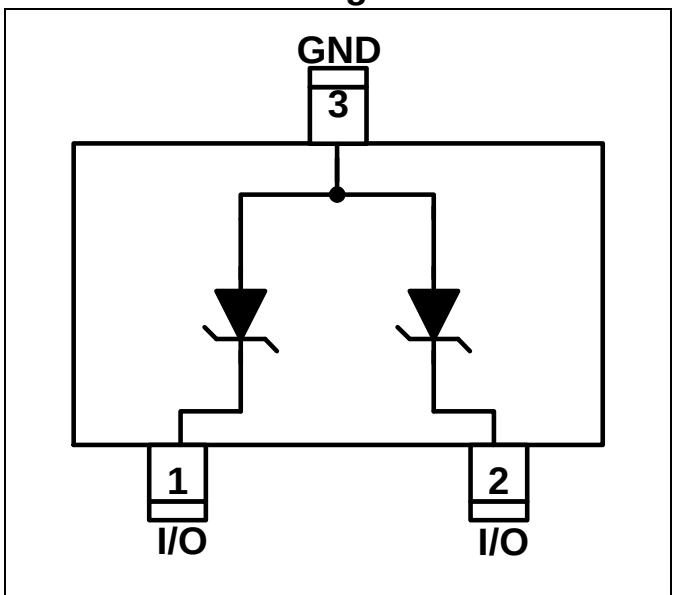
AZ2015-02S is a unique design which includes proprietary clamping cells in a single package. During transient conditions, the proprietary clamping cells prevent over-voltage on the power lines or control lines, protecting any downstream components.

AZ2015-02S may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 (±15kV air, ±8kV contact discharge).

Circuit Diagram



Pin Configuration



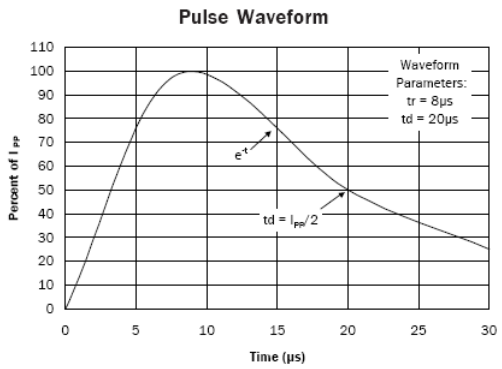
JEDEC SOT23-3L (Top View)

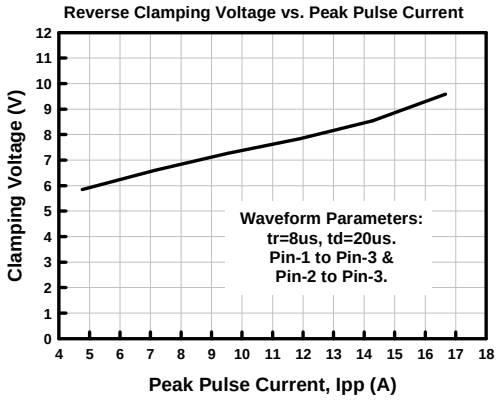
SPECIFICATIONS

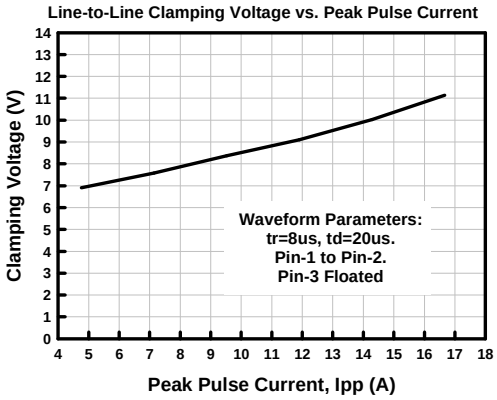
ABSOLUTE MAXIMUM RATINGS			
PARAMETER	**PARAMETER**	**RATING**	**UNITS**
Peak Pulse Current (tp =8/20us)	I_{PP}	16	A
Operating Supply Voltage (pin-1,-2 to pin-3)	V_{DC}	6	V
pin-1,-2 to pin-3 ESD per IEC 61000-4-2 (Air) pin-1,-2 to pin-3 ESD per IEC 61000-4-2 (Contact)	V_{ESD-1}	30 22	kV
pin-1 to pin-2 ESD per IEC 61000-4-2 (Air) pin-1 to pin-2 ESD per IEC 61000-4-2 (Contact)	V_{ESD-2}	30 20	kV
Lead Soldering Temperature	T_{SOL}	260 (10 sec.)	^{o}C
Operating Temperature	T_{OP}	-55 to +125	^{o}C
Storage Temperature	T_{STO}	-55 to +150	^{o}C

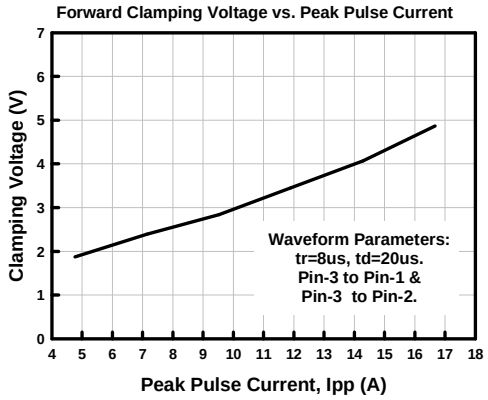
ELECTRICAL CHARACTERISTICS						
PARAMETER	**SYMBOL**	**CONDITIONS**	**MINI**	**TYP**	**MAX**	**UNITS**
Reverse Stand-Off Voltage	V_{RWM}	pin-1-to-pin-3, or pin-2-to-pin-3, T=25 ^{o}C.			5	V
Reverse Leakage Current	I_{Leak}	V_{RWM} = 5V, T=25 ^{o}C, pin-1-to-pin-3, or pin-2-to-pin-3.			2.5	µA
Reverse Breakdown Voltage	V_{BV}	I_{BV} = 1mA, T=25 ^{o}C, pin-1-to-pin-3, or pin-2-to-pin-3.	6.1		9	V
Forward Voltage	V_F	I_F = 15mA, T=25 ^{o}C	0.6	0.8	1	V
Surge Clamping Voltage 1	$V_{CL-surge-1}$	I_{PP}=5A, tp=8/20us, T=25 ^{o}C, pin-1-to-pin-3, or pin-2-to-pin-3.		6	7	V
Surge Clamping Voltage 2	$V_{CL-surge-2}$	I_{PP}=5A, tp=8/20us, T=25 ^{o}C, between pin-1 and pin-2, while pin-3 is floated.		7	8	V
			-8	-7		
ESD Clamping Voltage-1	$V_{clamp-1}$	I=17A pulse, T=25 ^{o}C, Contact mode, pin-1,-2, to pin-3.		9		V
ESD Clamping Voltage-2	$V_{clamp-2}$	I=17A pulse, T=25 ^{o}C, Contact mode, pin-1-to-pin-2, while pin-3 is floated.		11		V
ESD Dynamic Turn-on Resistance-1	$R_{dynamic-1}$	IEC 61000-4-2 0~+6kV, T=25 ^{o}C, Contact mode, pin-1,-2, to pin-3.		0.2		Ω
ESD Dynamic Turn-on Resistance-2	$R_{dynamic-2}$	IEC 61000-4-2 0~+6kV, T=25 ^{o}C, Contact mode, pin-1-to-pin-2, while pin-3 is floated.		0.28		Ω
Channel Input Capacitance	C_{IN}	V_R= 0V, f = 1MHz, T=25 ^{o}C, pin-1-to-pin-3, or pin-2-to-pin-3.		55	65	pF
Channel to Channel Input Capacitance	C_{CROSS}	V_R= 0V, f = 1MHz, pin-3 floated, T=25 ^{o}C , between pin-1 and pin-2.		27.5	32.5	pF

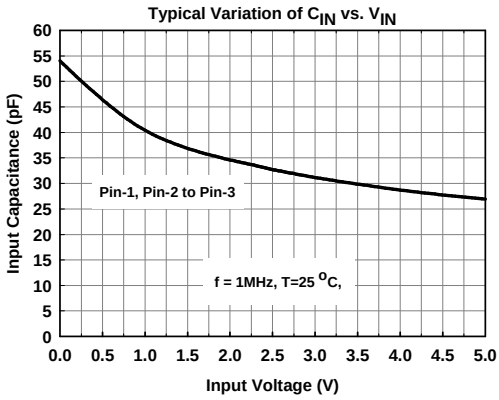
Typical Characteristics

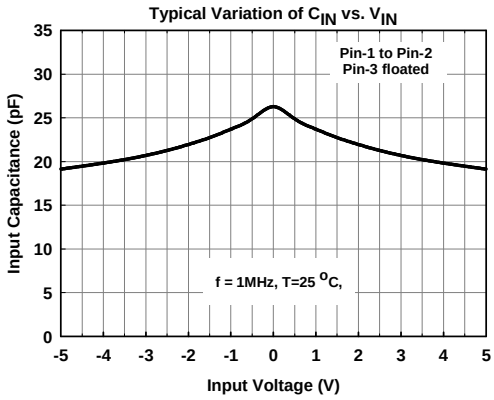


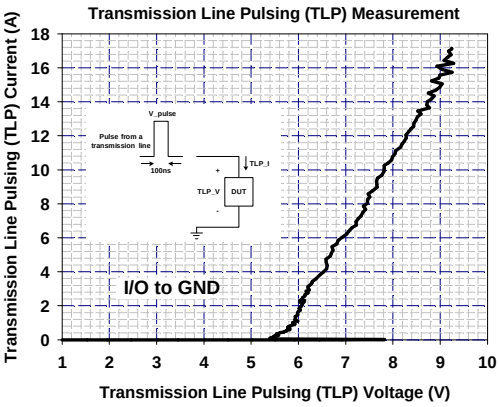


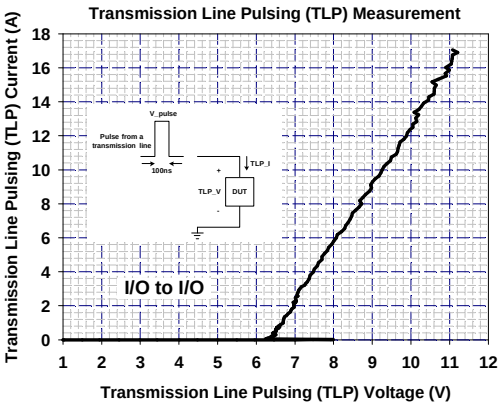












Applications Information

The AZ2015-02S is designed to protect two lines against System ESD/EFT/Lightning pulses by clamping them to an acceptable reference.

The usage of the AZ2015-02S is shown in Fig. 1. Protected lines, such as data lines, control lines, or power lines, are connected at pin 1 and 2. The pin 3 should be connected directly to a ground plane on the board. All path lengths connected to the pins of AZ2015-02S should be kept as short as possible to minimize parasitic inductance in the board traces.

In order to obtain enough suppression of ESD induced transient, good circuit board is critical. Thus, the following guidelines are recommended:

- Minimize the path length between the protected lines and the AZ2015-02S.
- Place the AZ2015-02S near the input terminals or connectors to restrict transient coupling.
- The ESD current return path to ground should be kept as short as possible.
- Use ground planes whenever possible.
- NEVER route critical signals near board edges and near the lines which the ESD transient easily injects to.

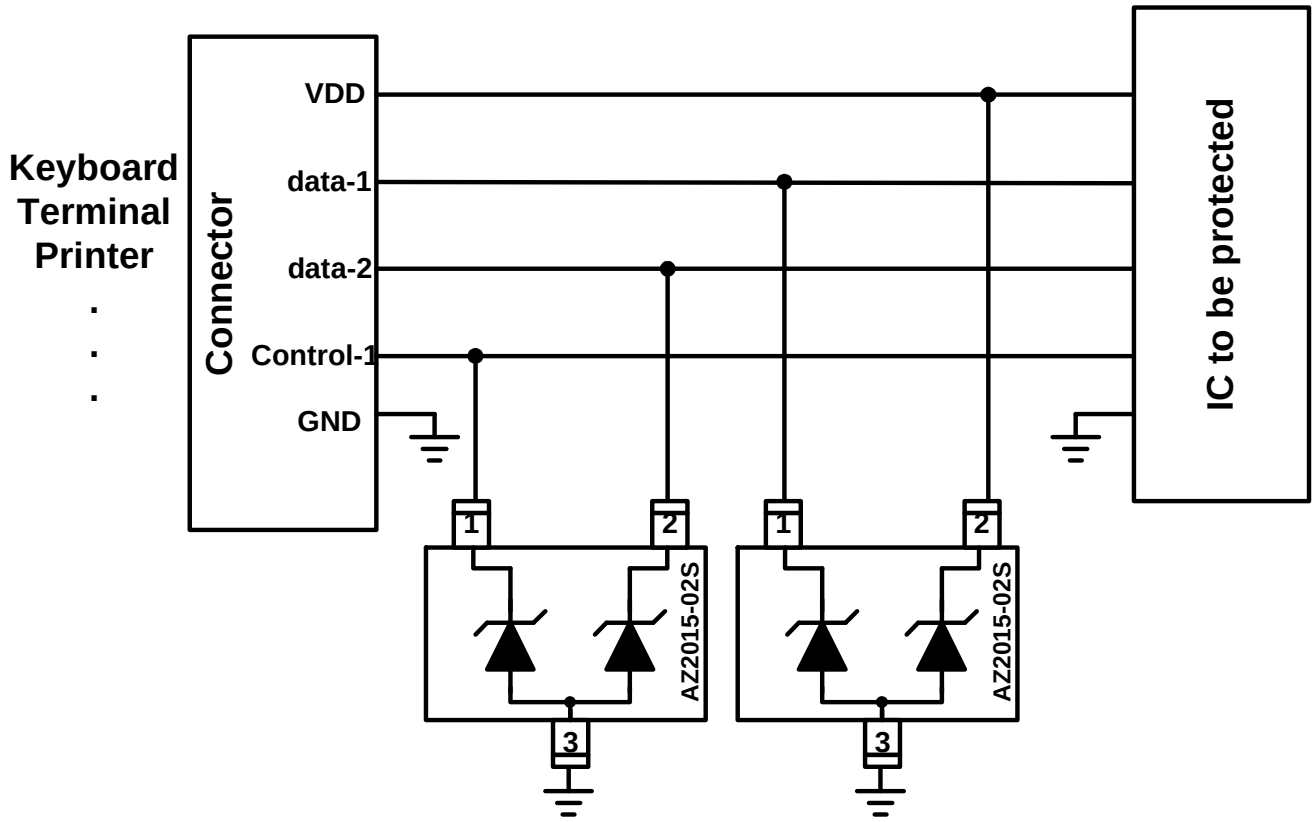


Fig. 1

Fig. 2 shows another simplified example of using AZ2015-02S to protect the control lines, low speed data lines, and power lines from ESD transient stress.

Fig. 3 shows the simplified example of using AZ2015-02S to provide a bidirectional protection on a data line from ESD transient stress.

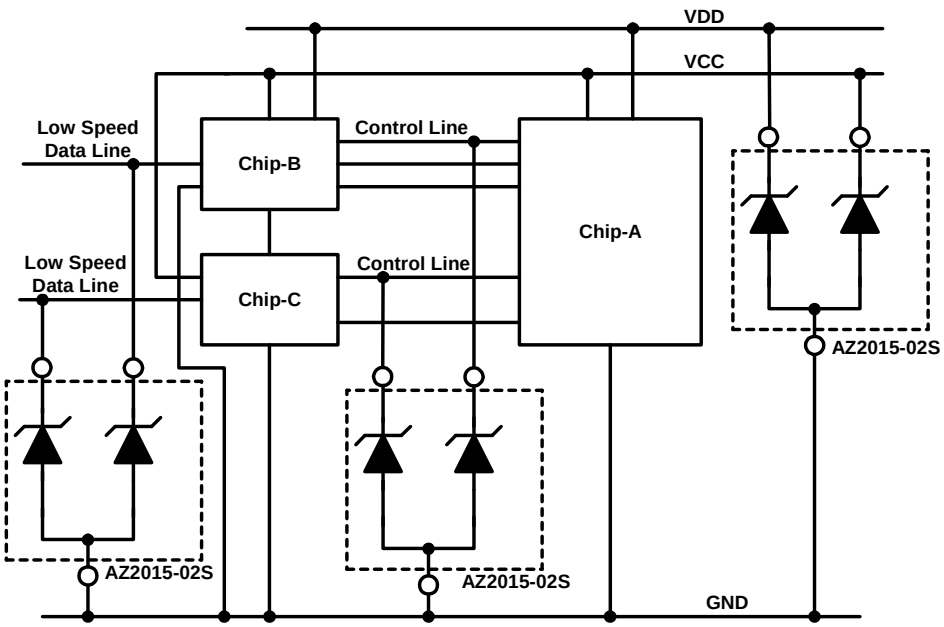


Fig. 2

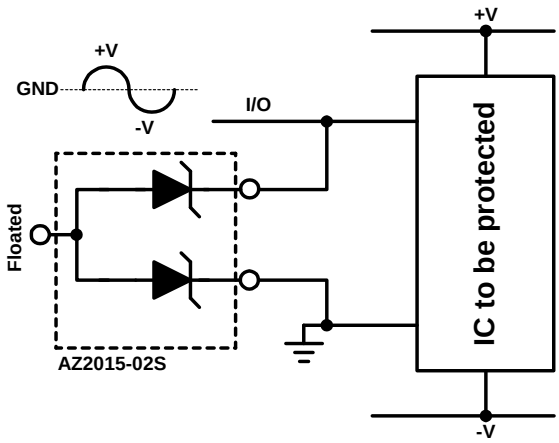
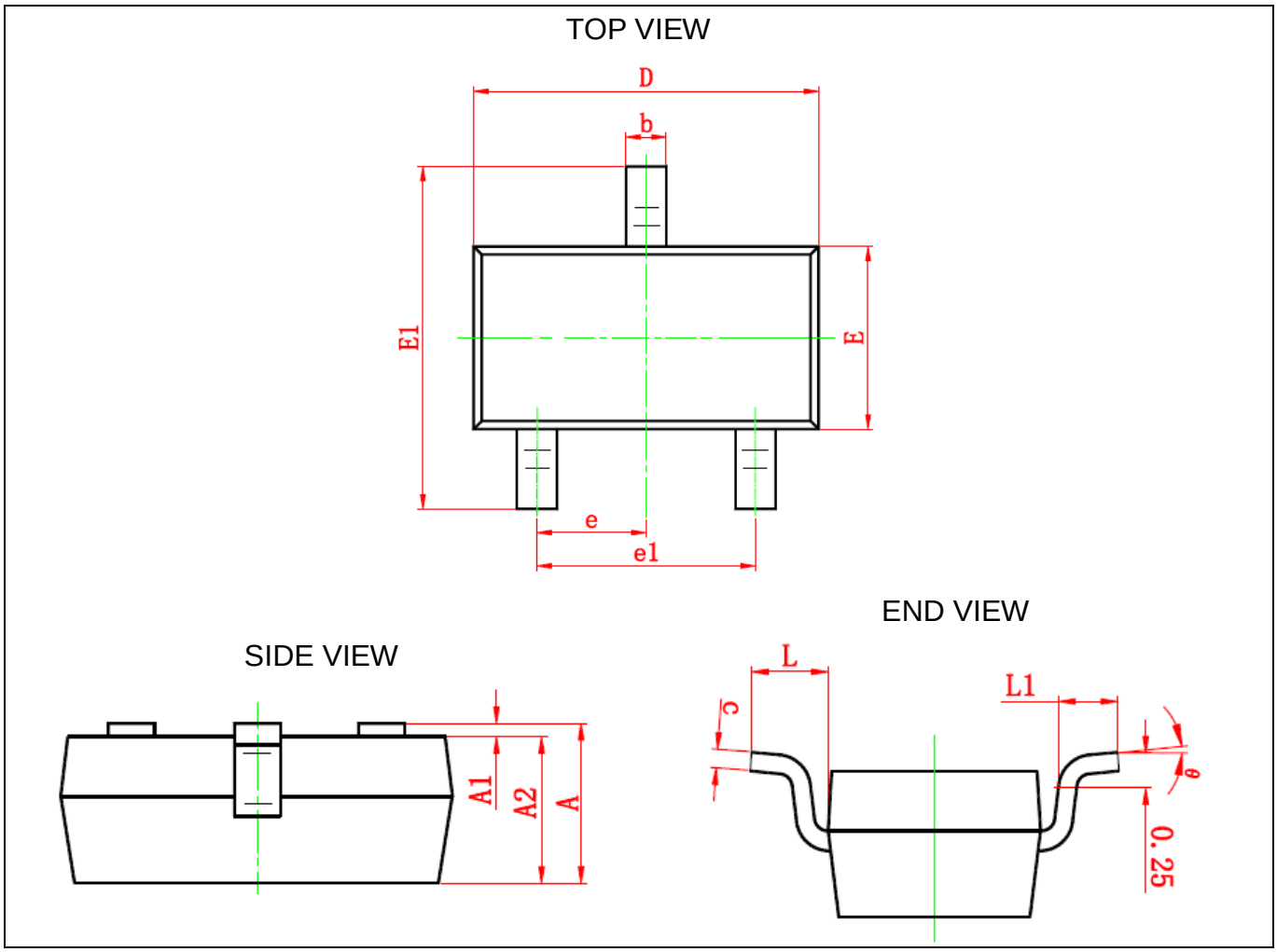


Fig. 3 Bidirectional Protection

Mechanical Details

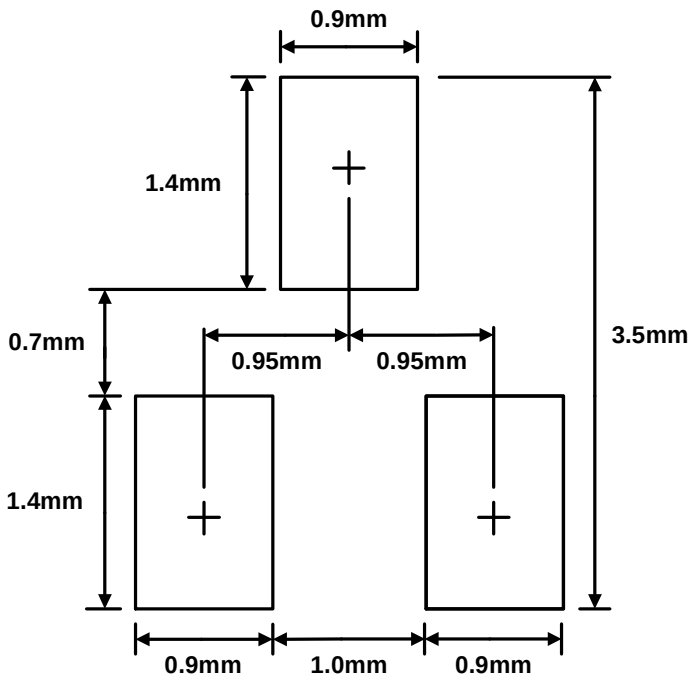
SOT23-3L PACKAGE DIAGRAMS



PACKAGE DIMENSIONS

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.900	1.150	0.035	0.045
A1	0.000	0.100	0.000	0.004
A2	0.900	1.050	0.035	0.041
b	0.300	0.500	0.012	0.020
c	0.080	0.150	0.003	0.006
D	2.800	3.000	0.110	0.118
E	1.200	1.400	0.047	0.055
E1	2.250	2.550	0.089	0.100
e	0.950 TYP		0.037 TYP	
e1	1.800	2.000	0.071	0.079
L	0.550 REF		0.022 REF	
L1	0.300	0.500	0.012	0.020
θ	0°	8°	0°	6°

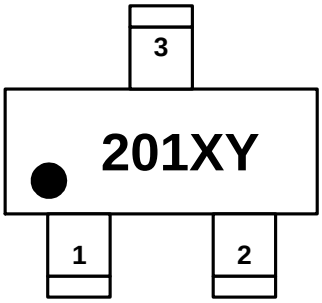
LAND LAYOUT



Notes:

This LAND LAYOUT is for reference purposes only. Please consult your manufacturing partners to ensure your company's PCB design guidelines are met.

MARKING CODE



201 = Device Code
X = Date Code
Y = Control Code

Part Number	Marking Code
AZ2015-02S (Rohs part)	201XY
AZ2015-02S (Green part)	**227XY**

Ordering Information

PN#	Material	Type	Reel size	MOQ/interal box	MOQ/carton
AZ2015-02S.R7G	Green	T/R	7 inch	4 reel=12,000/box	6 box=72,000/carton

Revision History

Revision	Modification Description
Revision 2006/8/28	Original Release.
Revision 2006/10/25	1. Increase ESD spec. from (Air-15KV, Contact-8kV) to (Air-22KV, Contact-16kV). 2. Increase EFT spec. from 40A to 60A. 3. Adjust Lightning spec. from 15A to 13A. 4. Modify the ABSOLUTE MAXIMUM RATINGS of ESD and Lightning. 5. Enhance the ELECTRICAL CHARACTERISTICS on page 2. 6. Update the curves on page 3.
Revision 2007/02/07	1. Change the clamping cell symbol for easy understanding. 2. Add the TLP characterization. 3. Add the ESD holding voltage characterization under IEC61000-4-2 6kV contact mode. 4. Change the Characterization Temp of V_{RWM}, V_{Leak}, and V_{BV} from 125°C to 25°C. 5. Modify the ABSOLUTE MAXIMUM RATINGS of ESD.
Revision 2007/05/15	Update the Marking Code from 201X to 201XY
Revision 2007/08/01	Remove the Ordering Information
Revision 2008/04/03	1. Update the Mechanical Details. 2. Increase ESD spec to (Air-30KV Contact-22KV), EFT spec from 60A to 80A, and Lightning spec from 13A to 16A. 3. Rename the 8/20us clamping voltage V_{CL_1} and V_{CL_2} as Surge Clamping Voltage $V_{CL\_surge\_1}$ and $V_{CL\_surge\_2}$, and update their values from (7V, 8V) to (6V, 7V), respectively. 4. Rename the ESD holding voltage V_{hold} as ESD Clamping Voltage $V_{Clamp-1}$, $V_{Clamp-2}$, and update the values to be 8V and 10V, respectively. 5. Add the parameters of ESD Dynamic Turn-on Resistance, $R_{dynamic-1}$ and $R_{dynamic-2}$. 6. Update the values of C_{IN} and C_{CROSS} from (90pF, 45pF) to (55pF, 27.5pF).
Revision 2008/05/23	1. Redefine the ESD Clamping Voltage $V_{Clamp-1}$, $V_{Clamp-2}$, to be under TLP 17A pulse instead of under IEC61000-4-2 6kV. And update their values from (8V, 10V) to be (9V, 11V). 2. Update the ESD Dynamic Turn-on Resistance, $R_{dynamic-1}$ and $R_{dynamic-2}$ from (0.16Ω, 0.21Ω) to be (0.2Ω, 0.28Ω). 3. Update the TLP I-V curves. 4. This version is valid from the date code of “201hJ”.
Revision 2008/10/14	Add marking code for the Green part.
Revision 2011/06/18	1. Update the Company Logo. 2. Add the Ordering Information.