Features

- ESD Protect for 2 Lines with Unidirectional
- Provide ESD protection for a line to
  IEC 61000-4-2 (ESD) ±15kV (air/contact)
  IEC 61000-4-4 (EFT) 60A (5/50ns)
  IEC 61000-4-5 (Lightning) 5.5A (8/20μs)
- Suitable for, **24V and below,** operating voltage applications
- Fast turn-on and Low clamping voltage
- Array of ESD rated equivalent TVS diodes
- Small package saves board space
- Solid-state silicon-avalanche and active circuit triggering technology
- ***Green part***

Applications

- Battery Contacts
- HBT Power Amp Protection
- GaAs Photodetector Protection
- Power Manager System
- Cellular handsets AND accessories
- Set-Top Box
- Notebooks, desktops, and servers
- Portable instrumentation

Description

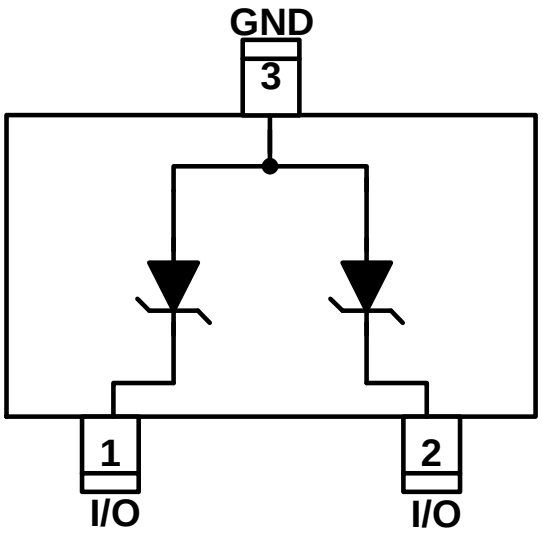
AZ4024-02S is a design which includes ESD /surge rated clamping cell arrays to protect the power lines or control lines in an electronic system. The AZ4024-02S has been specifically designed to protect sensitive components which are connected to power and control lines from over-voltage caused by Electrostatic Discharging (ESD), Electrical Fast Transients (EFT), Lightning, and Cable Discharge Event (CDE).

AZ4024-02S is a unique design which includes proprietary clamping cells in a single package.

During transient conditions, the proprietary clamping cells prevent over-voltage on the power lines or control lines, protecting any downstream components.

AZ4024-02S may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 (±15kV air, ±8kV contact discharge).

Circuit Diagram / Pin Configuration



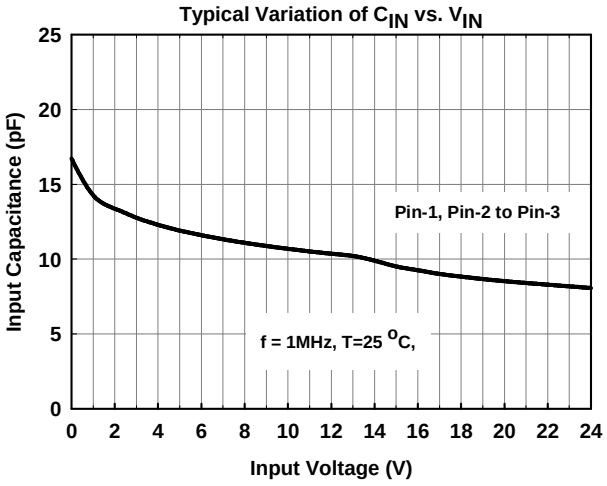
JEDEC SOT23-3L (Top View)

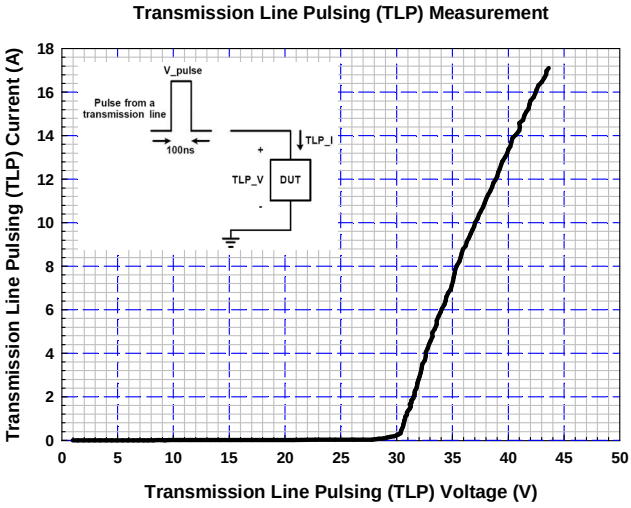
SPECIFICATIONS

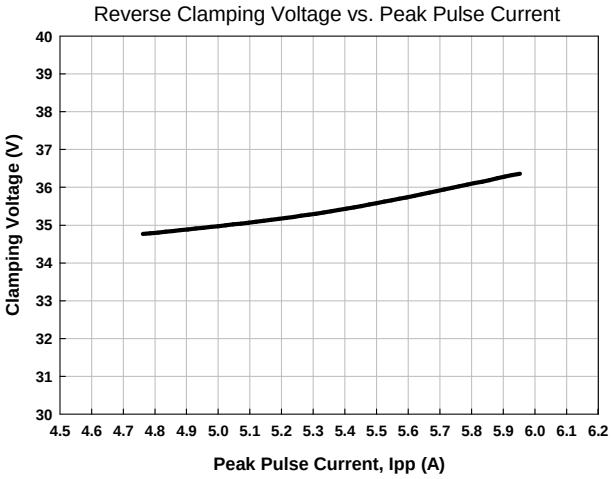
ABSOLUTE MAXIMUM RATINGS			
PARAMETER	**PARAMETER**	**RATING**	**UNITS**
Peak Pulse Current (tp = 8/20 us)	I_{PP}	5.5	A
Operating Supply Voltage (pin-1, -2 to pin-3)	V_{DC}	24	V
pin-1,-2 to pin-3 ESD per IEC 61000-4-2 (Air/Contact)	V_{ESD}	±15	kV
Lead Soldering Temperature	T_{SOL}	260 (10 sec.)	^{o}C
Operating Temperature	T_{OP}	-55 to +125	^{o}C
Storage Temperature	T_{STO}	-55 to +150	^{o}C

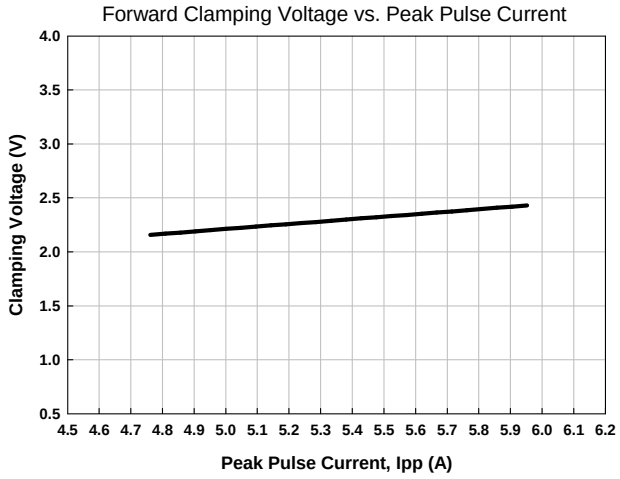
ELECTRICAL CHARACTERISTICS						
PARAMETER	**SYMBOL**	**CONDITIONS**	**MINI**	**TYP**	**MAX**	**UNITS**
Reverse Stand-Off Voltage	V_{RWM}	pin-1-to-pin-3, or pin-2-to-pin-3, T=25 ^{o}C			24	V
Reverse Leakage Current	I_{Leak}	V_{RWM} = 24V, T=25 ^{o}C, pin-1-to-pin-3, or pin-2-to-pin-3			1	μA
Reverse Breakdown Voltage	V_{BV}	I_{BV} = 1mA, T=25 ^{o}C, pin-1-to-pin-3, or pin-2-to-pin-3	26.7			V
Forward Voltage	V_F	I_F = 15mA, T=25 ^{o}C, pin-3 to pin-1 or pin-3 to pin-2	0.6	0.8	1	V
ESD Clamping Voltage	V_{ESD_clamp}	IEC 61000-4-2 +6kV, T=25 ^{o}C, Contact mode, pin-1 (or pin-2) to pin-3		43.5		V
ESD Dynamic Turn-on Resistance	$R_{dynamic}$	IEC 61000-4-2 0~+6kV, T=25 ^{o}C, Contact mode, pin-1 (or pin-2) to pin-3		0.85		**Ω**
Surge Clamping Voltage	V_{surge_clamp}	Ipp = 5A, tp = 8/20us, T = 25 ^{o}C, pin-1 (or pin-2) to pin3		35	40	V
Channel Input Capacitance	C_{IN}	V_R = 0V, f = 1MHz, T=25 ^{o}C, pin-1-to-pin-3, or pin-2-to-pin-3		20	25	pF

Typical Characteristics









Applications Information

The AZ4024-02S is designed to protect two lines against System ESD/EFT/CDE pulses by clamping them to an acceptable reference.

The usage of the AZ4024-02S is shown in Fig. 1. Protected lines, such as data lines, control lines, or power lines, are connected at pin 1 and 2. The pin 3 should be connected directly to a ground plane on the board. All path lengths connected to the pins of AZ4024-02S should be kept as short as possible to minimize parasitic inductance in the board traces.

In order to obtain enough suppression of ESD induced transient, good circuit board is critical. Thus, the following guidelines are recommended:

- Minimize the path length between the protected lines and the AZ4024-02S.
- Place the AZ4024-02S near the input terminals or connectors to restrict transient coupling.
- The ESD current return path to ground should be kept as short as possible.
- Use ground planes whenever possible.
- NEVER route critical signals near board edges and near the lines which the ESD transient easily injects to.

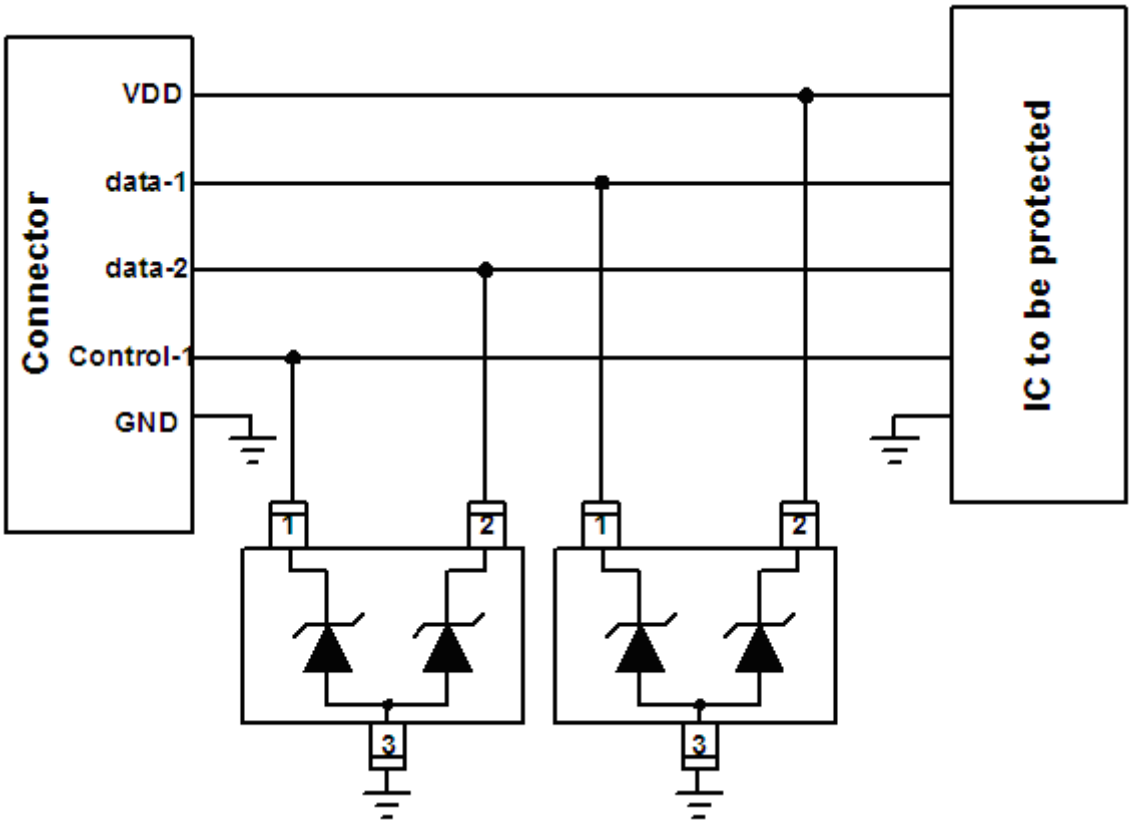


Fig. 1

Fig. 2 shows another simplified example of using AZ4024-02S to protect the control lines, low speed data lines, and power lines from ESD transient stress.

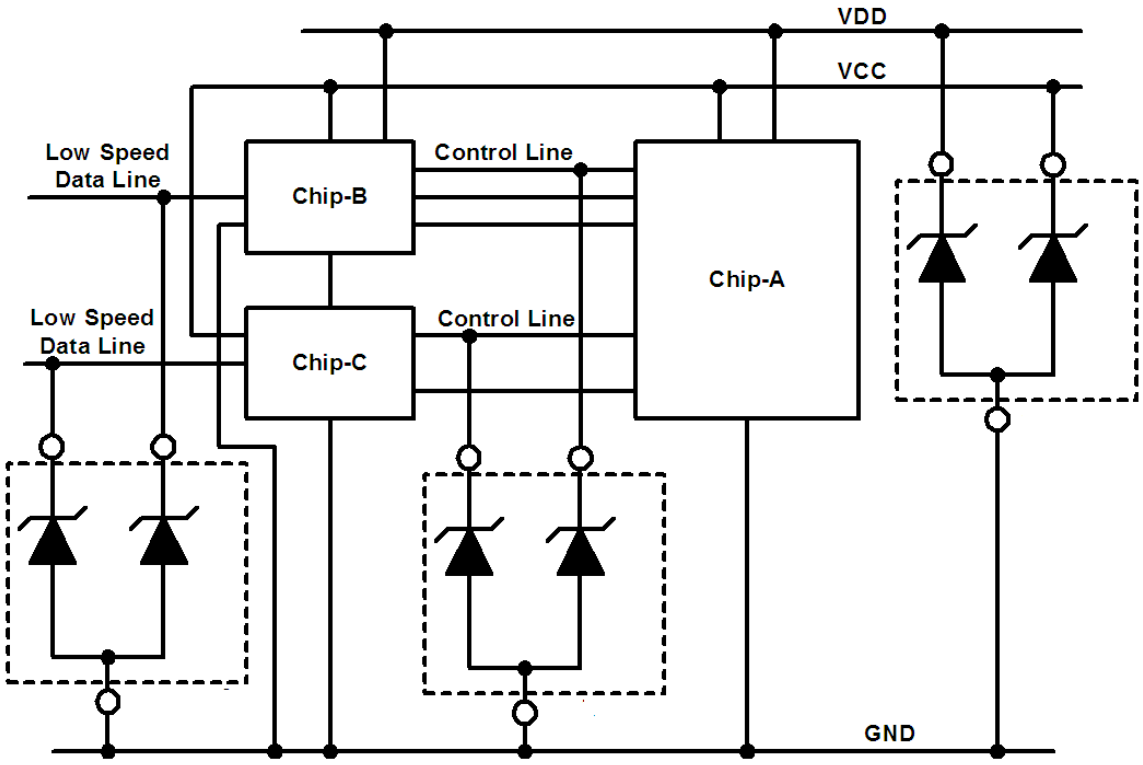
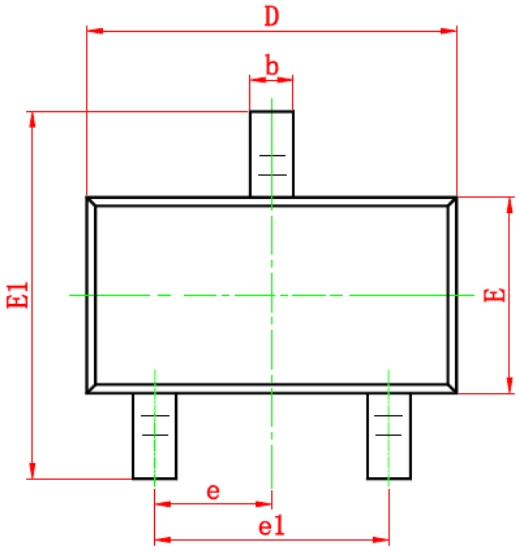


Fig. 2

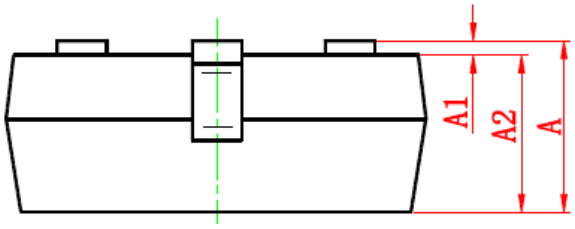
Mechanical Details

SOT23-3L PACKAGE DIAGRAMS

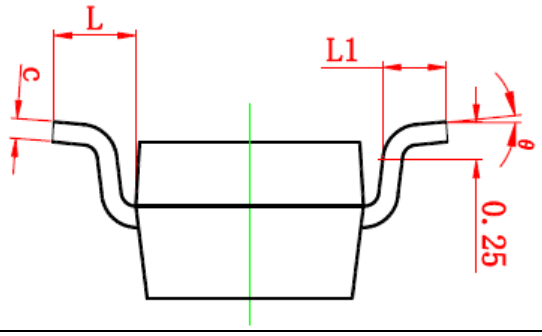
TOP VIEW



SIDE VIEW



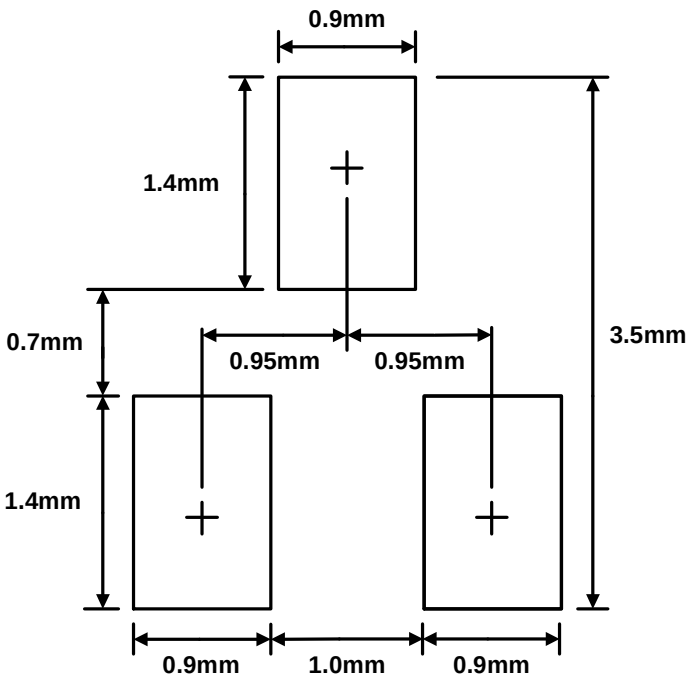
END VIEW



PACKAGE DIMENSIONS

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.900	1.150	0.035	0.045
A1	0.000	0.100	0.000	0.004
A2	0.900	1.050	0.035	0.041
b	0.300	0.500	0.012	0.020
c	0.080	0.150	0.003	0.006
D	2.800	3.000	0.110	0.118
E	1.200	1.400	0.047	0.055
E1	2.250	2.550	0.089	0.100
e	0.950 TYP		0.037 TYP	
e1	1.800	2.000	0.071	0.079
L	0.550 REF		0.022 REF	
L1	0.300	0.500	0.012	0.020
θ	0°	8°	0°	6°

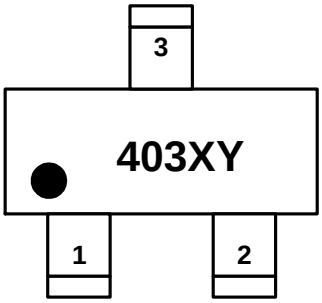
LAND LAYOUT



Notes:

This LAND LAYOUT is for reference purposes only. Please consult your manufacturing partners to ensure your company's PCB design guidelines are met.

MARKING CODE



403 = Device Code
X = Date Code
Y = Control Code

Part Number	Marking Code
AZ4024-02S (Green part)	403XY
AZ4024-02S (Engineering part)	EE104

Ordering Information

PN#	Material	Type	Reel size	MOQ/internal box	MOQ/carton
AZ4024-02S.R7G	Green	T/R	7 inch	4 reel=12,000/box	6 box=72,000/carton

Revision History

Revision	Modification Description
Revision 2010/08/30	Formal Release.
Revision 2011/07/28	1. Update the Company Logo. 2. Add the Ordering Information.
Revision 2011/11/30	Correct the symbols of ESD and Surge Clamping Voltage to be V_{ESD_clamp} and V_{surge_clamp}.