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Application Note

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Auto-Wake/Sleep Using the MMA8451, 2, 3Q

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1.0 Introduction

Accelerometers are commonly used in hand-held electronics and/or battery operated electronic devices. Consumption of current in the entire system is a critical feature of the product design. Users do not want to be inconvenienced by continually recharging or changing out batteries. When designing in the accelerometer, battery power usage is often a critical feature which concerns many designers.

Therefore, current consumption of the sensor as well as of the entire system should be paramount design considerations. If the system processor is used often only for processing data from the accelerometer, then it is ideal to embed the intelligence in the sensor to avoid burdening the system processor from running continually. The flexibility of embedded interrupt driven functions and selectable data rates with trade-offs for resolution, response time, and current are the types of intelligent features in the MMA8451, 2, 3Q.

This application note will explain the following:

- The Auto-Wake/Sleep feature
- Description of the configuration procedure with example register settings and code.

1.1 Key Words

Accelerometer, Output Data Rate (ODR), Current, Standby Current, Power Down Mode Current, Low Power Mode, Noise, Auto-Wake/Sleep, Sleep Timer, Sensor.

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1.2 Summary

The MMA845xQ can be used to cycle between different ODRs, which results in overall lower current consumption of the device. This can be achieved from several programmable functions.

2.0 MMA8451, 2, 3Q Consumer 3-axis Accelerometer 3 by 3 by 1 mm

The MMA8451, 2, 3Q has a selectable dynamic range of ±2g, ±4g, ±8g. The device has 8 different output data rates, selectable high pass filter cut-off frequencies, and high pass filtered data. The available resolution of the data and the embedded features is dependant on the specific device.

Note: The MMA8450Q has a different memory map and has a slightly different pinout configuration.

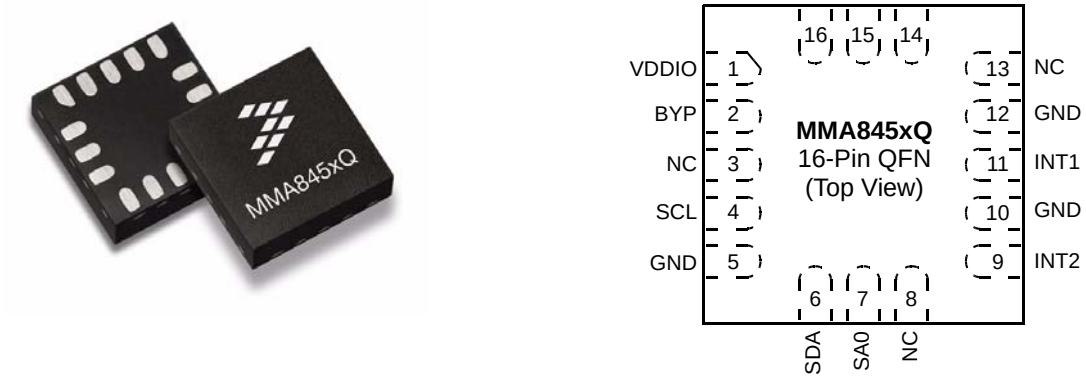

Figure 1. MMA8451, 2, 3Q Consumer 3-axis Accelerometer 3 by 3 by 1 mm

2.1 Output Data, Sample Rates and Dynamic Ranges of all Three Products

2.1.1 MMA8451Q

1. **14-bit data**
   2g (4096 counts/g = 0.25 mg/LSB) **4g** (2048 counts/g = 0.5 mg/LSB) **8g** (1024 counts/g = 1 mg/LSB)
2. **8-bit data**
   2g (64 counts/g = 15.6 mg/LSB) **4g** (32 counts/g = 31.25 mg/LSB) **8g** (16 counts/g = 62.5 mg/LSB)
3. **Embedded 32 sample FIFO (MMA8451Q)**

2.1.2 MMA8452Q

1. **12-bit data**
   2g (1024 counts/g = 1 mg/LSB) **4g** (512 counts/g = 2 mg/LSB) **8g** (256 counts/g = 3.9 mg/LSB)
2. **8-bit data**
   2g (64 counts/g = 15.6 mg/LSB) **4g** (32 counts/g = 31.25 mg/LSB) **8g** (16 counts/g = 62.5 mg/LSB)

2.1.3 MMA8453Q Note: No HPF Data

1. **10-bit data**
   2g (256 counts/g = 3.9 mg/LSB) **4g** (128 counts/g = 7.8 mg/LSB) **8g** (64 counts/g = 15.6 mg/LSB)
2. **8-bit data**
   2g (64 counts/g = 15.6 mg/LSB) **4g** (32 counts/g = 31.25 mg/LSB) **8g** (16 counts/g = 62.5 mg/LSB)

3.0 Configuring the MMA8451, 2, 3Q into Auto-Wake/Sleep Mode

The MMA8451, 2, 3Q can be configured to transition between different sample rates (different current consumption) based on different selected events. Enabling this feature can be accomplished by enabling the Sleep Mode and setting a timeout period. Then the functions of interest must be set to trigger the device to wake. Both Wake and Sleep are considered “Active” Modes because data and interrupts are available. The difference between the modes is that the sample rate in Sleep Mode is limited to a maximum of 50 Hz. The advantage of using the Auto-Wake/Sleep is that the system can automatically transition to a higher sample rate (higher current consumption) when needed but spends the majority of the time in the Sleep Mode (lower current) when the device does not require higher sampling rates. This can all be triggered on selected events. The Low Noise bit (Register 0x2A bit 2) can be used as well with this feature. ***Be aware that using the Low Noise bit will limit the dynamic range to 4g, regardless of the set range of the full scale value.*** The oversampling mode can also be changed from Active Sleep Mode to Active Wake Mode. The Sleep Mode oversampling option is set in **Register 0x2B** using **bit 3** and **bit 4 SMODS0** and **SMODS1**. The Active Wake Mode oversampling option is set in **Register 0x2B** using **bit 0** and **bit 1 MODS0** and **MODS1**. For example the device can be configured to be in Low Power Mode when asleep at 1.56 Hz to be in the lowest current consumption configuration. Then the device can be set for High Resolution Mode at 6.25 Hz when awake to be prepared to take higher resolution data for a tilt application.

Figure 2 shows transition states from the Wake, Sleep and Standby modes.

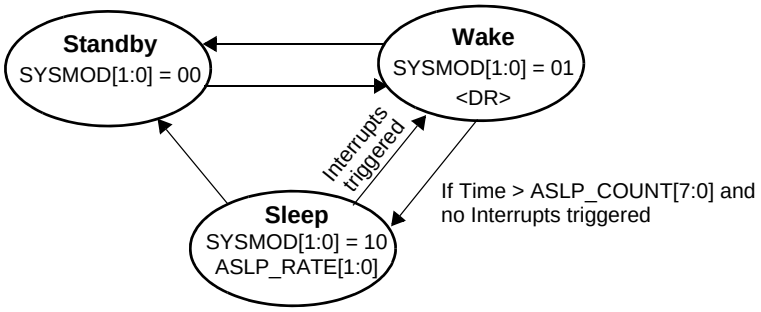

Figure 2. Mode Transitions

Table 1 compares how the current consumption changes with the data rate and with the oversampling mode chosen. The oversampling modes are “Normal”, “Low Noise and Low Power”, “High Resolution” and “Low Power”. The oversampling ratios are given at each data rate along with the current consumption values for each. The more averaging done internally results in higher current consumption. Note the Low Power Mode has the least amount of averaging and the lowest current consumption.

Table 1. (S)MODS Oversampling Options with Current Consumption Values

Mode ODR	Normal		Low Noise and Low Power		High Resolution		Low Power	
	Current μA	OS Ratio	Current μA	OS Ratio	Current μA	OS Ratio	Current μA	OS Ratio
800	165	2	165	2	165	2	165	2
400	165	4	165	4	165	4	85	2
200	85	4	85	4	165	8	44	2
100	44	4	44	4	165	16	24	2
50	24	4	24	4	165	32	14	2
12.5	24	16	8	4	165	128	6	2
6.25	24	32	8	8	165	256	6	4
1.5625	24	128	8	32	165	1024	6	16

Table 2 shows the list of functions that will delay the device from returning to sleep and waking from sleep. Note that the MMA8451Q is the only device that contains the FIFO. The FIFO can delay the device from going to sleep but it is not capable of waking the device from sleep. The transient, portrait/landscape, tap, and motion/freefall functions can all delay the device from sleep by servicing the interrupt before the timeout period. They can also wake the device from sleep. The Auto-Sleep interrupt indicates when the device changes modes from Wake to Sleep or Sleep to Wake but the interrupt does not affect the state change. Also the data ready interrupt does not affect the state change from the Wake to Sleep or Sleep to Wake state.

Table 2. Interrupt Sources and the effects on the state change from Wake to Sleep and Sleep to Wake Modes

Interrupt Source	Event Restarts Timer and Delays Return-to-Sleep	Event will Wake-from-Sleep
FIFO_GATE	Yes	No
SRC_TRANS	Yes	Yes
SRC_LNDPRT	Yes	Yes
SRC_PULSE	Yes	Yes
SRC_FF_MT	Yes	Yes
SRC_ASLP	No	No
SRC_DRDY	No	No

Note that to configure the Auto-Wake/Sleep functionality, the selected embedded functions must be enabled (Register 0x2D) and the same corresponding functions must be set to “Wake-from-Sleep” (Register 0x2C) if they are to be used to wake the device.

All enabled functions will still function in Sleep Mode at the sleep ODR. Only the functions that have been selected for “Wake-from-Sleep” will wake the device. If nothing is selected to Wake-from-Sleep then the device will remain in Sleep Mode and will never wake up.

This section reviews the different registers involved in configuring the device for auto-wake/sleep.

1. Register 0x2B bit 2 – **SLPE** Enable Sleep bit
2. Register 0x2B Set the Sleep Mode Oversampling Rate
3. Register 0x2A Sleep Sample Rate and Wake Sample Rate
4. Register 0x29 Timeout Counter
5. Register 0x2D Enable the Interrupts for the Selected Functions
6. Register 0x2E Route the Interrupts to INT1 or INT2
7. Register 0x2C Enable the Wake-from-Sleep Interrupts

3.1 Set the Sleep Enable Bit

If the Sleep Enable bit (Register 0x2B bit 2) is **NOT** enabled then the device can only toggle between Standby and Wake Mode by writing to the Active bit in Register 0x2A. When the Sleep Enable bit is enabled the device can transition between Standby, Wake, and Sleep. The **SLPE** bit is shown as bit 2 in Table 4.

3.2 Set the Sleep Mode and Wake Mode Oversampling Mode

There are four different oversampling modes described in Table 3 They are “Normal”, “Low Noise and Low Power”, “High Resolution” and “Low Power”. The oversampling mode changes the current consumption, resolution and also the debounce counter timers in the part. The device can be configured to be in Low Power Mode while in Sleep and then to Normal Mode when awake or any of the other fifteen combinations. This allows for further current savings in the Sleep Mode. The different bit settings are shown in Table 3. The Wake oversampling modes configured from bit 0 and bit 1 in Register 0x2B. The Sleep oversampling modes are configured from bit 3 and bit 4 in SMODS in Register 0x2B.

Table 3. Settings for Oversampling Modes

(S)MODS1	(S)MODS0	Power Mode
0	0	Normal
0	1	Low Noise and Low Power
1	0	High Resolution
1	1	Low Power

Table 4. 0x2B CTRL_REG2 Register (Read/Write) and Description

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ST	RST	0	**SMODS1**	**SMODS0**	**SLPE**	**MODS1**	**MODS0**

3.3 Configure the Sleep Sample Rate and Wake Sample Rate

It is important to note that when the device is in Sleep Mode, the system ODR is overwritten by the data rate set by the **ASLP_RATE** field in the **CTRL_REG1** Register (0x2A). The Sleep Sample Rate (ASLP_RATE[0:1]) and the Wake Mode Sample Rate (DR[0:3]) are found in Table 5. The different bit settings for the Sleep Mode Sample Rate can be found in Table 6. The bit settings for the Wake Mode Sample Rates are found in Table 7.

Table 5. 0x2A CTRL_REG1 Register (Read/Write) and Description

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ASLP_RATE1	ASLP_RATE0	DR2	DR1	DR0	LNOISE	F_READ	ACTIVE

Table 6. Sleep Mode Sample Rate Description

ASLP_RATE1	ASLP_RATE0	ODR	Period
0	0	50 Hz	20 ms
0	1	12.5 Hz	80 ms
1	0	6.25 Hz	160 ms
1	1	1.56 Hz	640 ms

Table 7. Wake Mode Sample Rate Description

DR2	DR1	DR0	ODR	Period
0	0	0	800.0 Hz	1.25 ms
0	0	1	400.0 Hz	2.5 ms
0	1	0	200.0 Hz	5 ms
0	1	1	100.0 Hz	10 ms
1	0	0	50.0 Hz	20 ms
1	0	1	12.5 Hz	80 ms
1	1	0	6.25 Hz	160 ms
1	1	1	1.56 Hz	640 ms

3.4 Set the Timeout Counter

The **ASLP_COUNT** Register 0x29 shown in Table 8 sets the minimum time period of inactivity required to change the current ODR value from the value specified in the **DR[2:0]** to that in the **ASLP_RATE[1:0]** (Register 0x2A). Of course this only occurs provided the **SLPE** bit is set.

Table 8. 0x29 ASLP_COUNT Register (Read/Write) and Description

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D7	D6	D5	D4	D3	D2	D1	D0

D7-D0 defines the minimum duration time to change current ODR value from **DR** to **ASLP_RATE**. Time step and maximum value depend on the ODR chosen. See Table 9.

Table 9. ASLP_COUNT Relationship with ODR

Output Data Rate (ODR)	Duration	ODR Time Step	ASLP_COUNT Step
800	0 to 81s	1.25 ms	320 ms
400	0 to 81s	2.5 ms	320 ms
200	0 to 81s	5 ms	320 ms
100	0 to 81s	10 ms	320 ms
50	0 to 81s	20 ms	320 ms
12.5	0 to 81s	80 ms	320 ms
6.25	0 to 81s	160 ms	320 ms
1.56	0 to 162s	640 ms	640 ms

3.5 Enable the Interrupts to be used in the System and Route to INT1 or INT2

The interrupt functions must be enabled in Register 0x2D per Table 10 for the event to trigger the Auto-Wake/Sleep. The functions must also be configured with the appropriate thresholds and timing values to detect the events.

Table 10. Register 0x2D CTRL_REG4 Register (Read/Write) and Description

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INT_EN_ASLP	INT_EN_FIFO	INT_EN_TRANS	INT_EN_LNDPRT	INT_EN_PULSE	INT_EN_FF_MT	—	INT_EN_DRDY

The corresponding interrupt enable bit allows the function to route its event detection flag to the interrupt controller. The interrupt controller routes the enabled interrupt to the INT1 or INT2 pin. By default all interrupts are routed to INT2 and the corresponding configuration register bit value is 0. To route a functional block to INT1 instead of the default, set the corresponding configuration register bit to 1. The configuration register bit settings are shown in Table 11.

Table 11. Register 0x2E CTRL_REG5 Register (Read/Write) and Description

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INT_CFG_ASLP	INT_CFG_FIFO	INT_CFG_TRANS	INT_CFG_LNDPRT	INT_CFG_PULSE	INT_CFG_FF_MT	—	INT_CFG_DRDY

3.6 Enable the Interrupt Sources that Wake the Device

The register to control which interrupts will wake the device are configured in Register 0x2C shown in Table 12. **There are five (5) functions that can be used to keep the sensor from falling asleep if they are enabled.** These are the Transient, Orientation, Tap, Motion/FF and the FIFO. **There are only four (4) functions used to wake the device.** The FIFO will not wake the device from sleep. Also note the Auto-Wake/Sleep interrupt and the data ready interrupt do not affect the Wake/Sleep. Note that the FIFO is only available in the MMA8451Q device.

Table 12. Register 0x2C CTRL_REG3 Interrupt Control Register and Description

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FIFO_GATE	WAKE_TRANS	WAKE_LNDPRT	WAKE_PULSE	WAKE_FF_MT	—	IPOL	PP_OD

Note: The FIFO is flushed whenever the system ODR changes in order to prevent mixing the FIFO data from different time domains unless the FIFO_GATE (bit 7) is set. Also, the FIFO cannot wake the device from sleep but can prevent the device from going to sleep. Details of the functionality of the FIFO is captured in Table 13.

Table 13. Behavior of FIFO under Wake/Sleep Conditions

FIFO INT Enabled	Wake-from-Sleep Enabled	Result
NO	NO	FIFO will fall asleep when the sleep timer times out and no other interrupt wakes the system. There is an AUTOMATIC flush and the FIFO starts refilling at the Sleep ODR from 0. If another functional block causes the device to wake the FIFO will FLUSH itself again and start filling at the Wake ODR.
YES	NO	With the interrupt enabled the FIFO can be read and flushed clearing the interrupt. The system is kept from falling asleep by reading the status after the interrupt is set. The FIFO does not have to be flushed to keep the device in Wake Mode- as long as the FIFO status is read continuously after the FIFO interrupt is enabled. If the system falls asleep (and no new interrupts occur during the timeout period), the FIFO AUTOMATICALLY flushes and starts refilling at the Sleep ODR from 0 and stores at the Wake ODR.
NO	YES	FIFO will fall asleep if no wake events occur within the timeout period. Last data remains here in the FIFO until it is flushed. Once the FIFO is flushed, it will start collecting the new data at the current ODR.
YES	YES	With interrupt enabled, the FIFO can be read and flushed (clearing the interrupt) . Note: Reading the FIFO status will keep the system from falling asleep. If the system does fall asleep (and no interrupts occur during the timeout period) then the FIFO will stop collecting any data. The last data will be held in the FIFO. Once the FIFO is flushed, it will start collecting the new data at the current ODR.

4.0 Example Configuration for the Auto-Wake/Sleep Function

The following are the steps to configure the Auto-Wake/Sleep function with the registers of importance in Table 14. In this example, the data rate will be set to 100 Hz in Wake Mode and 6.25 Hz in Sleep Mode. The Oversampling Mode will be set to High Resolution in the Wake Mode and Low Power Mode in Sleep Mode. The timeout period will be set to 20 seconds. The wake triggers will be tap and motion. There may be other interrupts that are enabled in the system including orientation detection, but these will not wake the device in this example.

Table 14. Registers used for Auto-Wake/Sleep Functionality

Reg	Name	Definition	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0B	SYSMOD	System Mode R	FGERR	FGT_4	FGT_3	FGT_2	FGT_1	FGT_0	SYSMOD1	SYSMOD0
0C	INT_SOURCE	Interrupt Status R	SRC_ASLP	SRC_FIFO	SRC_TRANS	SRC_LNDPRT	SRC_PULSE	SRC_FF_MT	—	SRC_DRDY
29	ASLP_COUNT	Auto-Sleep Counter R/W	D7	D6	D5	D4	D3	D2	D1	D0
2A	CTRL_REG1	Control Reg1 R/W	ASLP_RATE1	ASLP_RATE0	DR2	DR1	DR0	LNOISE	F_READ	ACTIVE
2B	CTRL_REG2	Control Reg2 R/W	ST	RST	0	SMODS1	SMODS0	SLPE	MODS1	MODS0
2C	CTRL_REG3	Control Reg3 R/W (Wake Interrupts from Sleep)	FIFO_GATE	WAKE_TRANS	WAKE_LNDPRT	WAKE_PULSE	WAKE_FF_MT	—	IPOL	PP_OD
2D	CTRL_REG4	Control Reg4 R/W (Interrupt Enable Map)	INT_EN_ASLP	INT_EN_FIFO	INT_EN_TRANS	INT_EN_LNDPRT	INT_EN_PULSE	INT_EN_FF_MT	—	INT_EN_DRDY
2E	CTRL_REG5	Control Reg5 R/W (Interrupt Configuration)	INT_CFG_ASLP	INT_CFG_FIFO	INT_CFG_TRANS	INT_CFG_LNDPRT	INT_CFG_PULSE	INT_CFG_FF_MT	—	INT_CFG_DRDY

4.1 Example Procedure for Configuring the Auto-Wake/Sleep Function Conditions

- Dynamic Range = 2g
- Sleep Timeout period = 20 seconds
- Wake Triggers = Tap and Motion
- Wake Sample Rate = 100 Hz,
- Wake Oversampling Mode = High Resolution
- Sleep Sample Rate = 6.25 Hz
- Sleep Oversampling Mode = Low Power

Step 1: Put the device in Standby Mode

Register 0x2A CTRL_REG1

CTRL_REG1_Data = IIC_RegRead(0x2A);

CTRL_REG1_Data& = 0xFE; //Clear Active Bit

IIC_RegWrite(0x2A,CTRL_REG1_Data);

Step 2: To enable the Auto-Wake/Sleep set bit 2 in Register 0x2B, the **SLPE** bit.

Register 0x2B CTRL_REG2

CTRL_REG2_Data = IIC_RegRead(0x2B); //Store value in the Register

CTRL_REG2_Data| = 0x04; //Set the Sleep Enable bit

IIC_RegWrite(0x2B, CTRL_REG2_Data); //Write the updated value into CTRL_REG2.

Step 3: The sleep sample rate must be chosen by writing in the corresponding sample rate value to bits 6 and 7 ASLP_RATE0 and ASLP_RATE1 (01) and the Wake Sample rate bits 5, 4 and 3 to DR (011) in Register 0x2A.

Register 0x2A CTRL_REG1 ASLP_RATE = 01 (6.25 Hz), DR = 011(100 Hz)

CTRL_REG1_Data = IIC_RegRead(0x2A);

CTRL_REG1_Data& = 0x5E; //clear the bits that should be cleared for the sample rates

CTRL_REG1_Data| = 0x58; //Set ASLP = 6.25 Hz, DR = 100 Hz

IIC_RegWrite(0x2A,CTRL_REG1_Data);

Step 4: Set the Wake Oversampling Mode to High Resolution (10) and the Sleep Oversampling Mode to Low Power (11)

CTRL_REG2_Data = IIC_RegRead(0x2B);

CTRL_REG2_Data& = 0xE4; //puts both Oversampling modes in Normal Mode

CTRL_REG2_Data| = 0x1A; //Wake High Res, Sleep Low Power

IIC_RegWrite(0x2B,CTRL_REG2_Data);

Step 5: The Interrupt for the event to trigger the device to wake up must be enabled by writing to Register 0x2D, CTRL_Reg4. Bits 2 through 7 will affect the Auto-Wake/sleep. The data ready interrupt doesn't trigger the Auto-Wake/Sleep mechanism.

Example: Set Pulse and Orientation and Motion 1 and Auto-Wake/Sleep Interrupts

Enabled in the System

IIC_RegWrite(0x2D, 0x9C);

Step 6: Route the interrupt chosen and enabled to either INT1 or INT2 in Register 0x2E CTRL_REG5.

Example: Route Pulse, Motion1 and Orientation to INT2 and Auto-Sleep to INT1.

IIC_RegWrite(0x2E,0x80);

Step 7: Enable the interrupts that will wake the device from sleep. There can be more interrupts enabled in Step 4 than in Step 6. Only interrupts that are Enabled in Step 4 and that have the "Wake-from -Sleep" bit set in Register 0x2C will actually wake the device.

Example: Choose Pulse and Motion to wake the device from sleep

IIC_RegWrite(0x2C,0x18);

Step 8: Set the Dynamic Range to 2g

Register 0x0E XYZ_DATA_CFG

XYZ_CFG_Data = IIC_RegRead(0x0E);

XYZ_CFG_Data & = 0xFC; //Clear the FS bits to 00 2g

IIC_RegWrite(0x0E, XYZ_CFG_Data);

Step 9: Write an Interrupt Service routine to monitor the Auto-Sleep Interrupt

```
Interrupt void isr_KBI (void)
{
      //clear the interrupt flag
      CLEAR_KBI_INTERRUPT;
      //Determine the source of interrupt by reading the system interrupt register
      Int_SourceSystem = IIC_RegRead(0x0C);
      //Set up Case statement here to service all of the possible interrupts
      if ((Int_SourceSystem &=0x80)==0x80)
      {
            //Perform an Action since Auto-Sleep Flag has been set
            //Read the System Mode to clear the system interrupt
            Int_SysMod = IIC_RegRead(0x0B);
            if (Int_SysMod==0x02)
            {//sleep mode
            }
            else if (Int_SysMod==0x01)
            {//Wake Mode
            }
            else
            {//Error
            }
      }
}
```

Related Documentation

The MMA845xQ device features and operations are described in a variety of reference manuals, user guides, and application notes. To find the most-current versions of these documents:

1. Go to the Freescale homepage at:

   http://www.freescale.com/

2. In the Keyword search box at the top of the page, enter the device number MMA845xQ.
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