Freescale Semiconductor
Application Note

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Power Quad Flat No-Lead (PQFN) Package

1 Purpose

This document provides guidelines for Printed Circuit Board (PCB) design and assembly. Package performance attributes such as Moisture Sensitivity Level (MSL) rating, board level reliability and Thermal Resistance data are included as reference.

2 Scope

This document is written to generically encompass several different Power Quad Flat No-Lead (PQFN) packages assembled at Freescale internal assembly sites and external subcontractor sites. It should be noted that device specific information is not provided. This document serves only as a guideline to assist in the development of user specific solutions. Development effort will still be required by end users to optimize PCB mounting processes and board design.

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3 Power Quad Flat No-Lead (PQFN) Package

3.1 Package Description

The PQFN is a surface mount plastic package with lead pads located on the bottom surface of the package. All PQFN packages have either been designed with a single exposed die pad (flag) or multiple exposed die pads depending on device requirements and intended application. The industry standardization committee, JEDEC, has given a registered designator of MO-251 to describe the family of single exposed pad PQFN packages.

3.1.1 Package Application

The PQFN surface mount packages have been designed to meet the high power dissipation requirements of automotive, industrial, and commercial applications. Features such as solder die attach material, thick copper lead frames, exposed heatsinks, and heavy gauge aluminum wire capability, allow for efficient heat transfer out of the PQFN packages.

3.1.2 Package Dimensioning

Currently, PQFN packages range from 5 x 5 mm to 12 x 12 mm in body size.
Lead counts range from 16 to 36. The lead pads have been designed in both single-row and double-row configurations, depending upon the specific package requirements. The lead pitch of the perimeter leads is available in 0.65 mm, 0.80 mm, and 0.9 mm designs.

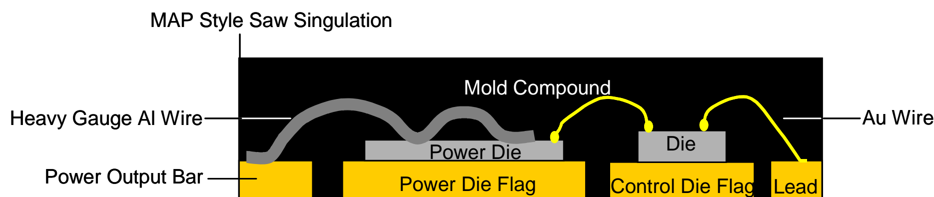


Figure 1. Cross-Section of a Custom PQFN MAP (Molded Array Package).

4 Printed Circuit Board Guidelines

4.1 Printed Circuit Board Design for PQFN Packages

PQFN packages have unique and varied footprints due to the use of exposed pads for thermal management. Care should be taken to design pads on a PCB that are compatible with the arrangement of unique features on the bottom-side of PQFN packages. The following guidelines can be used to help address a user specific solution.

4.1.1 Periphery I/O Pads

The board design should begin with copper pads that sit beneath the periphery leads of a mounted PQFN. These board pads should extend outside the PQFN edge a distance of approximately 0.15 mm (**Figure 2**). Solder fillet information along the PQFN package edge can be inconsistent, due to varying levels of oxidation on the bare copper surfaces exposed by the saw singulation assembly process, and the half etch lead configuration. Oxidation levels are influenced by handling and environmental exposure prior to board mounting. Removal of this oxidation through flux activation will be dependent on the end user's selection of the solder paste's inherent flux activity. All PQFNs are tested for solderability on a sample basis, at the package level, following assembly. The end user is advised to verify satisfactory component solder attach to the PCB with x-ray analysis.

The periphery lead length under the package should be the nominal value for the length, as taken from the case outlines for individual components. For example, Case Number 1503 for the 36 I/O 0.8 mm pitch PQFN has the minimum and maximum lead lengths at 0.95 mm and 1.20 mm respectively. Using the average value as the nominal lead length gives 1.075 mm for the lead length. The total pad length would thus be 0.15 + 1.075 = 1.225 mm.

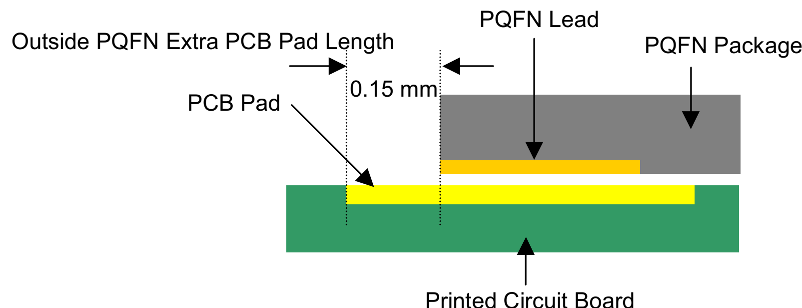


Figure 2. A Cross-Section of Package Lead and Suggested PCB Pad

The pad width should be approximately 0.025 mm wider than the nominal (case outline) lead dimension on each side (**Figure 3**). Using Case Outline 1503 again as example, the minimum and maximum periphery pad width is 0.48 mm and 0.62 mm, respectively. The average of these two measurements yields a nominal width of 0.55 mm. Adding 0.025 mm to each side results in a final pad width of 0.60 mm. All periphery pads have a reduced width at the package edge. No effort should be made to duplicate this on the PCB pad design.

Increasing the pad width 0.025 mm on both sides (0.05 mm total) helps with placement of parts during assembly by allowing a larger target for the seating of the PQFN. It will be important to keep at least 0.20 mm board spacing between adjacent pads. The 0.20 mm spacing will keep solder from bridging neighboring leads, causing them to electrically "short." For the 0.65 mm pitch PQFN periphery pads, the typical spacing between pads will be 0.20 mm. For the 0.8 mm pitch PQFN's the spacing increases to 0.3 mm.

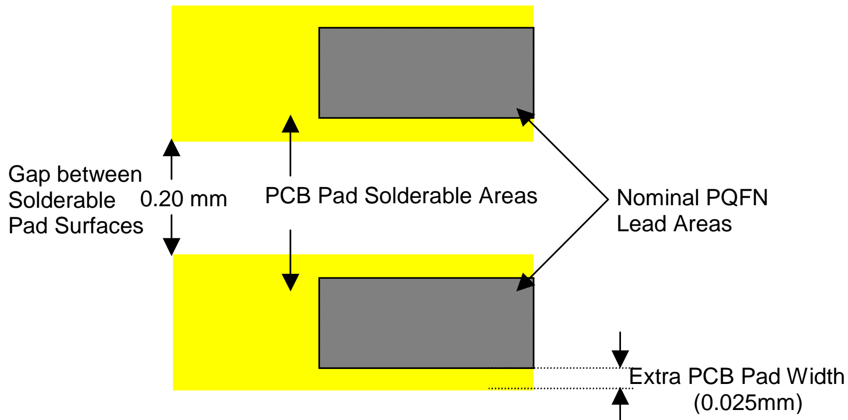


Figure 3. Top View of PCB and Suggested PCB Pad Size for PQFN Leads

Some PQFN packages have a dual row of I/O leads as illustrated in **Figure 4**. These packages require extra caution to ensure no solder bridging occurs between the leads. Again, the goal would be to have at least 0.20 mm between the heel and toe of the leads.

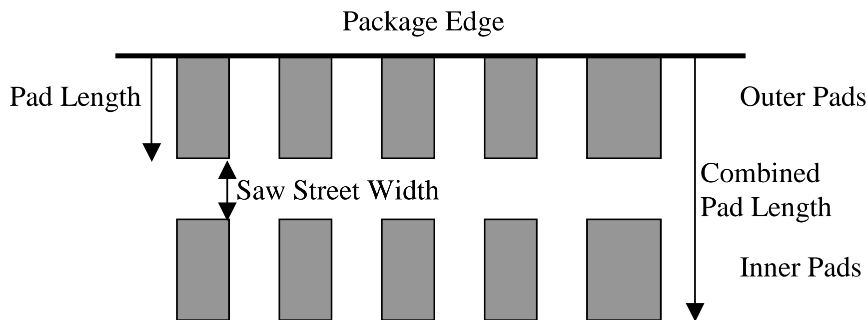


Figure 4. Dual Row Periphery Leads on PQFN from Case Outline 1445

The saw separation between the two rows of leads is created by sawing a gap between the lead rows. The width of this saw street is stated to be between 0.35 mm and 0.50 mm. The outer lead row length has a range of 0.65 mm to 0.85 mm. The combined pad length can vary between 1.9 mm and 2.1 mm.

For both lead rows, the width of each individual pad can be set with the rules supplied above. In order to determine an acceptable pad length, consider the smallest package. Edge-to-toe, the inner lead row distance will be 1.0 mm (0.65 mm minimum lead length + 0.35 minimum saw street width). Since the goal is to have a 0.20 mm gap between the outer PCB pad row and the inner package pad row, the length of 1.00 mm is a critical dimension for designing the outer PCB pad length.

Using the nominal (average value) of the outer package lead row length, 0.775 mm provides sufficient spacing to the inner package pad row. In the smallest outer package pad case with the minimum saw street width, the inner row is again 1.0 mm, thus, allowing 0.225 mm spacing from the outer PCB pad to the inner package pad row that is above the minimum 0.20 mm. For the

largest package pad, the outer row spacing from PCB outer row pad to the inner package pad increases to 0.425 mm ((0.85 + 0.35) - 0.775). If the package outer row is at its smallest and the saw street width is at its largest, the spacing between the outer PCB pad and the inner package pad is 0.375 mm.

Once the outer pad row length is chosen, the spacing between the inner and outer rows for the PCB needs to be set. In this example, the saw street has been conservatively chosen to be 0.5 mm. With a PCB outer pad row length of 0.775 mm and the saw street width of 0.50 mm, the inner PCB pad would start 1.275 mm inward from the package edge.

The back edge of the inner package row (heel) can be between 1.9 mm and 2.1 mm from the package edge. For the small case, the “ideal” inner PCB pad length would be 0.625 mm (1.9 - 1.275). For the largest case of 2.1 mm, the “ideal” PCB pad length would be 0.825 mm. By using the average (nominal spacing) between these two cases, 0.725 mm, sufficient overlap between the package pad and PCB pad allows for a good solder joint in both extremes. Additionally, this creates a small buffer of spacing between the inner pad row and the exposed pad. Further suggestions on how to create acceptable spacing between exposed pads and periphery pads will be discussed in the following sections.

Figure 5 shows a series of possibilities for the above PCB pad layout and variations for the package pad. Type A, has the smallest outer pad length, the smallest saw street width, and the shortest combined pad length for the package. In this case, the design guidelines work to keep the inner package pad from being too close to the outer PCB pad. For Type B, the saw street width has been changed to the maximum length and the PCB design is very compatible. In Type C, the outer package is at the largest size while the saw street width remains as small as allowed. Again, the design suggestions keep both package pads from being too near the opposing row PCB pads. Finally, in type D, the saw street width increases to the maximum allowed and the spacing between package pads and PCB pads remains acceptable.

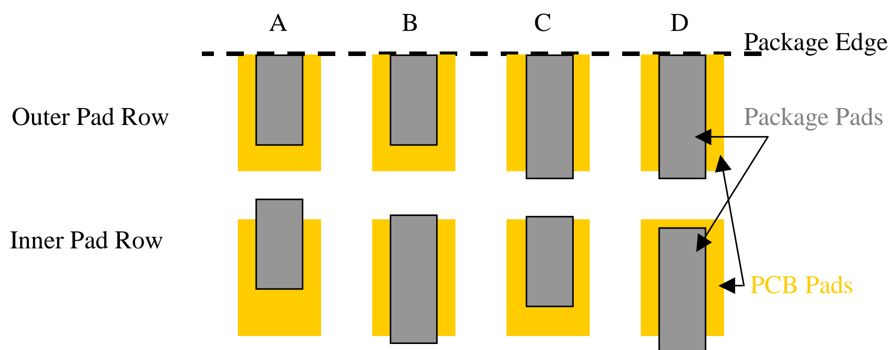


Figure 5. Examples of Dual Row Pad Layout with Extremes of Package Pads

For the periphery pads, Freescale encourages package users to have Non-Solder Mask Defined (NSMD) pad openings. The NSMD pad has demonstrated better reliability for solder-joint life than Solder Mask Defined (SMD) pads often used for ball grid array packages. The SMD pad is less reliable than NSMD pad because the solder mask edge on top of the copper pad creates a “stress riser” that pinches the solder joint during cycling, leading to crack initiation. Nonetheless,

SMD pads are very capable and are necessary for some applications whose primary reliability concern is not solder-joint life.

The NSMD pad should have a solder mask opening between 0.0625 mm and 0.075 mm around the perimeter of the copper pad size. Thus, the total opening size increases between 0.125 mm and 0.150 mm (**Figure 6**). The resulting spacing should meet the tolerance conditions found in most printed circuit board manufacturing environments.

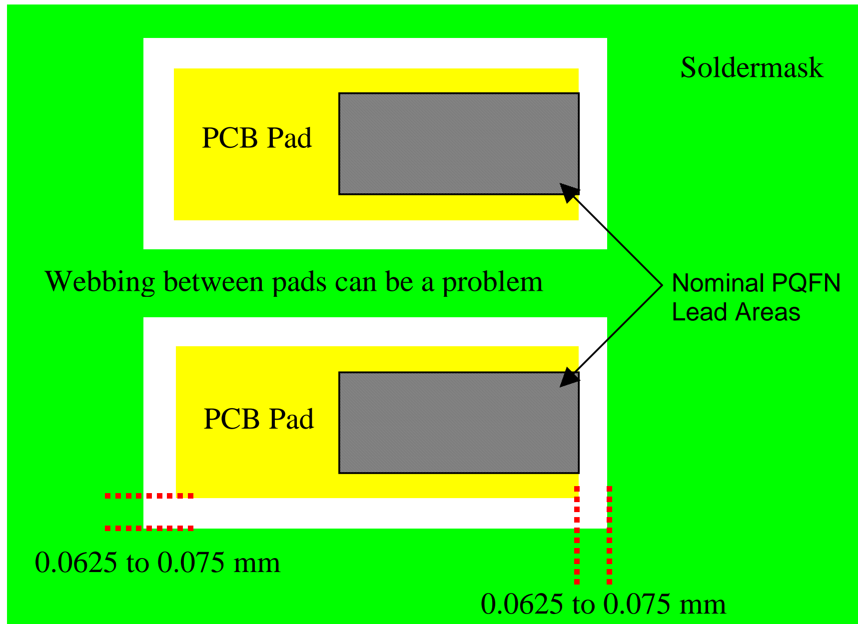


Figure 6. Top View of PQFN Pads on PCB Pads with Solder Mask Around PCB Pads

Depending upon the gap between neighboring periphery pads, there may or may not be space for a line of solder mask (**Figure 6**, green region between pads). In general, solder mask widths less than 0.150 mm are difficult to keep in place since they have little surface area for contact to the board, and thus, can lift off the board. Since there is a need to have 0.0625 mm to 0.075 mm clearance between copper pad edge and solder mask edge, the spacing between pads should be 0.275 mm or larger; this should allow for an adequate solder mask between individual leads.

For SMD pads, the expected solderable surface will be defined by the solder mask opening. The above rules will again apply for determining solderable surface. The copper pad under the solder mask could be increased between 0.0625 mm and 0.075 mm around the perimeter. The solder mask opening could decrease the same amount (**Figure 7**). By increasing the copper pad size, the tolerance of the solder mask alignment can be accounted for, resulting in a final solderable surface as defined by the solder mask opening on all four sides. Nominally, the solderable surface for both NSMD and SMD pads should be the same.

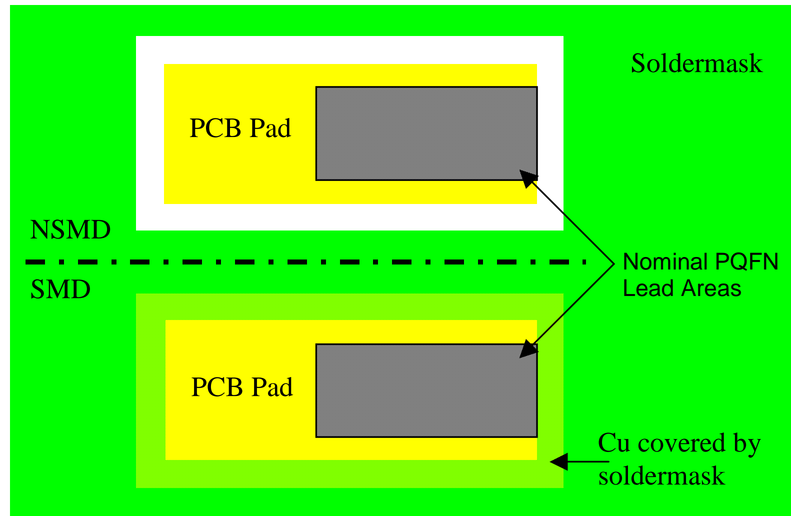


Figure 7. Comparison Between NSMD and SMD PCB Pads

4.1.2 Large Pads for Exposed Heatsinks

After completion of the periphery pad design, the larger exposed pads will be designed to create the mounting surface of the PQFN exposed heatsink(s). The primary transfer of heat out of the PQFN will be directly through the bottom surface of the exposed heatsink(s). To aid in the transfer of generated heat into the PCB, the use of an array of plated through-hole vias beneath the mounted part is recommended. The specific diameter and pitch of the via hole array will need to be defined by the end user. These are typically consistent in size with other drill hole diameters found on the application PCB. The JEDEC committee proposes an array of plated vias for thermally standardized testing with via hole diameters of 0.3 mm, and a center-to-center pitch of 1.2 mm per JESD51-5. This via pattern can be used as a starting point for creating a customer specific board design. If via holes are not capped, solder paste volume will be decreased as the inside of the vias are filled.

A PCB exposed pad that is lined with periphery pads, having at least 0.20 mm spacing between the periphery pad edge and the exposed pad, would again provide some assurance against solder bridging. Since there can be a large volume of solder beneath the package, to cover the large exposed pad region, the 0.20 mm spacing can be increased to approximately 0.25 mm (**Figure 8**). There will often be a resulting PCB exposed pad that is smaller in size than the PQFN exposed heatsink(s) after the application of the noted guidelines (**Figure 8**). This situation is acceptable since there will likely be a sufficient volume of solder beneath the PQFN exposed heatsolder masksink to mount the package and help remove heat from the package during usage.

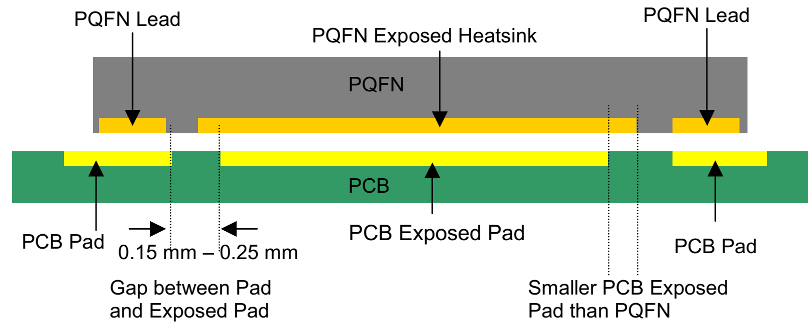


Figure 8. Comparison Between NSMD and SMD PCB Pads

The choice of NSMD or SMD for the large exposed pads is not as important as for the I/O periphery leads. The use of SMD exposed pads for the large copper areas reduce potential problems with solder bridging between the periphery leads and the exposed pads. In designing a SMD exposed pad, use the above rules for designing the copper area and reduce the opening for the solder mask on the copper area around the entire perimeter between 0.0625 mm and 0.075 mm. This reduces the solderable surface area a little more and can again make the PCB exposed pad smaller than the package exposed heatsink.

The maximum exposed pad size, in both X & Y directions, is 6.6 mm. With the above designed periphery pad lengths of 1.075 mm under the package, the spacing between each periphery pad row and the exposed pad can be calculated:

(9 - 6.6 - 2(1.075))/2 = 0.125 mm. This is below the minimum separation goal of 0.20 mm, needed to avoid solder bridging. To achieve the goal of 0.20 mm spacing, a reduction of the PCB exposed pad size by 0.075 mm around the perimeter would be sufficient. Alternatively, using 0.10 mm as the extra spacing may be easier since this will increase the gap between the periphery pads and the exposed pads to 0.225 mm. Finally, the exposed pad size with the 0.1 mm reduction around the perimeter would be: (6.6 - 0.1 - 0.1) = 6.4 mm, in total width.

Spacing between exposed pads on PQFNs is generally greater than 0.15 mm. Nonetheless, caution should be exercised to ensure spacings between exposed pads on the PCB are sufficient to block the potential of solder bridging. Due to the total solder paste volume printed on these large areas, the displacement of the solder paste during part mounting can potentially lead to neighbors meeting and result in solder bridging. Ensuring that the space between large exposed pads is greater than 0.20 mm reduces this problem. Additionally, by using SMD exposed pads, the spacing between them can be increased again.

PQFN packages can have unusual shapes for the large exposed pads. Many of these are due to the shape of the leadframe used to make the package. Incorporating these unusual shapes in the board side pad structure can be avoided in most cases. For example, the 16-Lead PQFN (Case Outline 1402) has “fingers” on pads 14 and 15 that extend to the package edge (**Figure 9**).

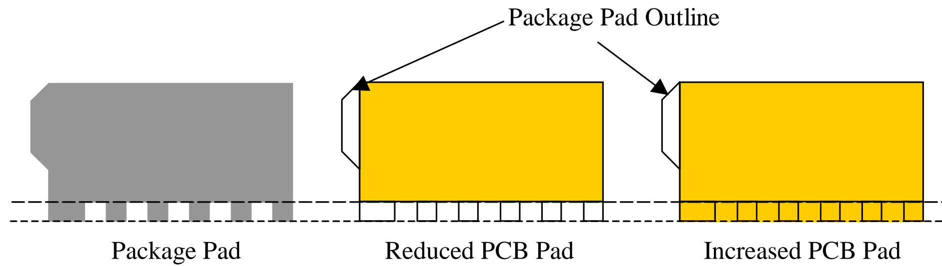


Figure 9. Examples of Exposed Pad Shapes and Possible PCB Pads Case Outline 1402

Making the PCB pad 1:1 may not be valuable. Instead, there are two possible alternatives: One is to reduce the PCB pad to be “square” to the package pad side; the other is to make the PCB pad “square” to the package edge.

Some PQFN packages will have un-numbered areas of exposed copper on the package. The creation of a PCB pad, to join these pads, is not recommended. In general, they are from the leadframe shape and may lead to unexpected electrical behavior if joined to the PCB. A good example can be found in Case Outline 1558 (**Figure 10**). There are a total of 4 small squares of exposed Cu on the package (circled in red). These are from the leadframe construction and if they are joined to the PCB, unanticipated electrical results for the component may occur. Additionally, this package has “cats ears” on the large exposed pad #16 (boxed in green). They are not important to solder-joint reliability nor are they important for thermal performance. Therefore, these regions of pad #16 may be left out of the PCB pad design.

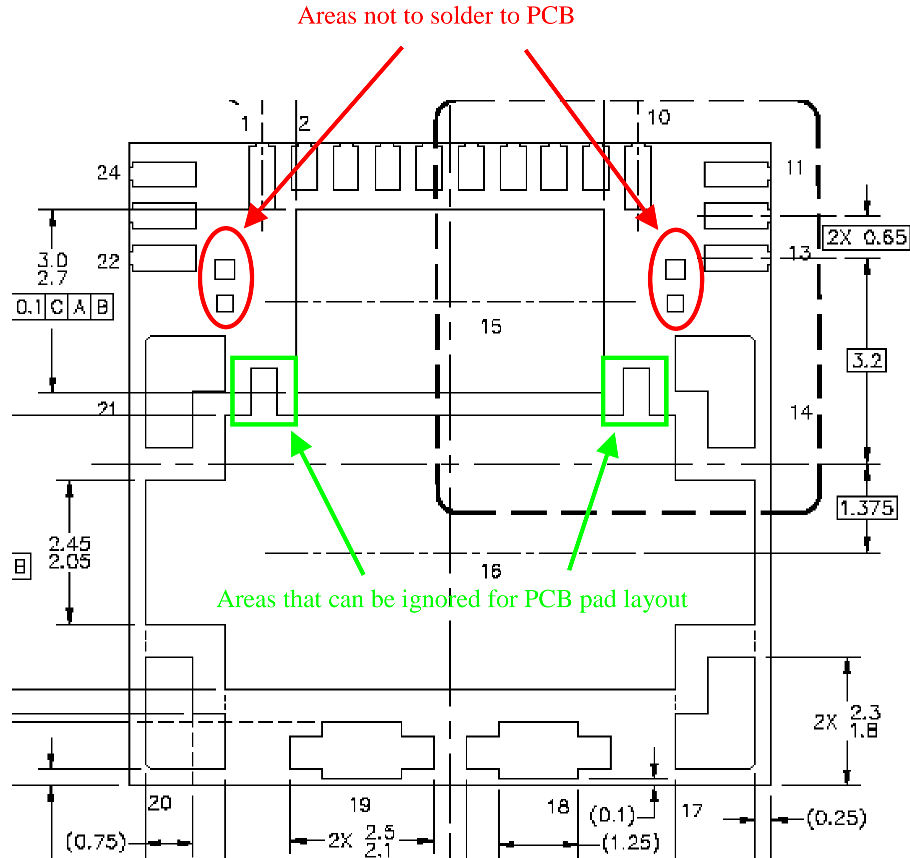


Figure 10. Example of Un-Numbered Areas Not to Be Joined to PCBs

4.2 Solder Paste Stencil Design for PQFN Packages

In general, solder paste stencil aperture openings can be one-to-one (1:1) with the peripheral PCB pad sizes. However, the stencil aperture openings should be smaller than the large PCB exposed pad regions to reduce the chance of solder bridging. There will be a large volume of solder in the PCB exposed pad region so it is necessary to create additional physical space between the exposed pad and the surrounding PCB pads. The suggested reduction of the stencil aperture opening by a minimum of 0.25 mm, as seen in **Figure 11**, allows compatibility with a maximum exposed pad size per any case outline drawing.

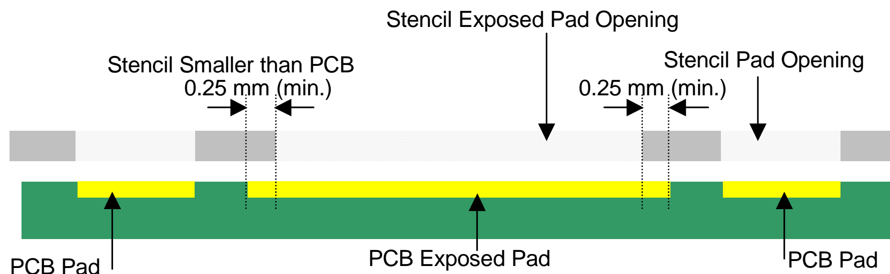


Figure 11. Reduced Solder Stencil Aperture for Exterior of Exposed Pad

During the solder screen print operation, a stencil blade can both deposit solder paste, and remove, or “scoop” it out, in the large aperture openings. In the large openings, the blade bends down into the opening thereby leaving less solder volume than anticipated. To mitigate the effect of scooping, the aperture can be broken up into an array of smaller openings. The array of openings will resemble a “window pane” pattern as seen in **Figure 12**. Large PCB exposed pads that are approximately 3.2 mm x 3.2 mm or larger in size should have a “window pane” stencil opening pattern. It is suggested that a spacing of 0.25 mm is used between the individual panes.

Stencil thickness can play an important role in solder joining. The stencil thickness is usually chosen by a combination of both typical industry practices and the requirements of the other components on a PCB module. Freescale has had success with solder joining processing by using stencil thickness of both 0.125 mm and 0.150 mm (5 and 6 mils). If stencils with a thickness greater than 0.150 mm are used, it is suggested to investigate a reduction of the stencil opening size, thereby reducing total solder volume to minimize the risk of solder bridging. For stencils thinner than 0.125 mm, aperture openings may have to be increased in order to provide enough volume of solder to get complete solder wetting between all contact surfaces.

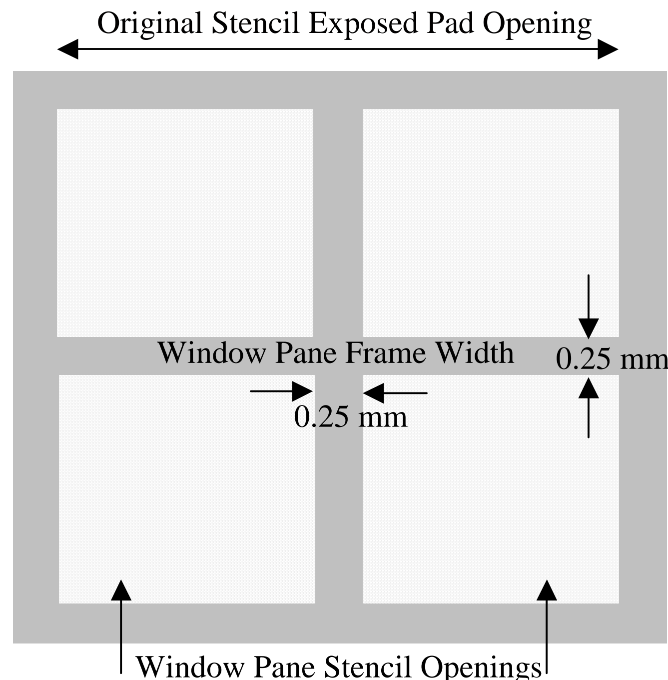


Figure 12. Window Pane Pattern for Exposed Pad Stencil Opening

Freescale encourages customers of PQFN packages to use stainless steel foil for the stencil material. The stainless steel stencil has a long usage life. Additionally, using a laser to cut the openings produces good opening uniformity. When followed by an electro-polish, the solder paste releases off the opening sidewalls more consistently after the printing process. Customers are strongly encouraged to use X-ray analysis before and after reflow to confirm that any stencil design can provide sufficient solder paste to the PCB and also keep good separation between regions of solder paste.

When working with packages like the QFN family, including the PQFN packages, the solder paste powder type can be important in consistently having equal volume per print. Type 3 powders in solder pastes are commonly available and work well. Type 4 powders are also recommended. For fine pitch parts like QFNs and PQFN (in particular the periphery pads), they are becoming more readily available.

Voiding in the reflowed solder should be minimized. Voiding occurs naturally since the solder paste flux and solvents will vaporize during the reflow due to the temperatures reached. Voiding can be minimized by careful selection of solder paste and optimizing the reflow temperature profile. The large exposed pads are most susceptible to having void formations. Additionally, exposed pads with thermal vias in them can have many voids, depending upon the care taken to plug or seal the vias properly.

If the guidelines described previously lead to unacceptably high voiding levels in board attach soldering, or prevention of high voiding levels is desired, modify the large exposed pad PCB design using the following the recommendations:

- **Step 1:** Identify the minimum size of the large exposed pad, as specified in the package outline drawing.
- **Step 2:** Following the pad outline as defined in step 1, split up the PCB pad into single, evenly distributed single pads. The recommended edge length of a single pad is between 1mm and 2mm. The distance between the single pads should be 0.2mm. (See **Figure 13** for details)
- **Step 3:** Place one via per pad in the pad center position. The via must be plugged or filled. The recommended via diameter is 0.5mm. (See **Figure 14** for details)
- **Step 4:** Generate solder paste stencil aperatures following the outline of the designed PCB pads. A 50μm peripheral reduction of the pad size is recommended for the aperature size. A 75μm radius of the aperature corner will lead to optimized solder paste release. (See **Figure 15** for details)

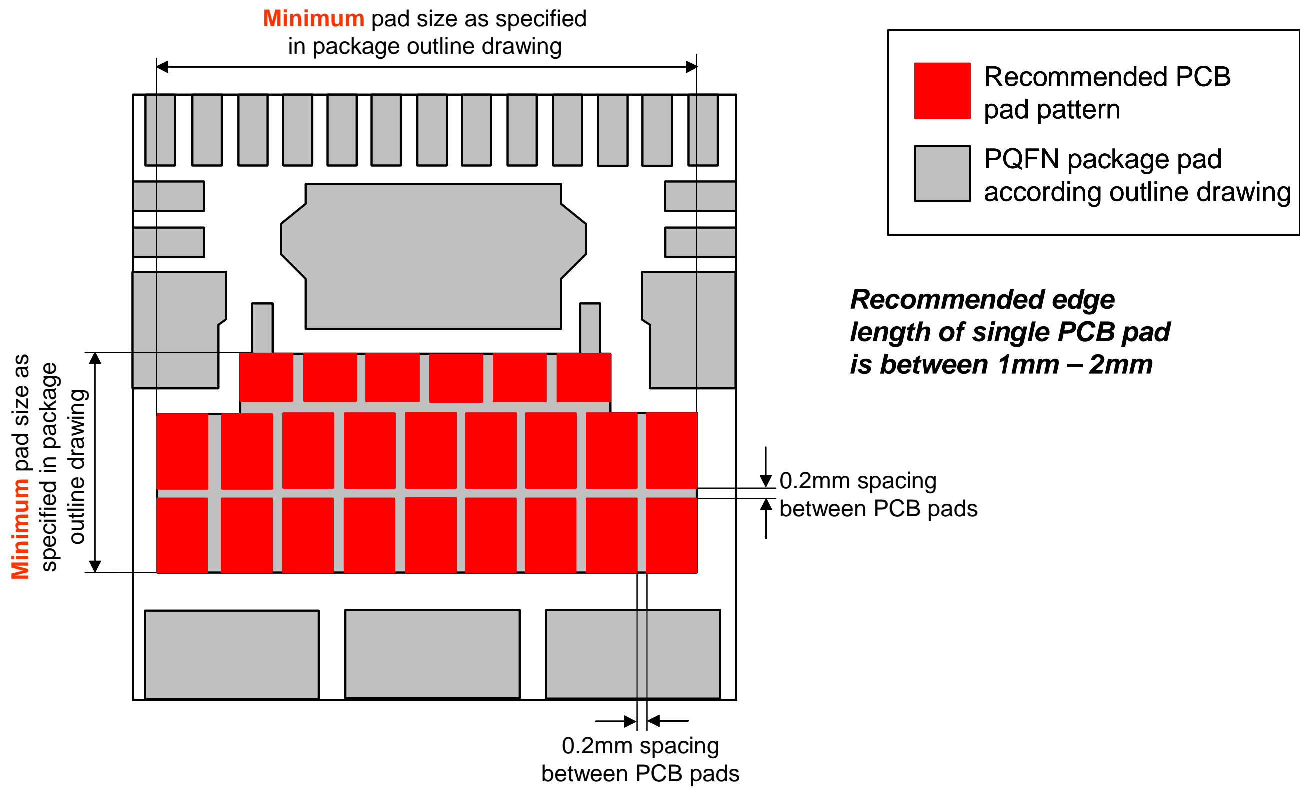
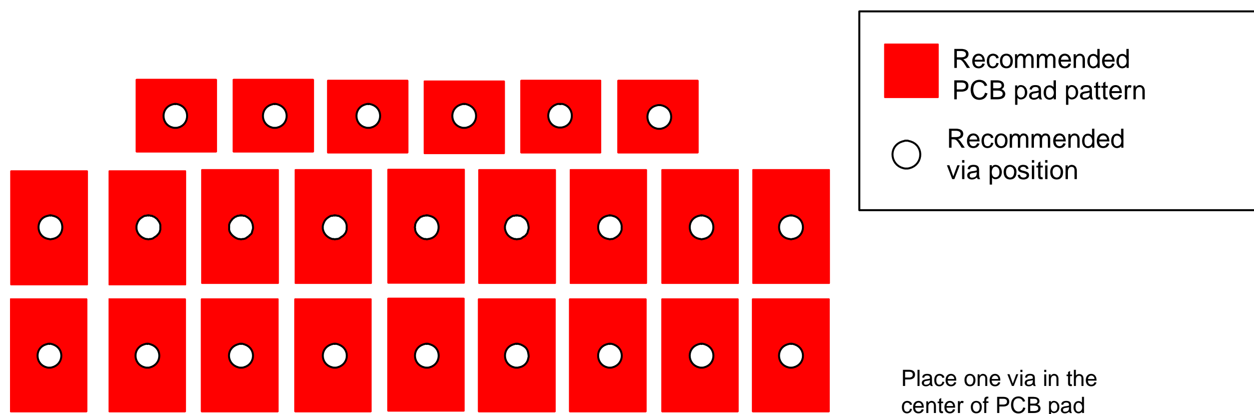


Figure 13. PCB Pad Design



Recommended via diameter is 0.5mm.
PTH (plated through hole) via must be plugged/ filled with epoxy or solder mask in order minimize void formation and to avoid any solder wicking into the via.

Figure 14. Via Design

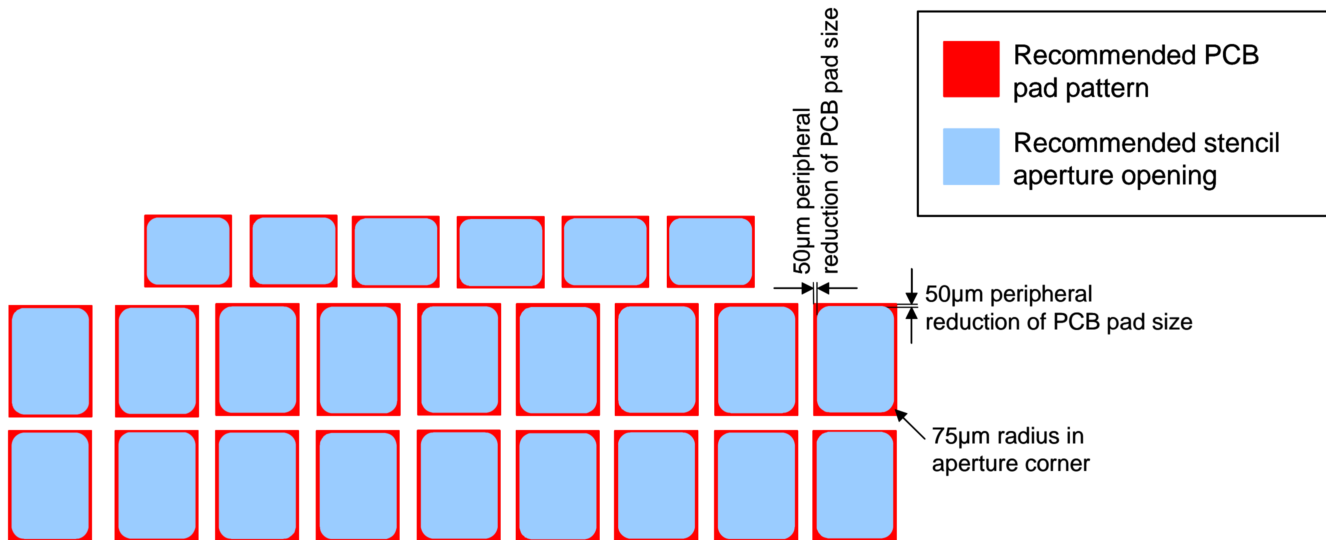


Figure 15. Stencil Design

- Typical appearance of the completed solder joint of the large exposed pad. Fully, void free solder joints with plugged, non-wetted via area in center of each pad.

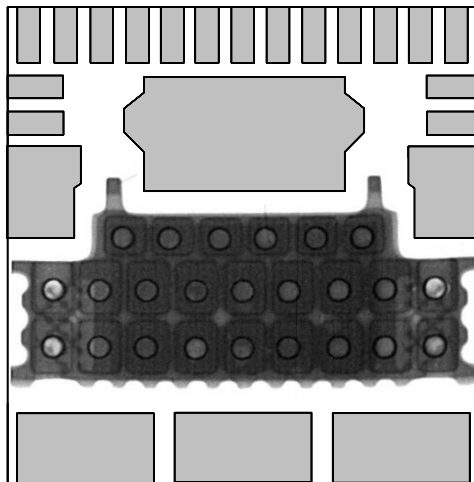


Figure 16. Typical Appearance of Assembly in X-ray

- Typical appearance of completed solder joint of the large exposed pad in cross-section. Fully wetted pads with non-wetted via area.

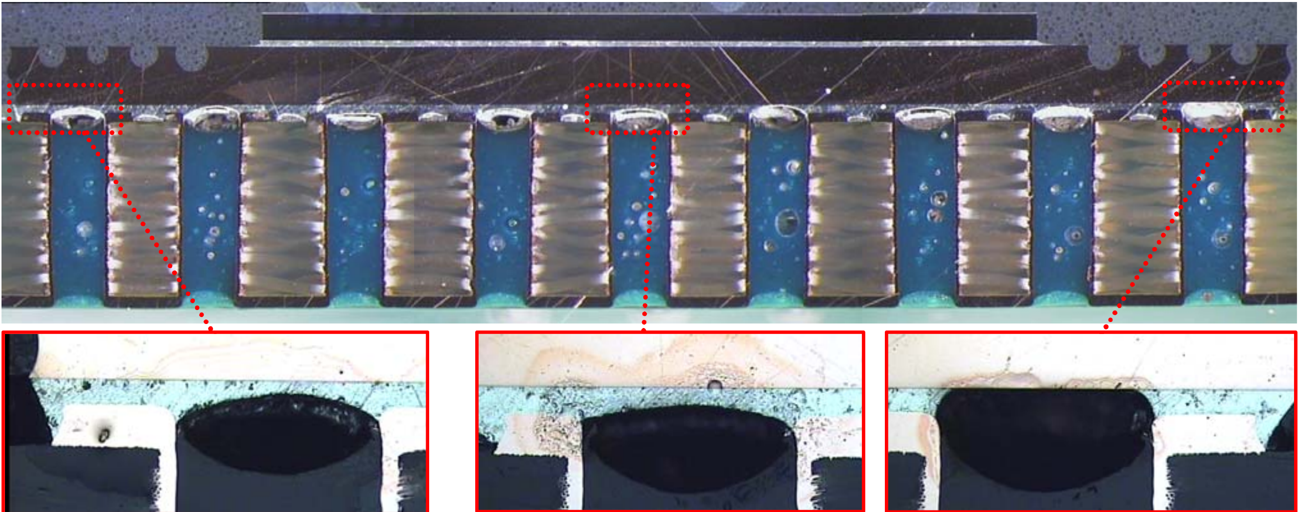


Figure 17. Typical Appearance in Cross-section

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