

# System Basis Chip (SBC) Lite with Low Speed Fault Tolerant CAN Interface

## THERMAL ADDENDUM

### Introduction

This thermal addendum is provided as a supplement to the MC33889 technical datasheet. The addendum provides thermal performance information that may be critical in the design and development of system applications. All electrical, application, and packaging information is provided in the datasheet.

### Packaging and Thermal Considerations

The MC33889 is offered in a 28 terminal SOICW, single die package. There is a single heat source (P), a single junction temperature (T<sub>J</sub>), and thermal resistance (R<sub>θJA</sub>).

$$\{ T_J \} = [ R_{\theta JA} ] \cdot \{ P \}$$

The stated values are solely for a thermal performance comparison of one package to another in a standardized environment. This methodology is not meant to and will not predict the performance of a package in an application-specific environment. Stated values were obtained by measurement and simulation according to the standards listed below.

### Standards

**Table 1. Thermal Performance Comparison**

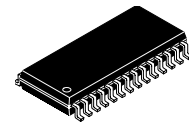
Thermal Resistance	[°C/W]
R <sub>θJA</sub> <sup>(1) (2)</sup>	42
R <sub>θJB</sub> <sup>(2) (3)</sup>	11
R <sub>θJA</sub> <sup>(1) (4)</sup>	69
R <sub>θJC</sub> <sup>(5)</sup>	23

Notes:

1. Per JEDEC JESD51-2 at natural convection, still air condition.
2. 2s2p thermal test board per JEDEC JESD51-7.
3. Per JEDEC JESD51-8, with the board temperature on the center trace near the center lead.
4. Single layer thermal test board per JEDEC JESD51-3.
5. Thermal resistance between the die junction and the package top surface; cold plate attached to the package top surface and remaining surfaces insulated.

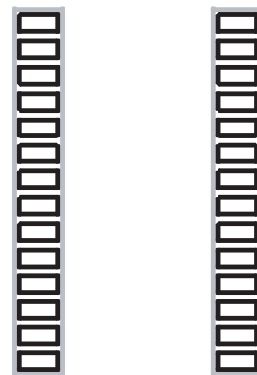
**33889DWB  
 33889EG**

**28-TERMINAL  
 SOICW**



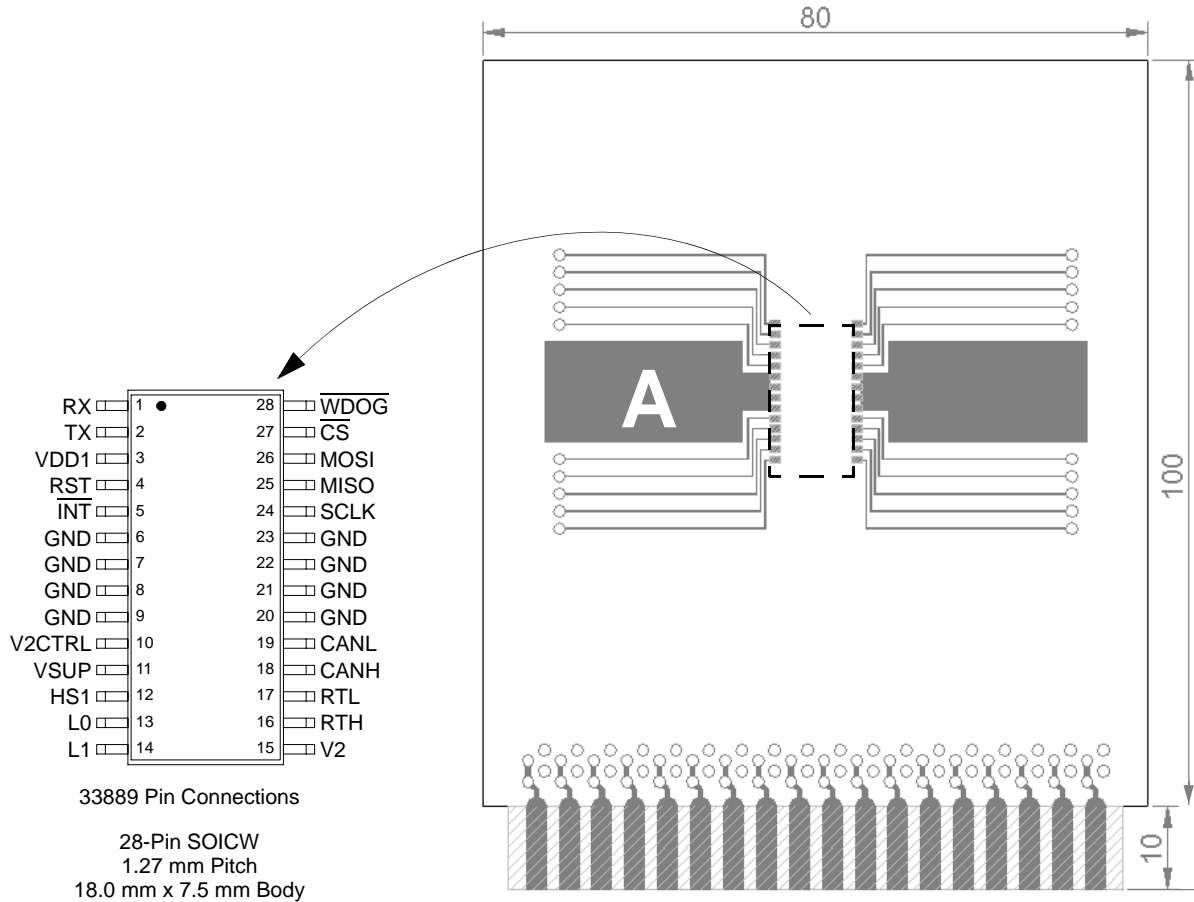
**DWB SUFFIX  
 EG SUFFIX (PB-FREE)  
 98ASB42345  
 28-TERMINAL SOICW**

**Note** For package dimensions, refer to the 33889 device datasheet.



20 Terminal SOICW  
 1.27 mm Pitch  
 18.0 mm x 7.5 mm Body

**Figure 1. Surface Mount for SOIC Wide Body non-Exposed Pad**



**Figure 2. Thermal Test Board**

**Device on Thermal Test Board**

- Material: Single layer printed circuit board  
 FR4, 1.6 mm thickness  
 Cu traces, 0.07 mm thickness
- Outline: 80 mm x 100 mm board area,  
 including edge connector for thermal testing
- Area A: Cu heat-spreading areas on board surface
- Ambient Conditions: Natural convection, still air

**Table 2. Thermal Resistance Performance**

Thermal Resistance	Area A (mm <sup>2</sup> )	(°C/W)
R <sub>θJA</sub>	0	69
	300	53
	600	48

R<sub>θJA</sub> is the thermal resistance between die junction and ambient air.

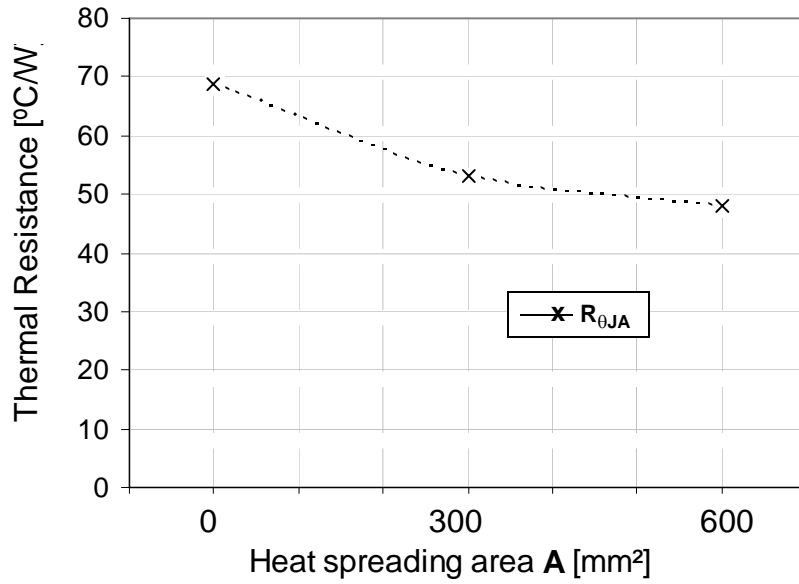


Figure 3. Device on Thermal Test Board  $R_{\theta JA}$

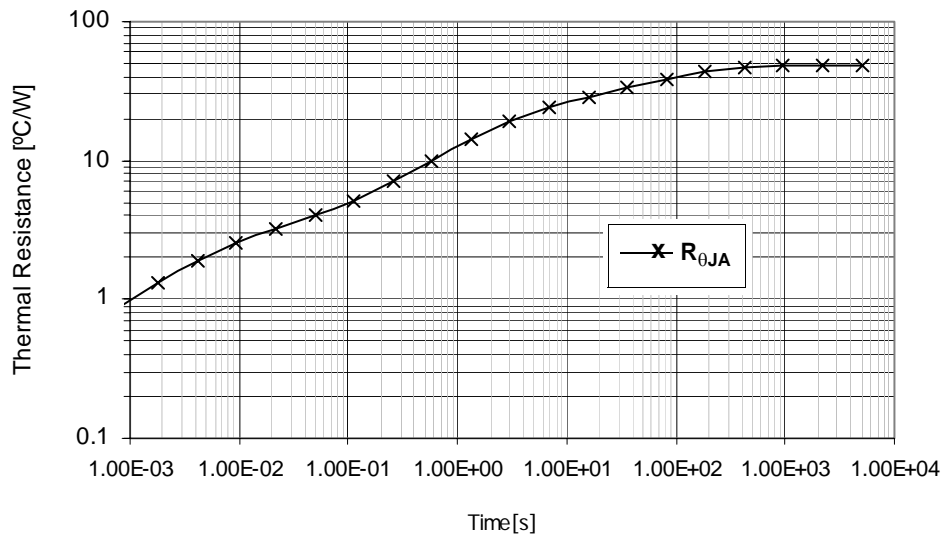


Figure 4. Transient Thermal Resistance  $R_{\theta JA}$   
 Device on Thermal Test Board Area  $A = 600$  (mm<sup>2</sup>)

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