Features

- Compatible with HDMI 1.3c
- Supports 2.25 Gbps Signaling Rate for 480i/p, 720i/p, and 1080i/p Resolutions up to 12-Bit Color Depth
- Integrated Receiver Termination
- Selectable Receiver Equalization to Accommodate to Different Input Cable Lengths
- ***Embedded EEPROM for EDID function***
- Intra-Pair Skew < 40 ps
- Inter-Pair Skew < 65 ps
- ***System Level ESD Protection Exceeds 8 kV (direct contact) for TMDS Inputs and DDC Interface***
- Supply Voltage, VCC= 3.3 V +/- 5%
- 5-V Tolerance on All Side Band Signals
- 100-pin LQFP Package
- ***Green Part*** and 260 °C reflow rated

Applications

- Digital TV
- Digital projector
- Digital Monitor
- Audio video receiver

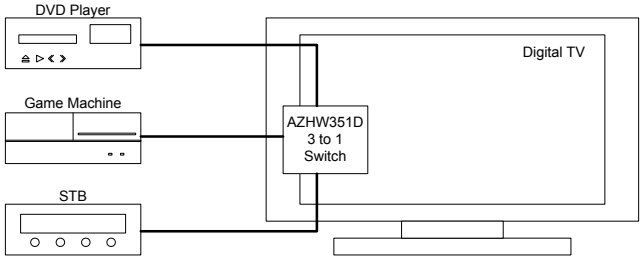
Description

The AZHW351D is a 3-port High-Definition Multimedia Interface (HDMI) or DVI switch which allows up to 3 HDMI or DVI ports to be switched to a single display terminal. Four TMDS channels, one hot plug detector, and a digital display control (DDC) interface are supported on each port. Each TMDS channel allows signaling rates up to 2.25 Gbps to allow 1080p resolution in 12-bit color depth.

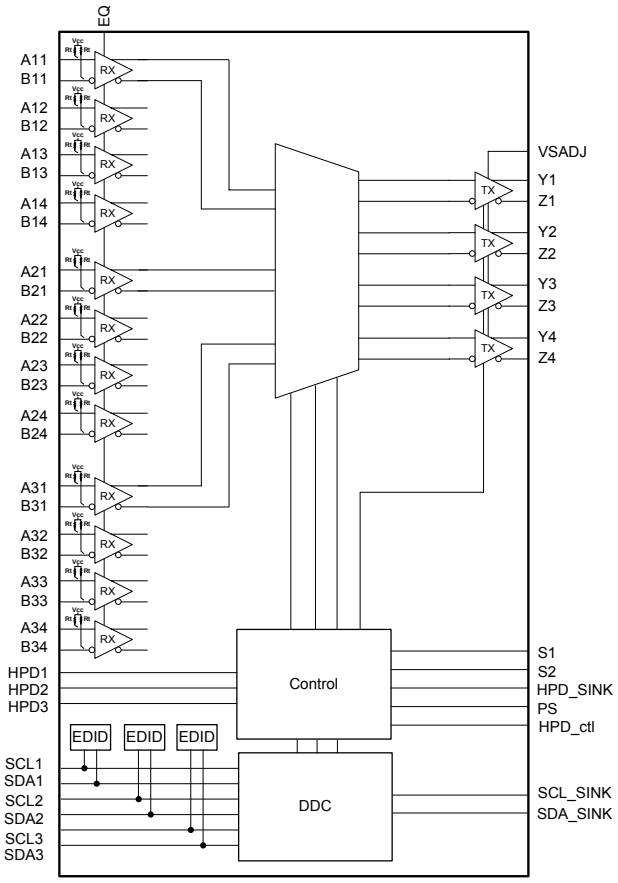
With two control pins, all input terminations can be disconnected, TMDS inputs are high impedance with standard TMDS terminations, all internal devices are turned off to disable the DDC links, and all HPD outputs are connected to the HPD_SINK. This allows the initiation of the HDMI physics address discovery process. Termination resistor (50-Ω), pulled up to VCC, are integrated at each TMDS receiver input. External terminations are not required. Moreover, the AZHW351D is the generation of devices from Amazing to integrate the Extended Display Identification Data (EDID). The EDID is stored in on-chip EEPROM (256 bytes for each port) and the memory is built-in on each port through the DDC bus.

The AZHW351D provides two levels of input equalization for different ranges of cable lengths. Each TMDS receiver owns frequency responsive equalization circuits. When EQ sets high, the receiver supports the connection in short range HDMI cables. When EQ sets low (recommended value), the receiver supports the input connection in long range HDMI cables. The AZHW351D supports two types of power saving operations. When a system is under power down mode and there is no digital audio/visual content from a connected source to minimize power consumption from TMDS inputs, outputs, and internal circuits. When a system in under standby mode, only TMDS clock inputs, outputs and termination are turned on, and the selected DDC link from the source to sink. The device is characterized for operation from 0 °C to 70 °C.

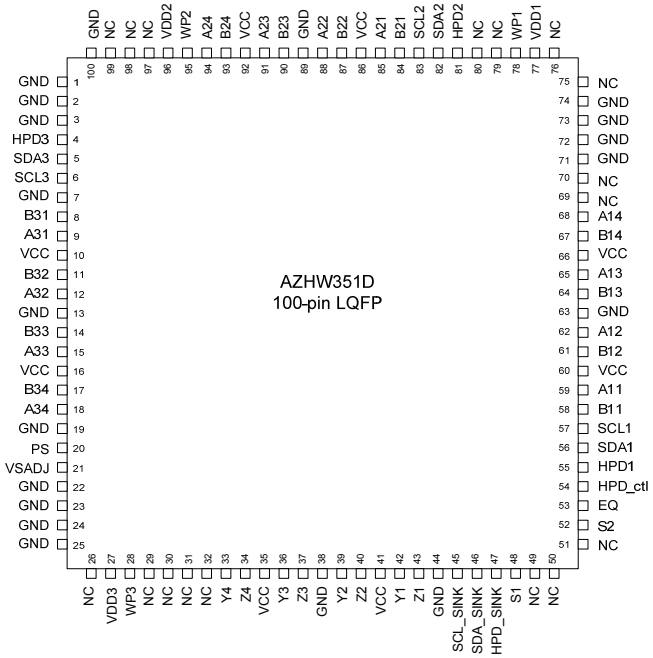
Typical application



Circuit diagram



Pin Configuration



TERMINAL FUNCTIONS

TERMINAL		I/O	Description
NAME	NO.		
A11, A12, A13, A14	59, 62, 65, 68	I	Source port 1 TMDS positive inputs
A21, A22, A23, A24	85, 88, 91, 94	I	Source port 2 TMDS positive inputs
A31, A32, A33, A34	9, 12, 15, 18	I	Source port 3 TMDS positive inputs
B11, B12, B13, B14	58, 61, 64, 67	I	Source port 1 TMDS negative inputs
B21, B22, B23, B24	84, 87, 90, 93	I	Source port 2 TMDS negative inputs
B31, B32, B33, B34	8, 11, 14, 17	I	Source port 3 TMDS negative inputs
GND	1, 2, 3, 7, 13, 19, 22, 23, 24, 25, 38, 44, 63, 71, 72, 73, 74, 89, 100	---	Ground
EQ	53	I	TMDS input equalization selector EQ= high---HDMI 1.3 compliant cable EQ= low---10m 28 AWG HDMI cable
PS	20	I	Power saving selector PS= high---standby mode PS= low---normal mode
HPD_ctl	54	I	HPD output selector HPD_ctl= high---all HPD output follows HPD_SINK HPD_ctl=low---only selected HPD output follows HPD_SINK
HPD1	55	O	Source port 1 hot plug detector output
HPD2	81	O	Source port 2 hot plug detector output
HPD3	4	O	Source port 3 hot plug detector output
HPD_SINK	47	I	Sink port hot plug detector input
SCL1	57	I/O	Source port 1 DDC I^2C clock line
SCL2	83	I/O	Source port 2 DDC I^2C clock line
SCL3	6	I/O	Source port 3 DDC I^2C clock line
SCL_SINK	45	I/O	Sink port DDC I2C clock line
SDA1	56	I/O	Source port 1 DDC I^2C data line
SDA2	82	I/O	Source port 2 DDC I^2C data line
SDA3	5	I/O	Source port 3 DDC I^2C data line

SDA_SINK	46	I/O	Sink port DDC I^2C data line
S1, S2,	48, 52	I	Source selector
VCC	10, 16, 35, 41, 60, 66, 86, 92	---	Power supply
V_{SADJ}	21	I	TMDS compliant voltage swing control
VDD1	77	---	Power supply for port 1 EEPROM
VDD2	96	---	Power supply for port 2 EEPROM
VDD3	27	---	Power supply for port 3 EEPROM
WP1	78	I	Write protection for port 1 EEPROM
WP2	95	I	Write protection for port 2 EEPROM
WP3	28	I	Write protection for port 3 EEPROM
Y1, Y2, Y3, Y4	42, 39, 36, 33	O	Sink port TMDS positive outputs
Z1, Z2, Z3, Z4	43, 40, 37, 34	O	Sink port TMDS negative outputs

Table-1-1: Source Selection Lookup (Normal operation)

CONTROL PINS				I/O SELECTED		HOT PLUG DETECT STATUS		
S1	**S2**	**PS**	**HPD_ctl**	**Y/Z**	**SCL_sink SDA_sink**	**HPD1**	**HPD2**	**HPD3**
H	H	L	L	**A1/B1** Terminations of A2/B2 and A3/B3 are disconnected	SCL1 SDA1	HPD_SINK	L	L
L	H	L	L	**A2/B2** Terminations of A1/B1 and A3/B3 are disconnected	SCL2 SDA2	L	HPD_SINK	L
L	L	L	L	**A3/B3** Terminations of A1/B1 and A2/B2 are disconnected	SCL3 SDA3	L	L	HPD_SINK

Note. **H: logic high; L: logic low;**

Table-1-2: Source Selection Lookup (Normal operation)

CONTROL PINS				I/O SELECTED		HOT PLUG DETECT STATUS		
S1	**S2**	**PS**	**HPD_ctl**	**Y/Z**	**SCL_sink SDA_sink**	**HPD1**	**HPD2**	**HPD3**
H	H	L	H	**A1/B1** Terminations of A2/B2 and A3/B3 are disconnected	SCL1 SDA1	HPD_SINK	HPD_SINK	HPD_SINK
L	H	L	H	**A2/B2** Terminations of A1/B1 and A3/B3 are disconnected	SCL2 SDA2	HPD_SINK	HPD_SINK	HPD_SINK
L	L	L	H	**A3/B3** Terminations of A1/B1 and A2/B2 are disconnected	SCL3 SDA3	HPD_SINK	HPD_SINK	HPD_SINK

Note. **H: logic high; L: logic low;**

Table-1-3: Source Selection Lookup (Standby mode)

CONTROL PINS				I/O SELECTED		HOT PLUG DETECT STATUS		
S1	**S2**	**PS**	**HPD_ctl**	**Y/Z**	**SCL_sink SDA_sink**	**HPD1**	**HPD2**	**HPD3**
H	H	H	L	**A11/B11** Terminations of others are disconnected	SCL1 SDA1	HPD_SINK	L	L
L	H	H	L	**A21/B21** Terminations of others are disconnected	SCL2 SDA2	L	HPD_SINK	L
L	L	H	L	**A31/B31** Terminations of others are disconnected	SCL3 SDA3	L	L	HPD_SINK

Note. **H: logic high; L: logic low;**

Table-1-4: Source Selection Lookup (Standby mode)

CONTROL PINS				I/O SELECTED		HOT PLUG DETECT STATUS		
S1	**S2**	**PS**	**HPD_ctl**	**Y/Z**	**SCL_sink SDA_sink**	**HPD1**	**HPD2**	**HPD3**
H	H	H	H	**A11/B11** Terminations of others are disconnected	SCL1 SDA1	HPD_SINK	HPD_SINK	HPD_SINK
L	H	H	H	**A21/B21** Terminations of others are disconnected	SCL2 SDA2	HPD_SINK	HPD_SINK	HPD_SINK
L	L	H	H	**A31/B31** Terminations of others are disconnected	SCL3 SDA3	HPD_SINK	HPD_SINK	HPD_SINK

Table-1-5: Source Selection Lookup (Power down mode)

CONTROL PINS				I/O SELECTED		HOT PLUG DETECT STATUS		
S1	**S2**	**PS**	**HPD_ctl**	**Y/Z**	**SCL_sink SDA_sink**	**HPD1**	**HPD2**	**HPD3**
H	L	L	H	**All** Terminations are disconnected	Are pulled high by external pull-up termination	HPD_SINK	HPD_SINK	HPD_SINK

Note. **H: logic high; L: logic low;**

ABSOLUTE MAXIMUM RATINGS

			UNIT
Supply voltage range	VCC		-0.5V to 4V
Supply voltage range	VDDn		-0.5V to 5.5V
Voltage range	Anm, Bnm		2.5V to 4V
	Ym, Zm, VSADJ, EQ, HPDn, PS, HPD_ctl		-0.5V to 4V
	SCLn, SCL_SINK, SDAn, SDA_SINK, HPD_SINK, S1, S2, WPn,		-0.5V to 5.5V
Electrostatic discharge	System level (direct contact) (1)	Anm, Bnm, SCLn, SDAn, HPDn,	+/-8 KV
	Human body model (2)	Anm, Bnm, SCLn, SDAn, HPDn	+/- 8 KV
		All pins	+/- 4 KV
	Machine model (2)	All pins	+/- 200V
	Charged-device model (2)	All pins	+/- 1000V

*(1) System level: tested in accordance with IEC61000-4-2

*(2) Tested in accordance with JEDEC Standard 22

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
VCC Supply voltage	3.135	3.3	3.465	V
VDD Supply voltage	4.5	5	5.5	V
T_A Operating free-air temperature	0	25	70	°C
TMDS differential pins				
V_{IC} Input common mode voltage	VCC-0.4		VCC+0.01	V
V_{ID} Receiver peak-to-peak differential input voltage	150		1560	mV_{P-P}
R_{VSADJ} Resistor for TMDS compliant voltage swing range		6.2k		Ω
AV_{CC} TMDS output termination voltage		3.3		V
R_T Termination resistance	45	50	55	Ω
Signaling rate	0		2.25	Gbps
Control pins (EQ, PS, HPD_ctl)				
V_{IH} LVTTL High-level input voltage	2		Vcc	V
V_{IL} LVTTL Low-level input voltage	GND		0.8	V
DDC I/O pins				
$V_{I(DDC)}$ DDC input voltage	GND		5.5	V
Status and source selector pins (S1, S2, S3, HPD_SINK)				
V_{IH} LVTTL High-level input voltage	2.5		5.5	V
V_{IL} LVTTL Low-level input voltage	GND		0.8	V
V_{IM} Middle state input voltage	1.6		2.0	V

Electrical Characteristics
Over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP (1)	MAX	UNIT
I_{CC} Supply current	R_T = 50 Ω VCC = 3.3V AV_{CC} = 3.3V Data pattern = 2.25 Gbps Clock = 225 MHz	S1/S2= L/L L/H H/H		225		mA
		S1/S2= H/L		6	14	mA
		S1/S2= L/L L/H H/H (PS=H)		70	150	mA
TMDS DIFFERENTIAL PINS (A/B; Y/Z)						
V_{OH} Single-ended high-level output Voltage	R_T = 50 Ω VCC = 3.3V AV_{CC} = 3.3V		AVCC -10	AV_{CC}	AVCC +10	mV
V_{OL} Single-ended low-level output voltage			AVCC -700	AV_{CC} -560	AVCC - 400	mV
V_{swing} Single-ended output swing voltage			400	560	700	mV
$I_{(os)}$ Short circuit output current				11.5	14	mA
R_{INT} Input termination resistance	V_{IN} = 2.9 V		45	50	55	Ω

Electrical Characteristics (continued)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DDC I/O PINS					
C_{IO} Input/output Capacitance	$V_{I(PP)}$ = 1V, 100 kHz		6		pF
R_{ON} Switch resistance	I_O = 3 mA, V_O = 0.4 V		80	150	Ω
V_{PASS} Switch output voltage	V_I = 3.3V, I_O=100 μA	1.5	2.0	2.5	V
STATUS AND SOURCE SELECTOR PINS					
V_{IH} TTL High-level input voltage		2.5		5.5	V
V_{IL} TTL Low-level input voltage		GND		0.8	V

- **(1) All typical values are at 25 °C and with a 3.3-V VCC supply.**

SWITCHING CHARACTERISTICS

Over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
TMDS DIFFERENTIAL PINS (Y/Z)					
t_{PLH} Propagation delay time, low-to-high-level output	R_T = 50 Ω AV_{CC} = 3.3V Am/Bm (1) = 225 MHz clock Am/Bm (2:4) = 2.25 Gbps pattern		1200	1500	ps
t_{PHL} Propagation delay time, high-to-low-level output			1200	1500	ps
t_r Differential output signal rise time		75		240	ps
t_f Differential output signal fall time		75		240	ps
$t_{sk(p)}$ Pulse skew (t_{PHL}-t_{PLH})			10	50	ps
$t_{sk(D)}$ Intra-pair differential skew			20	40	ps
$t_{sk(0)}$ Inter-pair differential skew			18	65	ps
$t_{jt(PP)}$ Peak-to-peak output jitter(Y1/Z1)			40	50	ps
$t_{jt(PP)}$ Peak-to-peak output jitter (Y2/Z2; Y3/Z3;Y4/Z4)			75	120	ps
t_{sx} Select to switch output			25	60	ns

***(1) All typical values are at 25℃ and with a 3.3-V VCC supply.**

EEPROM Features

- Operation Voltage VDD: 2.2V to 5.5V
- 2-wire Serial Interface
- Schmitt Trigger, Filtered Inputs for Noise Suppression
- Bi-directional Data Transfer Protocol
- 100 kHz(2.2V) and 400 kHz(5V) Compatibility
- Write Protect Pin for Hardware Data Protection
- 8-byte Page Write Modes
- Partial Page Writes are Allowed
- Self-timed Write Cycle (5 ms max)
- High-reliability
  -Endurance: 1,000,000 Write Cycles
  -Data Retention: 100 Years

Absolute Maximum Ratings for EEPROM

Operating Temperature (Plastic Package)	-55℃ to +125℃
Storage Temperature (Plastic Package)	-65℃ to +150℃
Voltage on VDDn and WPn Pins with Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Description

The AZHW351D provides 2048 bits of serial electrically erasable and programmable read-only memory (EEPROM) organized as 256 words of 8 bits each. The device is optimized for use in industrial and commercial applications where low-power and low-voltage operations are essential.

Other Description

SERIAL CLOCK (SCL): The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

SERIAL DATA (SDA): The SDA pin is bi-directional for serial data transfer.

DEVICE/PAGE ADDRESSES (A0): The A0 is device address for EDID function that is hard wired for the EEPROM.

Memory Organization

2K Serial EEPROM: Internally organized with 32 pages of 8 bytes each, the 2K requires an 8-bit data word address for random word addressing.

WRITE PROTECT (WP): The Write Protect pin provides hardware data protection. The Write Protect pin allows normal read/write operations when connected to ground (GND). When the Write Protect pin is connected to V_{DD}, the write protection feature is enabled.

Write Protect Description

WP Pin Status	Part of the Array Protected
WP= V_{DD}	Full (2K) Array
WP=GND	Normal Read/Write Operations

Capacitance

Applicable over recommended operating range from: T_A=25℃, f=1.0 MHz, V_{DD}=+2.2V.

Symbol	Test Condition	Max	Units	Conditions
$C_{I/O}$[1]	Input/Output Capacitance (SDA)	15	pF	$V_{I/O}$=0V
C_{IN}[1]	Input Capacitance (SCL)	14	pF	V_{IN}=0V

Note: 1. This parameter is characterized and is not 100% tested.

DC Characteristics

Applicable over recommended operating range from: T_A=-40℃ to +85℃, V_{DD}=+2.2V to +5.5V, (unless otherwise noted).

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
V_{DD}	Supply Voltage		2.2		5.5	V
I_{DD1}	Supply Current	V_{DD}=5.0V, Read at 100K		0.4	1.0	mA
I_{DD2}	Supply Current	V_{DD}=5.0V, Write at 100K		2.0	3.0	mA
I_{SB1}	Standby Current	V_{DD}=2.2V, V_{IN}= V_{DD}/ V_{ss}			1.0	μA
I_{SB2}	Standby Current	V_{DD}=5.0V, V_{IN}= V_{DD}/ V_{ss}			6.0	μA
I_{LI}	Input Leakage Current	V_{IN}= V_{DD}/ V_{ss}		0.10	3.0	μA
I_{LO}	Output Leakage Current	V_{OUT}= V_{DD}/ V_{ss}		0.05	3.0	μA
V_{IL}[1]	Input Low Level		-0.6		V_{DD}×0.3	V
V_{IH}[1]	Input High Level		V_{DD}×0.7		V_{DD}+0.5	V
V_{OL}	Output Low Level	V_{DD}=2.7V, I_{OL}=2.1 mA			0.4	V

AC Characteristics (As shown in Fig. 1. and Fig. 2.)

Applicable over recommended operating range from: T_A=-40℃ to +85℃, V_{DD}=+2.2V to +5.5V CL=1 TTL Gate and 100pF (unless otherwise noted). Test conditions are listed in Note 2.

Symbol	Parameter	2.2-volt		5.0-volt		Units
		Min	Max	Min	Max	
f_{SCL}	Clock Frequency, SCL		100		400	kHz
t_{LOW}	Clock Pulse Width Low	4.7		1.2		μs
t_{HIGH}	Clock Pulse Width High	4.0		0.6		μs
t_{AA}	Clock Low to Data Out Valid	0.1	4.5	0.1	0.9	μs
t_{BUF}[1]	Time the bus must be free before a new transmission can Start	4.7		1.2		μs
$t_{HD.STA}$	Start Hold Time	4.0		0.6		μs
$t_{SU.STA}$	Start Setup Time	4.7		0.6		μs
$t_{HD.STA}$	Data In Hold Time	0		0		μs

$t_{SU.DAT}$	Data In Setup Time	200		100		ns
t_R	Inputs Rise Time		1.0		0.3	μs
t_F	Inputs Fall Time		300		300	ns
$t_{SU.STO}$	Stop Setup Time	4.7		0.6		μs
t_{DH}	Data Out Hold Time	100		50		ns
t_{WR}	Write Cycle Time		5		5	ms
Endurance[1]	5.0V, 25℃, Page Mode	1,000,000				Write Cycles

Notes: 1. This parameter is characterized and is not 100% tested.

2. AC measurement conditions:

RL (connects to V_{DD}): 1.3kΩ. Input and output timing reference voltages: 0.5 V_{DD}

Input pulse voltages: 0.3 V_{DD} to 0.7 $V_{DD.}$ Input rise and fall times:≤50ns

Device Operation

CLOCK and DATA TRANSITIONS: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (refer to Figure 3). Data changes during SCL high periods will indicate a start or stop condition as defined below.

START CONDITION: A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (refer to Figure 4).

STOP CONDITION: A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the EEPROM in a standby power mode (refer to Figure 4).

All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a zero to acknowledge that it has received each word. This happens during the ninth clock cycle. Following receipt each word from the EEPROM, the microcontroller should send a zero to EEPROM and continue to output the next data word or send a stop condition to finish the read cycle (refer to Figure 5).

STANDBY MODE: The EEPROM features a low-power standby mode which is enabled: (a) upon power-up and (b) after the receipt of the stop bit and the completion of any internal operations.

DEVICE RESET: After an interruption in protocol, power loss or system reset, any 2-wire part can be protocol reset by following these steps:

1. Clock up to 9 cycles.
2. Look for SDA high in each cycle while SCL is high.
3. Create a start condition.

Device Addressing

The 2K EEPROM device requires an 8-bit device address word following a start condition to enable the chip for a read or write operation.

The device address word consists of a mandatory one, zero sequence for the first four most significant bits as shown. This is common to all the EEPROM devices.

The next 3 bits are the 0, 0 and 0 device address bits for the EEPROM. These 3 bits must compare to their corresponding hard-wired input pins.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low (refer to Figure 6).

Upon a compare of the device address, the EEPROM will output a zero. If a compare is not made, the chip will return to a standby state.

Write Operations

BYTE WRITE: A write operation requires an 8-bit data word address following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a zero and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a zero and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time

the EEPROM enters an internally timed write cycle, $t_{WR,}$ to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete (refer to Figure 7).

PAGE WRITE: The 2K EEPROM is capable of an 8-byte page write.

A page write is initiated the same as a byte write, but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to seven data words. The EEPROM will respond with a zero after each data word received. The microcontroller must terminate the page write sequence with a stop condition (refer to Figure 8).

The data word address lower three bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than eight data words are transmitted to the EEPROM, the data word address will "roll over" and previous data will be overwritten.

ACKNOWLEDGE POLLING: Once the internally timed write cycle has started and the EEPROM inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a zero allowing the read or write sequence to continue.

Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to one . There are three read operations: current address read, random address read and sequential read.

CURRENT ADDRESS READ: The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address "roll over" during read is from the last byte of the last memory page to the first byte of the first page. The address "roll over" during write is from the last byte of the current page to the first byte of the same page.

Once the device address with the read/write select bit set to one is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller does not respond with an input zero but does generate a following stop condition (refer to Figure 9).

RANDOM READ: A random read requires a "dummy" byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another start condition. The microcontroller now initiates a

current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a zero but does generate a following stop condition (refer to Figure 10).

SEQUENTIAL READ: Sequential reads are initiated by either a current address read or a random address read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the EEPROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will "roll over" and the sequential read will continue. The sequential read operation is terminated when the microcontroller does not respond with a zero but does generate a following stop condition (refer to Figure 11).

Fig.1. Bus Timing Definition

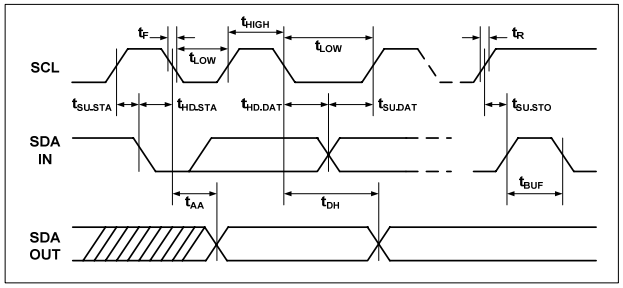
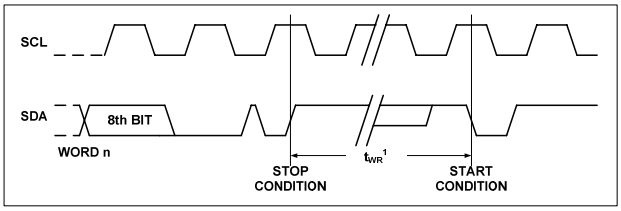


Fig. 2. SCL: Serial Clock, SDA: Serial Data I/O



Note: 1. The write cycle time t_{WR} is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.

Fig. 3. Data Validity

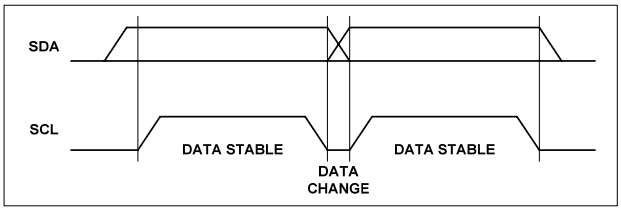


Fig. 4. Start and Stop Definition

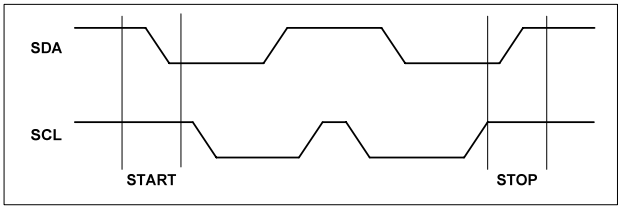


Fig. 5. Output Acknowledge

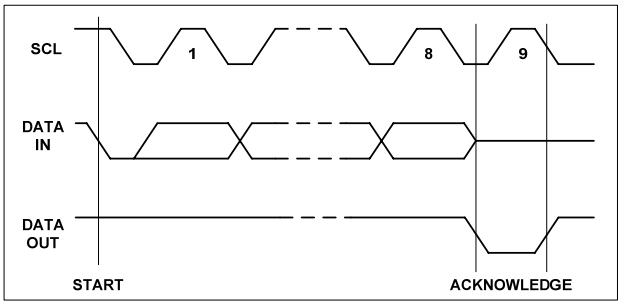


Fig. 6. Device Address

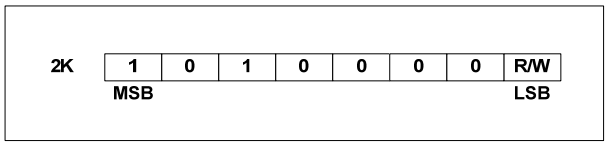


Fig. 7. Byte Write

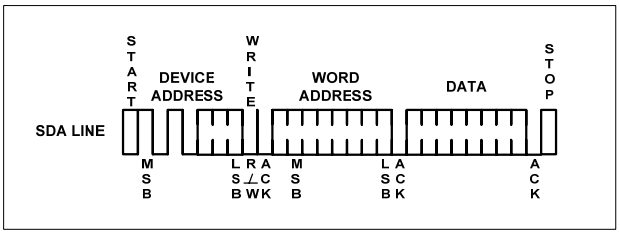


Fig. 8. Page Write

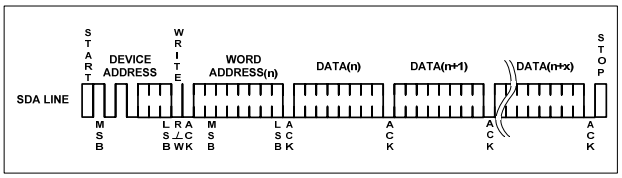


Fig. 9. Current Address Read

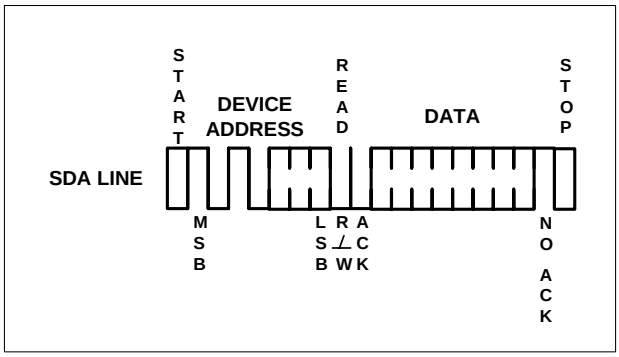


Fig. 10. Random Read

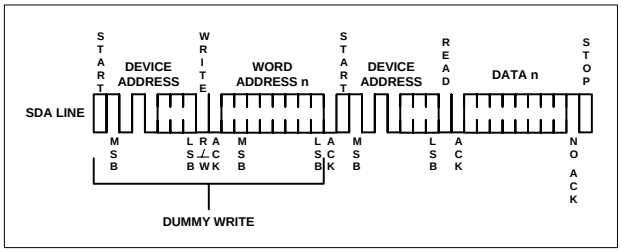
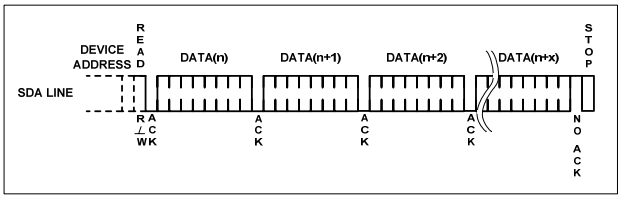


Fig. 11. Sequential Read

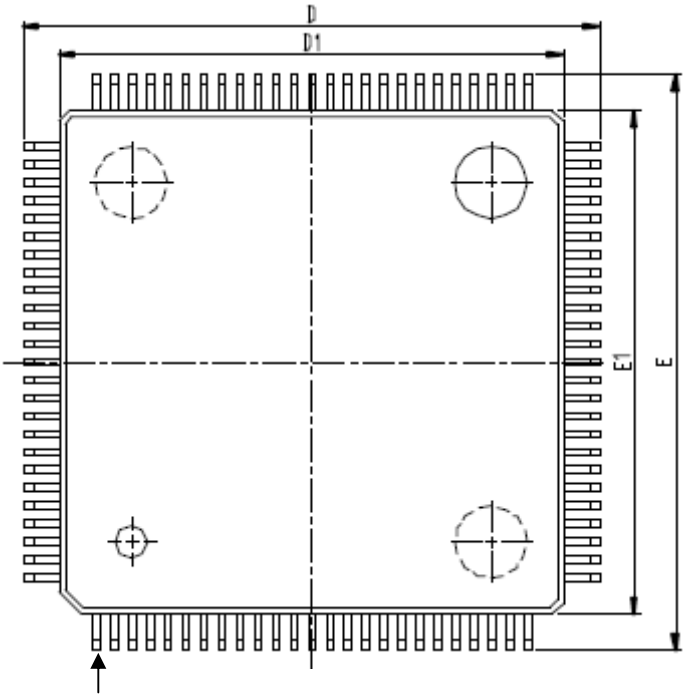


Mechanical Details

100-pin LQFP

PACKAGE DIAGRAMS

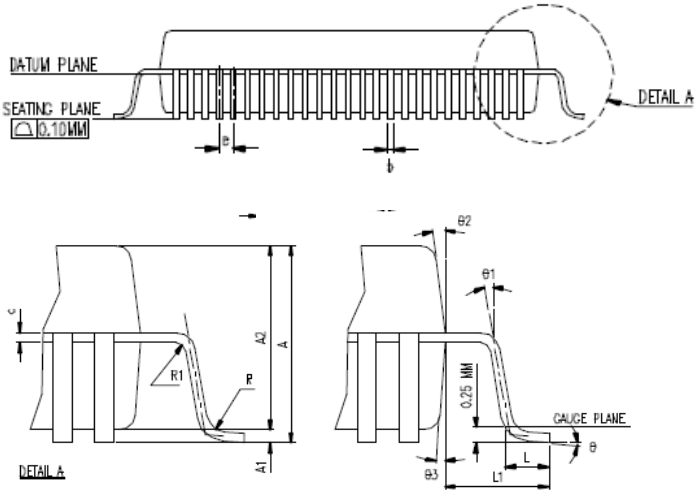
TOP VIEW



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN	NOM	MAX
A			1.60			0.063
A1	0.05		0.15	0.001		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.20	0.23	0.007	0.008	0.009
c	0.09		0.16	0.004		0.006
e	0.50 BASIC			0.020 BASIC		
D	16.00 BASIC			0.630 BASIC		
D1	14.00 BASIC			0.551 BASIC		
E	16.00 BASIC			0.630 BASIC		
E1	14.00 BASIC			0.551 BASIC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF.			0.039 REF.		
R1	0.08			0.003		
R	0.08		0.20	0.003		0.008
θ	0	3.5	7	0	3.5	7
θ1	0			0		
θ2	11	12	13	11	12	13
θ3	11	12	13	11	12	13
JEDEC	MS-026 (BED)					

⚠ *NOTES : DIMENSIONS " D1 " AND " E1 " DO NOT INCLUDE MOLD PROTRUSION ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE " D1 AND " E1 " ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD

SIDE VIEW



Marking Code

Part Number	Marking Code
AZHW351D	AZHW351D
AZHW351D	AZHW351D

Revision History

Revision	Modification Description
Revision 2009/02/07	Preliminary Release.
Revision 2009/04/27	Formal version initial release