Features

- Compatible with HDMI 1.3c
- Supports 2.5 Gbps signaling rate for 480i/p, 720i/p, and 1080i/p resolutions up to 12-bit color depth
- Integrated receiver termination
- Adaptive receiver equalization to accommodate to different input cable lengths
- DDC buffer link
- CEC buffer link
- ***Embedded memory for EDID function***
- Intra-pair skew < 40 ps
- Inter-pair skew < 65 ps
- ***System Level ESD Protection Exceeds 6 kV (direct contact) for TMDS Inputs and DDC Interface***
- Supply voltage, VCC= 3.3 V +/- 5%
- Controllable shutdown and standby modes for power saving
- Controllable logic states for HPD output
- 5-V tolerance on all side band signals
- 64-pin LQFP package
- ***Green part*** and 260 ^{o}C reflow rated

Applications

- Digital TV
- Digital projector
- Digital monitor
- Audio/video receiver

Description

The AZHW271D is a 2-port High-Definition Multimedia Interface (HDMI) or DVI switch which allows up to 2 HDMI or DVI ports to be switched to a single display terminal. Four TMDS channels, one hot plug detector, and a digital display control (DDC) interface are supported on each port. Each TMDS channel allows signaling rates up to 2.5 Gbps to allow 1080p resolution in 12-bit color depth.

With two control pins, the AZHW271D can be operated at the shutdown mode. At this condition, all TMDS input terminations are disconnected and at the state of high impedance. Moreover, the DDC links are disabled due to that all internal devices are turned off and all HPD outputs are connected to the HPD_SINK. This allows the initiation of the HDMI physics address discovery process. Termination resistor (50-Ω), pulled up to VCC, are integrated at each TMDS receiver input. External terminations are not required as shown in Fig.1. Moreover, the AZHW271D is the generation of the devices from Amazing

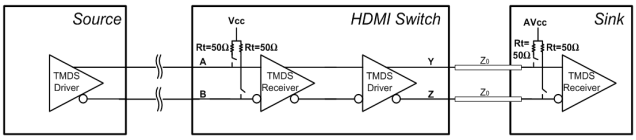


Fig.1. TMDS internal termination

to integrate the Extended Display Identification Data (EDID). The EDID is stored in on-chip memory (256 bytes) and it is built-in on each port through the DDC bus.

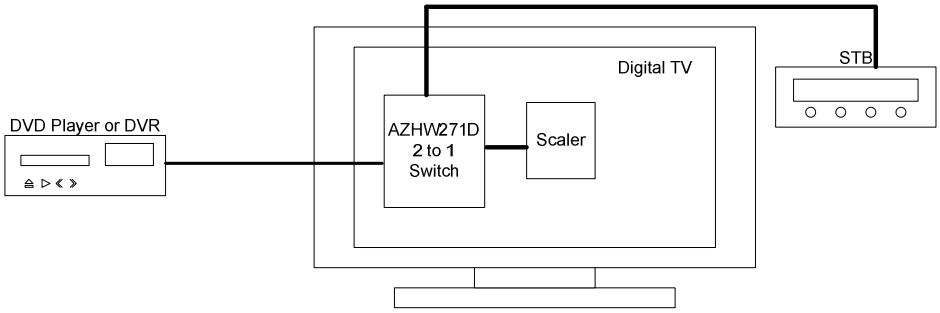
The AZHW271D provides adaptive input equalization for different ranges of cable lengths. Each TMDS receiver owns frequency responsive equalization circuits. A 0-ohm (recommended value) calibration resistor is tied to GND for EQ pin, the receiver with optimized equalization supports the connection in different range HDMI cables. Moreover, A 0-ohm (recommended value) calibration resistor is tied to GND for RP1 (pin 9) pin, the receiver of port 1 and

port 2 with adaptive equalization supports the input connection in different range HDMI cables. Also, A 100k-ohm (recommended value) calibration resistor is tied to GND for RP2 (pin 3) pin, the receiver of port 1 and port 2 with adaptive equalization supports the input connection in different range HDMI cables. The AZHW271D supports two types of power saving operations. When a system is under shutdown mode and there is no digital audio/visual content from a connected source to minimize power consumption from TMDS inputs, outputs, and internal circuits. When a system is under standby mode (PS at logic high), only TMDS clock inputs, outputs and termination are turned on, and the selected DDC repeater link from the source to sink. At this state, the system can be quick recovery as the digital audio/visual content from a connected source. Otherwise, to filter supply noise, all VCC pins are recommended to have a 0.01 uF capacitor tied from each VCC pin to ground directly. For the ESD protection function, the AZHW271D is designed to withstand the ESD level (IEC61000-4-2) to contact mode 6 kV. For the requirements of application, a higher protection level is needed. The AZHW271D can provide TMDS pairs, DDC, and HPD pins' ESD levels (IEC61000-4-2) to contact mode 6 kV. And external ESD components are not required for the criteria of ESD contact mode 6 kV.

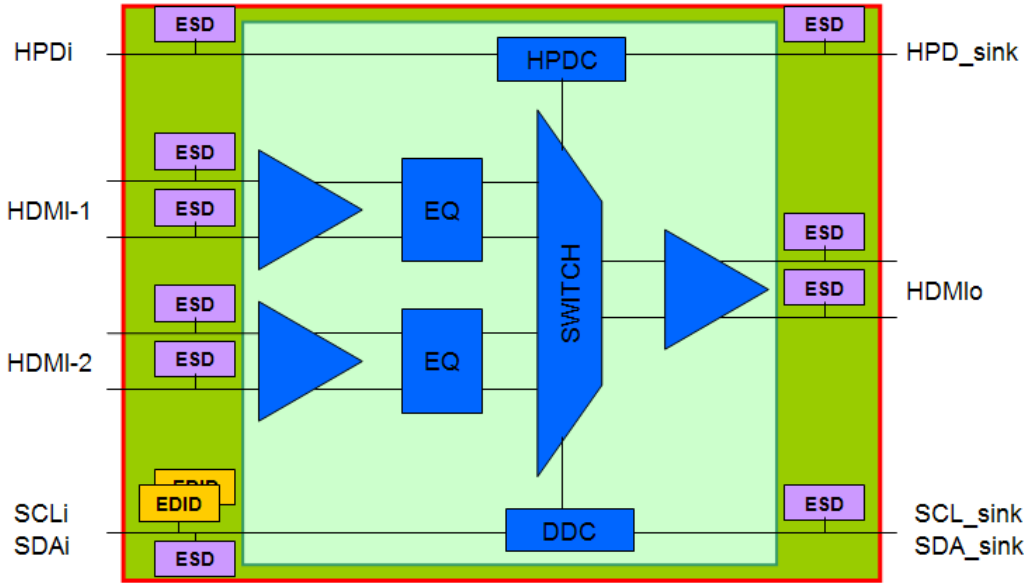
Furthermore, the AZHW271D also provides controllable states of HPD outputs. When HPD_ctl set high, all HPD outputs can follow HPD_SINK. For the VSADJ pin, it is recommended to be tied a 6.2-kΩ resistor (10% precision) to control the output swing to the HDMI compliance test.

Finally, the AZHW271D also integrates an HDMI compliant I/O to enable Consumer Electronics Control (CEC) in a DTV. The CEC I/O meets all HDMI compliance test and eliminates the need for additional external components. The device is characterized for operation from 0 ^{o}C to 70 ^{o}C.

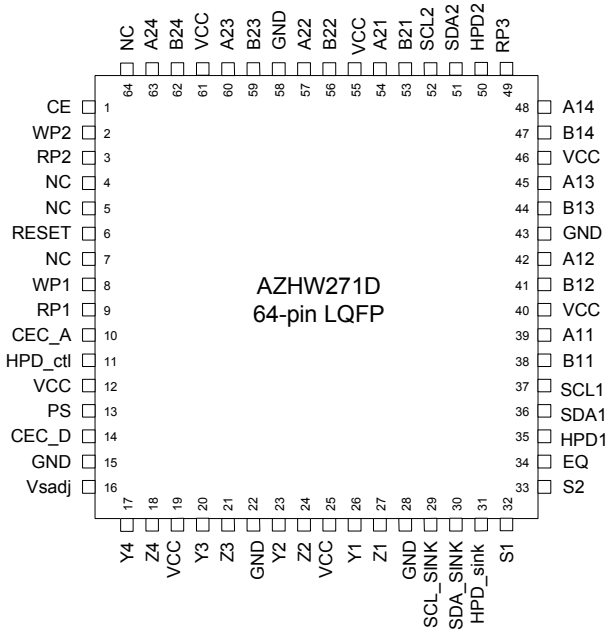
Typical application



Circuit diagram



Pin Configuration



TERMINAL FUNCTIONS

TERMINAL		I/O	Description
NAME	NO.		
A11, A12, A13, A14	39, 42, 45, 48	I	Source port 1 TMDS positive inputs
A21, A22, A23, A24	54, 57, 60, 63	I	Source port 2 TMDS positive inputs
B11, B12, B13, B14	38, 41, 44, 47	I	Source port 1 TMDS negative inputs
B21, B22, B23, B24	53, 56, 59, 62	I	Source port 2 TMDS negative inputs
GND	15, 22, 28, 43, 58	---	Ground
EQ	34	I	TMDS input equalization calibration
PS	13	I	Power saving selector PS= high---standby mode PS= low---normal mode
HPD_ctl	11	I	HPD output selector HPD_ctl= high---all HPD output follows HPD_SINK HPD_ctl=low---only selected HPD output follows HPD_SINK
HPD1	35	O	Source port 1 hot plug detector output
HPD2	50	O	Source port 2 hot plug detector output
HPD_SINK	31	I	Sink port hot plug detector input
SCL1	37	I/O	Source port 1 DDC I^2C clock line
SCL2	52	I/O	Source port 2 DDC I^2C clock line
SCL_SINK	29	I/O	Sink port DDC I2C clock line
SDA1	36	I/O	Source port 1 DDC I^2C data line
SDA2	51	I/O	Source port 2 DDC I^2C data line
SDA_SINK	30	I/O	Sink port DDC I^2C data line
S1, S2	32,33	I	Source selector
VCC	12, 19, 25, 40, 46, 55, 61	---	Power supply
Vsadj	16	I	TMDS compliant voltage swing control
CEC_A	10	I/O	Source port 1,2,3,4 CEC line
CEC_D	14	I/O	Sink port CEC line

TERMINAL		I/O	Description
NAME	NO.		
Y1, Y2, Y3, Y4	26, 23, 20, 17	O	Sink port TMDS positive outputs
Z1, Z2, Z3, Z4	27, 24, 21, 18	O	Sink port TMDS negative outputs
RP1	9	---	Calibration resistor
RP2	3	---	Calibration resistor
RP3	49	---	TMDS input equalization calibration
WP1	8	I	Write protection for port 1 EDID memory
WP2	2	I	Write protection for port 2 EDID memory
CE	1	---	Capacitor for memory enable function
RESET	6	---	Capacitor for memory reset function
NC	4, 5, 7, 64	---	NC pins

Table-1-1: Source Selection Lookup (Normal operation)

CONTROL PINS				I/O SELECTED		HOT PLUG DETECT STATUS	
S1	**S2**	**PS**	**HPD_ctl**	**Y/Z**	**SCL_sink SDA_sink**	**HPD1**	**HPD2**
H	H	L	L	**A1/B1 50Ω Terminations are connected** A2/B2 50Ω Terminations are disconnected	SCL1 SDA1	HPD_SINK	L
L	H	L	L	**A2/B2 50Ω Terminations are connected** A1/B1 50Ω Terminations are disconnected	SCL2 SDA2	L	HPD_SINK

Note. **H: logic high; L: logic low.**

Table-1-2: Source Selection Lookup (Normal operation)

CONTROL PINS				I/O SELECTED		HOT PLUG DETECT STATUS	
S1	**S2**	**PS**	**HPD_ctl**	**Y/Z**	**SCL_sink SDA_sink**	**HPD1**	**HPD2**
H	H	L	H	**A1/B1 50Ω Terminations are connected** A2/B2 50Ω Terminations are disconnected	SCL1 SDA1	HPD_SINK	HPD_SINK
L	H	L	H	**A2/B2 50Ω Terminations are connected** A1/B1 50Ω Terminations are disconnected	SCL2 SDA2	HPD_SINK	HPD_SINK

Note. **H: logic high; L: logic low.**

Table-1-3: Source Selection Lookup (Standby mode)

CONTROL PINS				I/O SELECTED		HOT PLUG DETECT STATUS	
S1	**S2**	**PS**	**HPD_ctl**	**Y/Z**	**SCL_sink SDA_sink**	**HPD1**	**HPD2**
H	H	H	L	**A11/B11 are active** A12, B12, A13, B13, A14, B14, A2n, B2n are inactive	SCL1 SDA1	HPD_SINK	L
L	H	H	L	**A21/B21 are active** A22, B22, A23, B23, A24, B24, A1n, B1n are inactive	SCL2 SDA2	L	HPD_SINK

Note. **H: logic high; L: logic low;**

Table-1-4: Source Selection Lookup (Standby mode)

CONTROL PINS				I/O SELECTED		HOT PLUG DETECT STATUS	
S1	**S2**	**PS**	**HPD_ctl**	**Y/Z**	**SCL_sink SDA_sink**	**HPD1**	**HPD2**
H	H	H	H	**A11/B11 are active** A12, B12, A13, B13, A14, B14, A2n, B2n are inactive	SCL1 SDA1	HPD_SINK	HPD_SINK
L	H	H	H	**A21/B21 are active** A22, B22, A23, B23, A24, B24, A1n, B1n are inactive	SCL2 SDA2	HPD_SINK	HPD_SINK

Note. **H: logic high; L: logic low;**

Table-1-5: Source Selection Lookup (Shutdown mode)

CONTROL PINS				I/O SELECTED		HOT PLUG DETECT STATUS	
S1	**S2**	**PS**	**HPD_ctl**	**Y/Z**	**SCL_sink SDA_sink**	**HPD1**	**HPD2**
H	L	L	H	**A/B are all inactive**	Be pulled high by external pull-up termination	HPD_SINK	HPD_SINK

Note. **H: logic high; L: logic low;**

ABSOLUTE MAXIMUM RATINGS

			UNIT
Supply voltage range	VCC		-0.5V to 4V
Voltage range	Anm, Bnm		2.5V to 4V
	Ym, Zm, VSADJ, EQ, HPDn, PS, HPD_ctl, CEC_A, CEC_D		-0.5V to 4V
	SCLn, SCL_SINK, SDAn, SDA_SINK, HPD_SINK, S1, S2, S3, WPn		-0.5V to 5.5V
Electrostatic discharge	System level (direct contact) (1)	Anm, Bnm, SCLn, SDAn, HPDn,	+/-6 KV
	Human body model (2)	Anm, Bnm, SCLn, SDAn, HPDn	+/- 8 KV
		All pins	+/- 4 KV
	Machine model (2)	All pins	+/- 200V
	Charged-device model (2)	All pins	+/- 1000V

*(1) System level: tested in accordance with IEC61000-4-2
*(2) Tested in accordance with JEDEC Standard 22

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
VCC Supply voltage	3.135	3.3	3.465	V
T_A Operating free-air temperature	0	25	70	^oC
TMDS differential pins				
V_{IC} Input common mode voltage	VCC-0.4		VCC+0.01	V
V_{ID} Receiver peak-to-peak differential input voltage	150		1560	mV_{P-P}
R_{VSADJ} Resistor for TMDS compliant voltage swing range		6.2		KΩ
RP1 Resistor for TMDS calibration		0		Ω
RP2 Resistor for TMDS calibration		100		KΩ
RP3 Resistor for TMDS calibration		0		Ω
EQ Resistor for TMDS equalization calibration		0		Ω
AV_{CC} TMDS output termination voltage		3.3		V
R_T Termination resistance	45	50	55	Ω
Signaling rate	0		2.5	Gbps
Control pins (PS, HPD_ctl)				
V_{IH} LVTTL High-level input voltage	2		VCC	V
V_{IL} LVTTL Low-level input voltage	GND		0.8	V
DDC I/O pins				
$V_{I(DDC)}$ DDC input voltage	GND		5.5	V
CE capacitor		0.1u		F
RESET capacitor		0.1u		F
Status and source selector pins (S1, S2, S3, HPD_SINK)				
V_{IH} LVTTL High-level input voltage	1.5		5.5	V
V_{IL} LVTTL Low-level input voltage	GND		0.8	V

Electrical Characteristics
Over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP (1)	MAX	UNIT
I_{CC} Supply current	R_T = 50 Ω VCC = 3.3V AV_{CC} = 3.3V Data pattern = 2.5 Gbps Clock = 250 MHz	S1/S2= L/H H/H PS=L		200		mA
		S1/S2= H/L		5		mA
		S1/S2= L/H H/H PS=H		10		mA
TMDS DIFFERENTIAL PINS (A/B; Y/Z)						
V_{OH} Single-ended high-level output Voltage	R_T = 50 Ω VCC = 3.3V AV_{CC} = 3.3V		AVCC -10	AVCC	AVCC +10	mV
V_{OL} Single-ended low-level output voltage			AVCC -700	AVCC -560	AVCC - 400	mV
V_{swing} Single-ended output swing voltage			400	560	700	mV
$I_{(os)}$ Short circuit output current				11.5	14	mA
R_{INT} Input termination resistance	V_{IN} = 2.9 V		45	50	55	Ω
STATUS AND SOURCE SELECTOR PINS						
V_{IH} TTL High-level input voltage			2.5		5.5	V
V_{IL} TTL Low-level input voltage			GND		0.8	V

Electrical Characteristics (continued)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DDC I/O PINS					
$C_{IO(sink)}$ Input/output capacitance	$V_{I(PP)}$ = 1V, 100 kHz		10		pF
$V_{IH(sink)}$ High-level input voltage		2.0		5.5	V
$V_{IL(sink)}$ Low-level input voltage		GND		0.8	V
$C_{IO\ (port\ 1:4)}$ Input/output capacitance	$V_{I(PP)}$ = 1V, 100 kHz		6		pF
$V_{IH(port\ 1:4)}$ High-level input voltage		2.0		5.5	V
$V_{IL(port\ 1:4)}$ low-level input voltage		GND		0.8	V
STATUS AND SOURCE SELECTOR PINS					
V_{IH} TTL High-level input voltage		2.5		5.5	V
V_{IL} TTL Low-level input voltage		GND		0.8	V

- **(1) All typical values are at 25 ^{o}C and with a 3.3-V VCC supply.**

SWITCHING CHARACTERISTICS

Over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
TMDS DIFFERENTIAL PINS (Y/Z)					
t_{PLH} Propagation delay time, low-to-high-level output	R_T = 50 Ω AV_{CC} = 3.3V Am/Bm (1) = 250 MHz clock Am/Bm (2:4) = 2.5 Gbps pattern		1200	1500	ps
t_{PHL} Propagation delay time, high-to-low-level output			1200	1500	ps
t_r Differential output signal rise time		75		240	ps
t_f Differential output signal fall time		75		240	ps
$t_{sk(p)}$ Pulse skew (t_{PHL}-t_{PLH})			10	50	ps
$t_{sk(D)}$ Intra-pair differential skew			20	40	ps
$t_{sk(0)}$ Inter-pair differential skew			18	65	ps
$t_{jt(PP)}$ Peak-to-peak output jitter(Y1/Z1)			40	50	ps
$t_{jt(PP)}$ Peak-to-peak output jitter (Y2/Z2; Y3/Z3;Y4/Z4)			75	120	ps
t_{sx} Select to switch output			25	60	ns

***(1) All typical values are at 25℃ and with a 3.3-V VCC supply.**

Memory Features

- Operation Voltage VCC: 3.0V to 3.6V
- 2-wire Serial Interface
- Schmitt Trigger, Filtered Inputs for Noise Suppression
- Bi-directional Data Transfer Protocol
- 100 kHz Compatibility
- Write Protect Pin for Hardware Data Protection
- 1-byte Write Modes
- Self-timed Write Cycle (5 ms max)
- High-reliability
  -Endurance: 10,000 Write Cycles
  -Data Retention: 10 Years

Absolute Maximum Ratings for Memory

Operating Temperature (Plastic Package)	-40℃ to +125℃
Storage Temperature (Plastic Package)	-40℃ to +150℃
Voltage on WPn Pins with Respect to Ground	-1.0V to 5.5V
Maximum Operating Voltage	3.6V
DC Output Current	5.0mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Description

The AZHW271D provides 2048 bits of serial electrically erasable and programmable memory organized as 256 words of 8 bits each. The device is optimized for use in industrial and commercial applications where low-power and low-voltage operations are essential.

Other Description

SERIAL CLOCK (SCL): The SCL input is used to positive edge clock data into each memory device and negative edge clock data out of each device.

SERIAL DATA (SDA): The SDA pin is bi-directional for serial data transfer.

DEVICE/PAGE ADDRESSES (A0): The A0 is device address for EDID function that is hard wired for the memory.

Memory Organization

2K Serial memory: Internally organized with 1 pages of 256 bytes each, the 2K requires an 8-bit data word address for random word addressing.

WRITE PROTECT (WP): The Write Protect pin provides hardware data protection. The Write Protect pin allows normal read/write operations when connected to ground (GND). When the Write Protect pin is connected to V_{DD}, the write protection feature is enabled.

Write Protect Description

WP Pin Status	Part of the Array Protected
WP= V_{cc}	Full (2K) Array
WP=GND	Normal Read/Write Operations

DC Characteristics

Applicable over recommended operating range from: T_A=-40℃ to +85℃, V_{cc}=+3.0V to +3.6V, (unless otherwise noted).

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
V_{cc}	Supply Voltage		3.0		3.6	V
I_{cc1}	Supply Current	V_{cc}=3.3V, Read at 100K		0.4	1.0	mA
I_{cc2}	Supply Current	V_{cc}=3.3V, Write at 100K		2.0	5.0	mA
I_{SB1}	Standby Current	V_{cc}=3.0V, V_{IN}= V_{cc}/ V_{ss}			1.0	μA
I_{SB2}	Standby Current	V_{cc}=3.6V, V_{IN}= V_{cc}/ V_{ss}			6.0	μA
I_{LI}	Input Leakage Current	V_{IN}= V_{cc}/ V_{ss}		0.10	3.0	μA
I_{LO}	Output Leakage Current	V_{OUT}= V_{cc}/ V_{ss}		0.05	3.0	μA
V_{IL}[1]	Input Low Level		-0.6		V_{cc}×0.3	V
V_{IH}[1]	Input High Level		V_{cc}×0.7		V_{cc}+0.5	V
V_{OL}	Output Low Level	V_{cc}=3.0V, I_{OL}=2.1 mA			0.4	V

AC Characteristics (As shown in Fig. 1. and Fig. 2.)

Applicable over recommended operating range from: T_A=-40℃ to +85℃, V_{cc}=+3.0V to +3.6V CL=1 TTL Gate and 100pF (unless otherwise noted). Test conditions are listed in Note 2.

Symbol	Parameter	3.0-volt		3.6-volt		Units
		Min	Max	Min	Max	
f_{SCL}	Clock Frequency, SCL		100		100	kHz
t_{LOW}	Clock Pulse Width Low	4.7		4.7		μs
t_{HIGH}	Clock Pulse Width High	4.0		4.0		μs
t_{AA}	Clock Low to Data Out Valid	0.1	4.5	0.1	4.5	μs
t_{BUF}[1]	Time the bus must be free before a new transmission can Start	4.7		4.7		μs
$t_{HD.STA}$	Start Hold Time	4.0		4.0		μs
$t_{SU.STA}$	Start Setup Time	4.7		4.7		μs
$t_{HD.STA}$	Data In Hold Time	0		0		μs
$t_{SU.DAT}$	Data In Setup Time	200		200		ns
t_R	Inputs Rise Time		1.0		1.0	μs
t_F	Inputs Fall Time		300		300	ns
$t_{SU.STO}$	Stop Setup Time	4.7		4.7		μs
t_{DH}	Data Out Hold Time	100		100		ns
t_{WR}	Write Cycle Time		5		5	ms
Endurance[1]	3.3V, 25℃, Page Mode	10,000				Write Cycles

Notes: 1. This parameter is characterized and is not 100% tested.
2. AC measurement conditions:
RL (connects to VDD = 5V): 4.7kΩ.
Input and output timing reference voltages: 0.5V_{DD}
Input pulse voltages: 0.3 V_{DD} to 0.7 V_{DD}
Input rise and fall times: ≦50ns

Device Operation

CLOCK and DATA TRANSITIONS: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (refer to Figure 3). Data changes during SCL high periods will indicate a start or stop condition as defined below.

START CONDITION: A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (refer to Figure 4).

STOP CONDITION: A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the memory in a standby power mode (refer to Figure 4).

All addresses and data words are serially transmitted to and from the memory in 8-bit words. The memory sends a zero to acknowledge that it has received each word. This happens during the ninth clock cycle. Following receipt each word from the memory, the microcontroller should send a zero to memory and continue to output the next data word or send a stop condition to finish the read cycle (refer to Figure 5).

STANDBY MODE: The memory features a low-power standby mode which is enabled: (a) upon power-up and (b) after the receipt of the stop bit and the completion of any internal operations.

DEVICE RESET: After an interruption in protocol, power loss or system reset, any 2-wire part can be protocol reset by following these steps:

1. Clock up to 9 cycles.
2. Look for SDA high in each cycle while SCL is high.
3. Create a start condition.

Device Addressing

The 2K memory device requires an 8-bit device address word following a start condition to enable the chip for a read or write operation.

The device address word consists of a mandatory one, zero sequence for the first four most significant bits as shown. This is common to all the memory devices.

The next 3 bits are the 0, 0 and 0 device address bits for the memory. These 3 bits must compare to their corresponding hard-wired input pins.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low (refer to Figure 6).

Upon a compare of the device address, the memory will output a zero. If a compare is not made, the chip will return to a standby state.

Write Operations

BYTE WRITE: A write operation requires an 8-bit data word address following the device address word and acknowledgment. Upon receipt of this address, the memory will again respond with a zero and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the memory will output a zero and the addressing device, such as a

microcontroller, must terminate the write sequence with a stop condition. At this time the memory enters an internally timed write cycle, $t_{WR,}$ to the nonvolatile memory. All inputs are disabled during this write cycle and the memory will not respond until the write is complete (refer to Figure 7).

PAGE WRITE: The 2K memory is capable of a 256-byte page write.

A page write is initiated the same as a byte write, but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the memory acknowledges receipt of the first data word, the microcontroller can transmit up to seven data words. The memory will respond with a zero after each data word received. The microcontroller must terminate the page write sequence with a stop condition (refer to Figure 8).

The data word address lower three bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than eight data words are transmitted to the memory, the data word address will "roll over" and previous data will be overwritten.

ACKNOWLEDGE POLLING: Once the internally timed write cycle has started and the memory inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the memory respond with a zero allowing the read or write sequence to continue.

Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to one . There are three read operations: current address read, random address read and sequential read.

CURRENT ADDRESS READ: The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address "roll over" during read is from the last byte of the last memory page to the first byte of the first page. The address "roll over" during write is from the last byte of the current page to the first byte of the same page.

Once the device address with the read/write select bit set to one is clocked in and acknowledged by the memory the current address data word is serially clocked out. The microcontroller does not respond with an input zero but does generate a following stop condition (refer to Figure 9).

RANDOM READ: A random read requires a "dummy" byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the memory, the microcontroller must generate another start

condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The memory acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a zero but does generate a following stop condition (refer to Figure 10).

SEQUENTIAL READ: Sequential reads are initiated by either a current address read or a random address read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the memory receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will "roll over" and the sequential read will continue. The sequential read operation is terminated when the microcontroller does not respond with a zero but does generate a following stop condition (refer to Figure 11).

Fig.1. Bus Timing Definition

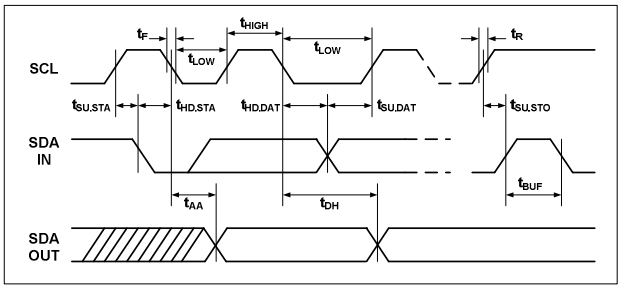
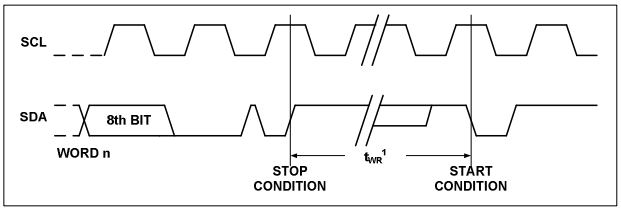


Fig. 2. SCL: Serial Clock, SDA: Serial Data I/O



Note: 1. The write cycle time t_{WR} is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.

Fig. 3. Data Validity

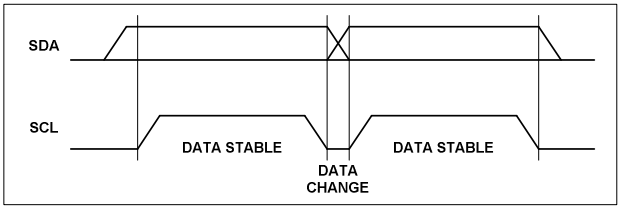


Fig. 4. Start and Stop Definition

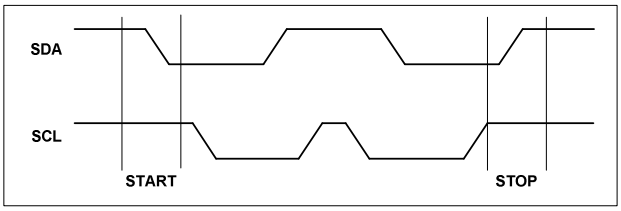


Fig. 5. Output Acknowledge

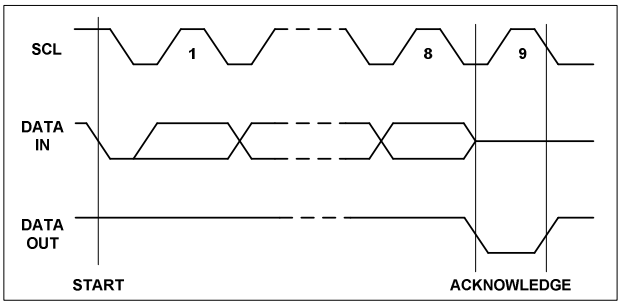


Fig. 6. Device Address

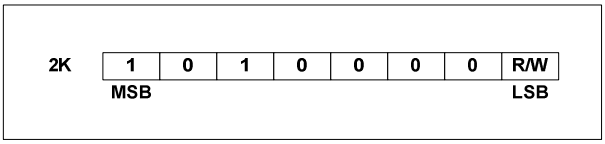


Fig. 7. Byte Write

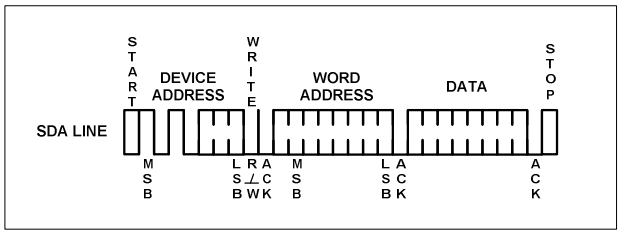


Fig. 8. Page Write

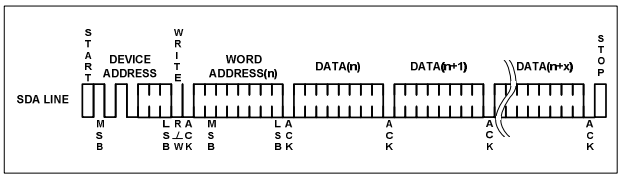


Fig. 9. Current Address Read

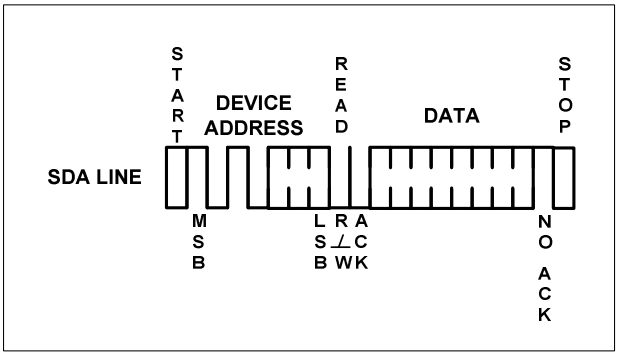


Fig. 10. Random Read

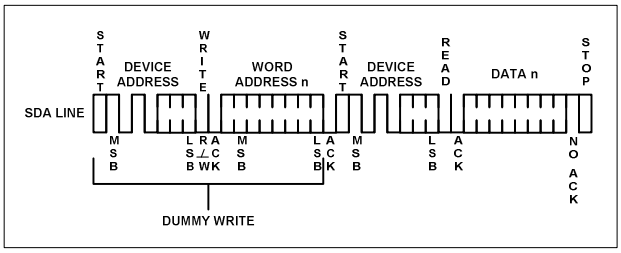
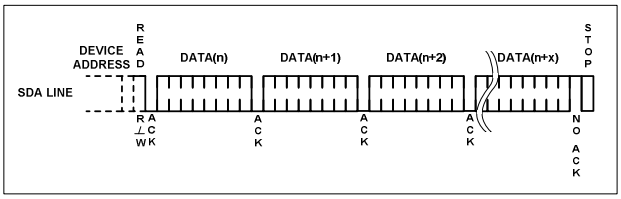


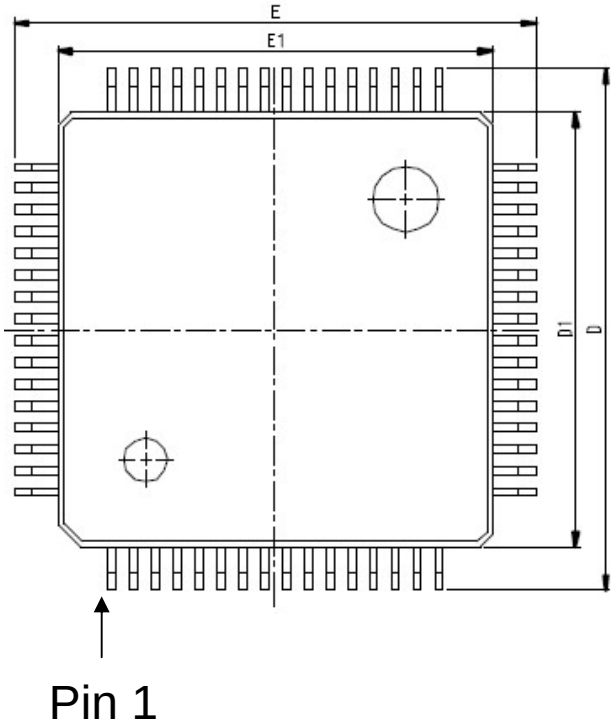
Fig. 11. Sequential Read



64-pin LQFP

PACKAGE DIAGRAMS

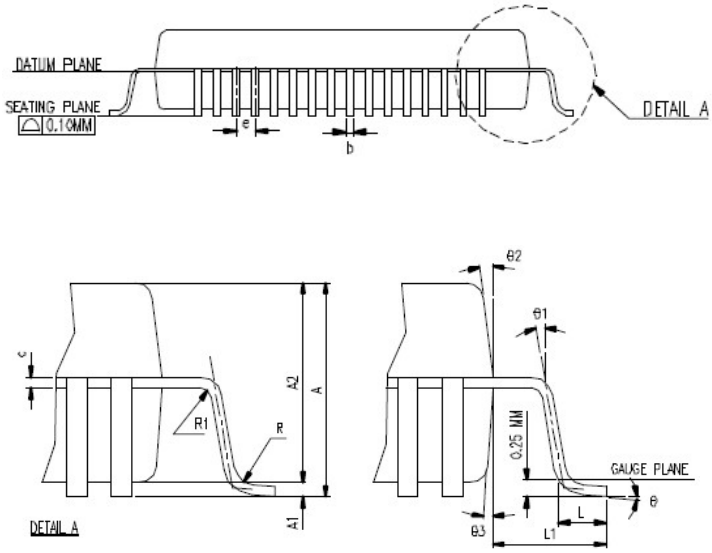
TOP VIEW



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.20	0.23	0.007	0.008	0.009
c	0.09		0.16	0.004		0.006
e	0.50 BASIC			0.020 BASIC		
D	12.00 BASIC			0.472 BASIC		
D1	10.00 BASIC			0.394 BASIC		
E	12.00 BASIC			0.472 BASIC		
E1	10.00 BASIC			0.394 BASIC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF.			0.039 REF.		
R1	0.08			0.003		
R	0.08		0.20	0.003		0.008
θ	0	3.5	7	0	3.5	7
θ1	0			0		
θ2	11	12	13	11	12	13
θ3	11	12	13	11	12	13
JEDEC	MS-026 (BCD)					

NOTES : DIMENSIONS " D1 " AND " E1 " DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSIN IS 0.25 mm PER SIDE. " D1 " AND " E1 " ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.

SIDE VIEW



Marking Code

Part Number	Marking Code
AZHW271D	AZHW271D

Revision History

Revision	Modification Description
Revision 2011/05/22	Preliminary Release.
Revision 2011/08/09	Formal Release.