Features

- Compatible with HDMI 1.3b
- Supports 2.25 Gbps Signaling Rate for 480i/p, 720i/p, and 1080i/p Resolutions up to 12-Bit Color Depth
- Integrated Receiver Termination
- Selectable Receiver Equalization to Accommodate to Different Input Cable Lengths
- Intra-Pair Skew < 40 ps
- Inter-Pair Skew < 65 ps
- ***System Level ESD Protection Exceeds 8 kV (direct contact) for TMDS Inputs and DDC Interface***
- Supply Voltage, VCC= 3.3 V +/- 5%
- 5-V Tolerance on All Side Band Signals
- 64-pin LQFP Package
- ***Green Part*** and 260 °C reflow rated

Applications

- Digital TV
- Digital projector
- Digital Monitor
- Audio video receiver

Description

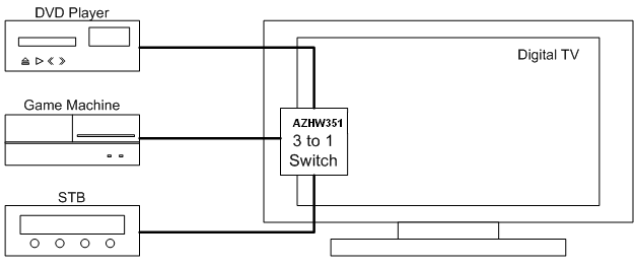
The AZHW351 is a 3-port High-Definition Multimedia Interface (HDMI) or DVI switch which allows up to 3 HDMI or DVI ports to be switched to a single display terminal. Four TMDS channels, one hot plug detector, and a digital display control (DDC) interface are supported on each port. Each TMDS channel allows signaling rates up to 2.25 Gbps to allow 1080p resolution in 12-bit color depth.

With two control pins, all input terminations can be disconnected, TMDS inputs are high impedance with standard TMDS terminations, all internal devices are turned off to disable the DDC links, and all HPD outputs are connected to the HPD_SINK. This allows the initiation of the HDMI physics address discovery process.

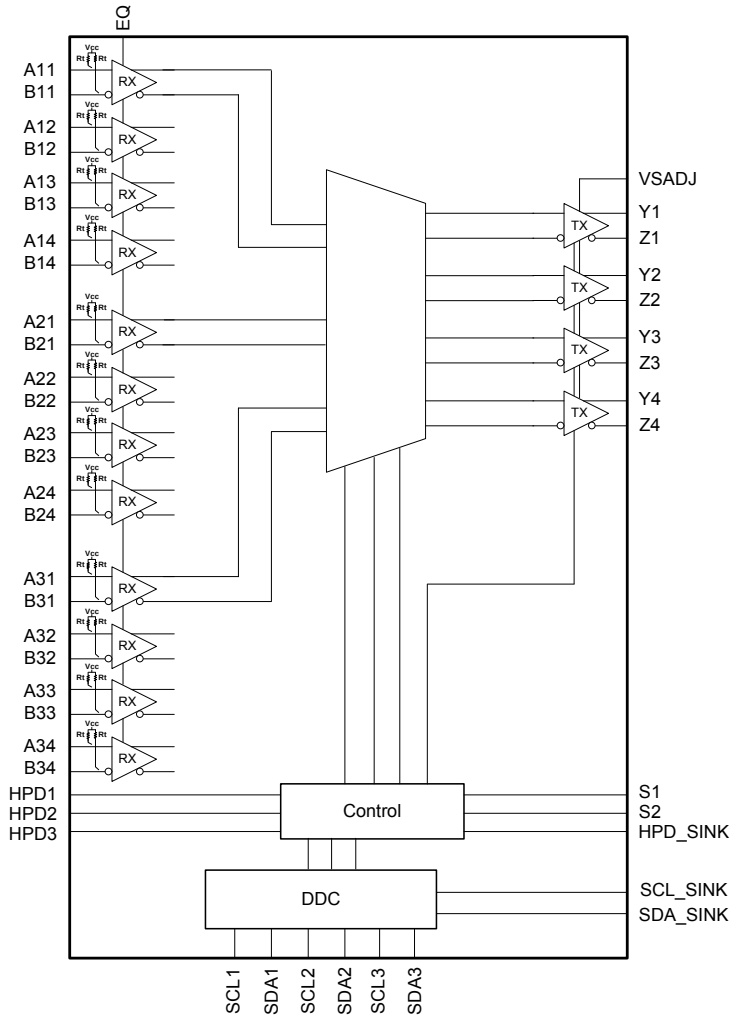
Termination resistor (50-Ω), pulled up to VCC, are integrated at each TMDS receiver input. External terminations are not required.

The AZHW351 provides two levels of input equalization for different ranges of cable lengths. Each TMDS receiver owns frequency responsive equalization circuits. When EQ sets high, the receiver supports the connection in short range HDMI cables. When EQ sets low (recommended value), the receiver supports the input connection in long range HDMI cables. The AZHW351 supports two power saving operations. When a system is under power down mode and there is no digital audio/visual content from a connected source to minimize power consumption from TMDS inputs, outputs, and internal circuits. When a system in under standby mode, only TMDS clock inputs, outputs and termination are turned on, and the selected DDC link from the source to sink. The device is characterized for operation from 0 °C to 70 °C.

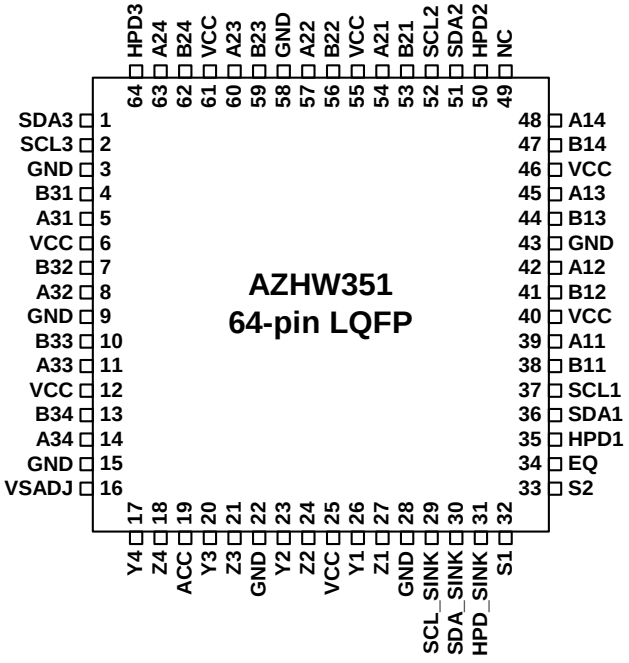
Typical application



Circuit diagram



Pin Configuration



TERMINAL FUNCTIONS

TERMINAL		I/O	Description
NAME	NO.		
A11, A12, A13, A14	39, 42, 45, 48	I	Source port 1 TMDS positive inputs
A21, A22, A23, A24	54, 57, 60, 63	I	Source port 2 TMDS positive inputs
A31, A32, A33, A34	5, 8, 11, 14	I	Source port 3 TMDS positive inputs
B11, B12, B13, B14	38, 41, 44, 47	I	Source port 1 TMDS negative inputs
B21, B22, B23, B24	53, 56, 59, 62	I	Source port 2 TMDS negative inputs
B31, B32, B33, B34	4, 7, 10, 13	I	Source port 3 TMDS negative inputs
GND	3, 9, 15, 22, 28, 43, 58	---	Ground
EQ	34	I	TMDS input equalization selector EQ= high---HDMI 1.3 compliant cable EQ= low---10m 28 AWG HDMI cable
HPD1	35	O	Source port 1 hot plug detector output
HPD2	50	O	Source port 2 hot plug detector output
HPD3	64	O	Source port 3 hot plug detector output
HPD_SINK	31	I	Sink port hot plug detector input
SCL1	37	I/O	Source port 1 DDC I^2C clock line
SCL2	52	I/O	Source port 2 DDC I^2C clock line
SCL3	2	I/O	Source port 3 DDC I^2C clock line
SCL_SINK	29	I/O	Sink port DDC I2C clock line
SDA1	36	I/O	Source port 1 DDC I^2C data line
SDA2	51	I/O	Source port 2 DDC I^2C data line
SDA3	1	I/O	Source port 3 DDC I^2C data line
SDA_SINK	30	I/O	Sink port DDC I^2C data line
S1, S2	32, 33	I	Source selector
VCC	6, 12, 19, 25, 40, 46, 55, 61	---	Power supply
VSADJ	16	I	TMDS compliant voltage swing control
Y1, Y2, Y3, Y4	26, 23, 20, 17	O	Sink port TMDS positive outputs
Z1, Z2, Z3, Z4	27, 24, 21, 18	O	Sink port TMDS negative outputs

Table-1: Source Selection Lookup

Operation Model	CONTROL PINS		I/O SELECTED		HOT PLUG DETECT STATUS		
	S1	S2	Y/Z	SCL_sink SDA_sink	HPD1	HPD2	HPD3
Normal Operation	H	H	**A1/B1** Terminations of A2/B2 and A3/B3 are disconnected	SCL1 SDA1	HPD_SINK	L	L
	L	H	**A2/B2** Terminations of A1/B1 and A3/B3 are disconnected	SCL2 SDA2	L	HPD_ SINK	L
	L	L	**A3/B3** Terminations of A1/B1 and A2/B2 are disconnected	SCL3 SDA3	L	L	HPD_ SINK
Power Down	H	L	All terminations are disconnected	Are pulled High by external pull-up termination	HPD_ SINK	HPD_ SINK	HPD_ SINK
Standby	M	L/H	**A11/B11** Terminations of others are disconnected	SCL1 SDA1	HPD_ SINK	L	L
	L/H	M	**A21/B21** Terminations of others are disconnected	SCL2 SDA2	L	HPD_ SINK	L
	M	M	**A31/B31** Terminations of others are disconnected	SCL3 SDA3	L	L	HPD_ SINK

Note. **H: logic high; L: logic low; M: logic middle state**

ABSOLUTE MAXIMUM RATINGS

			UNIT
Supply voltage range	VCC		-0.5V to 4V
Voltage range	Anm, Bnm		2.5V to 4V
	Ym, Zm, VSADJ, EQ		-0.5V to 4V
	SCLn, SCL_SINK, SDAn, SDA_SINK, HPDn, HPD_SINK, S1, S2		-0.5V to 6V
Electrostatic discharge	System level (direct contact) (1)	Anm, Bnm, SCLn, SDAn, HPDn,	+/-8 KV
	Human body model (2)	Anm, Bnm, SCLn, SDAn, HPDn	+/- 8 KV
		All pins	+/- 4 KV
	Machine model (2)	All pins	+/- 200V
	Charged-device model (2)	All pins	+/- 1000V

*(1) System level: tested in accordance with IEC61000-4-2

*(2) Tested in accordance with JEDEC Standard 22

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
VCC Supply voltage	3.135	3.3	3.465	V
T_A Operating free-air temperature	0	25	70	°C
TMDS differential pins				
V_{IC} Input common mode voltage	VCC-0.4		VCC+0.01	V
V_{ID} Receiver peak-to-peak differential input voltage	150		1560	mV_{P-P}
R_{VSADJ} Resistor for TMDS compliant voltage swing range		6.2k		Ω
AV_{CC} TMDS output termination voltage		3.3		V
R_T Termination resistance	45	50	55	Ω
Signaling rate	0		2.25	Gbps
Control pins (EQ)				
V_{IH} LVTTL High-level input voltage	2		Vcc	V
V_{IL} LVTTL Low-level input voltage	GND		0.8	V
DDC I/O pins				
$V_{I(DDC)}$ DDC input voltage	GND		5.5	V
Status and source selector pins (S1, S2, HPD_SINK)				
V_{IH} LVTTL High-level input voltage	2.5		5.5	V
V_{IL} LVTTL Low-level input voltage	GND		0.8	V
V_{IM} Middle state input voltage	1.6		2.0	V

Electrical Characteristics
Over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP (1)	MAX	UNIT
I_{CC} Supply current	R_T = 50 Ω VCC = 3.3V AV_{CC} = 3.3V Data pattern = 2.25 Gbps Clock = 225 MHz	S1/S2= L/L L/H H/H		205	232	mA
		S1/S2= H/L		6	14	mA
		S1/S2= M/L M/H L/M H/M M/M		50	80	mA
TMDS DIFFERENTIAL PINS (A/B; Y/Z)						
V_{OH} Single-ended high-level output Voltage	R_T = 50 Ω VCC = 3.3V AV_{CC} = 3.3V		AVCC -10	AV_{CC}	AVCC +10	mV
V_{OL} Single-ended low-level output voltage			AVCC -700	AV_{CC} -560	AVCC - 400	mV
V_{swing} Single-ended output swing voltage			400	560	700	mV
$I_{(os)}$ Short circuit output current				11.5	14	mA
R_{INT} Input termination resistance	V_{IN} = 2.9 V		45	50	55	Ω

Electrical Characteristics (continued)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DDC I/O PINS					
C_{IO} Input/output Capacitance	$V_{I(PP)}$ = 1V, 100 kHz		6	18	pF
R_{ON} Switch resistance	I_O = 3 mA, V_O = 0.4 V		80	150	Ω
V_{PASS} Switch output voltage	V_I = 3.3V, I_O=100 μA	1.5	2.0	2.5	V
STATUS AND SOURCE SELECTOR PINS					
V_{IH} TTL High-level input voltage		2.5		5.5	V
V_{IL} TTL Low-level input voltage		GND		0.8	V
V_{IM} Middle state input voltage		1.6		2.0	V

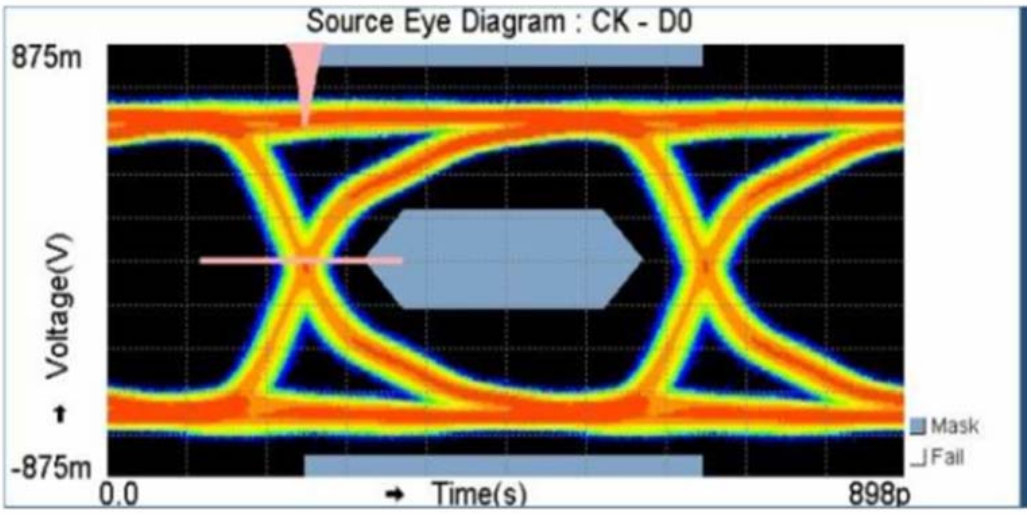
*** (1) All typical values are at 25 °C and with a 3.3-V VCC supply.**

SWITCHING CHARACTERISTICS

Over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
TMDS DIFFERENTIAL PINS (Y/Z)					
t_{PLH} Propagation delay time, low-to-high-level output	R_T = 50 Ω AV_{CC} = 3.3V Am/Bm (1) = 225 MHz clock Am/Bm (2:4) = 2.25 Gbps pattern		1200	1500	ps
t_{PHL} Propagation delay time, high-to-low-level output			1200	1500	ps
t_r Differential output signal rise time		75	140	240	ps
t_f Differential output signal fall time		75	140	240	ps
$t_{sk(p)}$ Pulse skew (t_{PHL}-t_{PLH})			10	50	ps
$t_{sk(D)}$ Intra-pair differential skew			20	40	ps
$t_{sk(0)}$ Inter-pair differential skew			18	65	ps
$t_{jt(PP)}$ Peak-to-peak output jitter(Y1/Z1)			40	50	ps
$t_{jt(PP)}$ Peak-to-peak output jitter (Y2/Z2; Y3/Z3;Y4/Z4)			75	120	ps
t_{sx} Select to switch output			25	60	ns

***(1) All typical values are at 25℃ and with a 3.3-V VCC supply.**



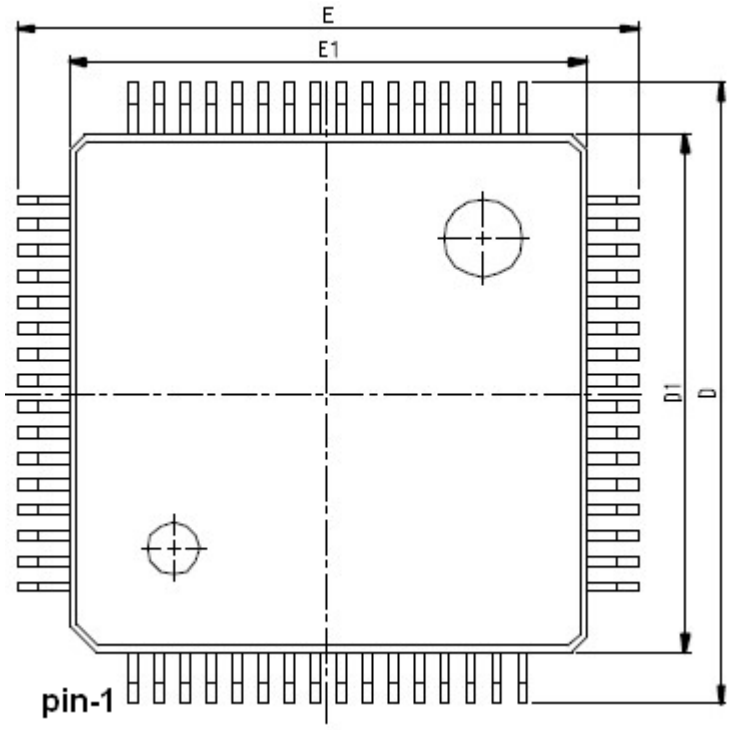
Eye diagram of the differential output at Ta = 25℃, AV_{CC}=3.3 V, VCC=3.3 V, differential swing at the input = 1000 mV, data rate = 2.25 Gbps,

Mechanical Details

64-pin LQFP

PACKAGE DIAGRAMS

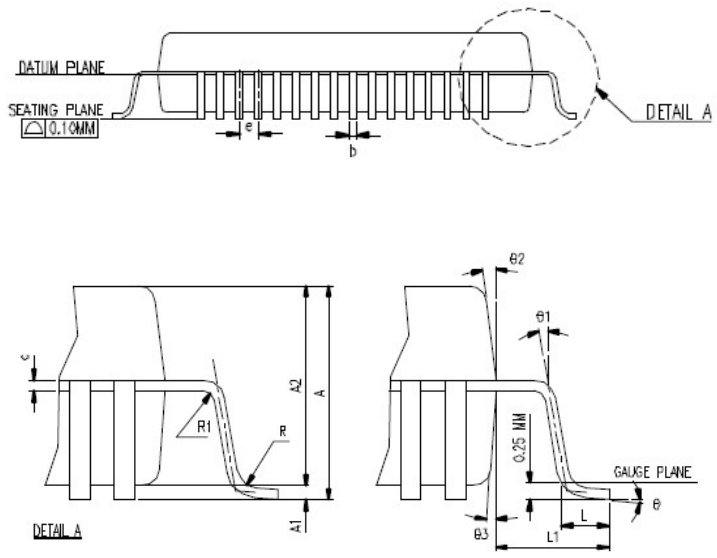
TOP VIEW



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.20	0.23	0.007	0.008	0.009
c	0.09		0.16	0.004		0.006
e	0.50 BASIC			0.020 BASIC		
D	12.00 BASIC			0.472 BASIC		
D1	10.00 BASIC			0.394 BASIC		
E	12.00 BASIC			0.472 BASIC		
E1	10.00 BASIC			0.394 BASIC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF.			0.039 REF.		
R1	0.08			0.003		
R	0.08		0.20	0.003		0.008
θ	0	3.5	7	0	3.5	7
θ1	0			0		
θ2	11	12	13	11	12	13
θ3	11	12	13	11	12	13
JEDEC	MS-026 (BCD)					

⚠ NOTES : DIMENSIONS " D1 " AND " E1 " DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSIN IS 0.25 mm PER SIDE.
" D1 " AND " E1 " ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.

SIDE VIEW



Marking Code

Part Number	Marking Code
AZHW351	AZHW351
AZHW351 (Engineering Samples)	E01016-8

Revision History

Revision	Modification Description
Revision 2008/08/26	Preliminary Release.
Revision 2008/12/01	* Updated EQ selection function. * Updated R_{VSADJ} resistor value to 6.2 kΩ.
Revision 2009/01/05	Formal version initial release.
Revision 2009/01/19	Add “pin-1” indication on package diagram.