

Quad High Side Switch (Dual 10 mOhm, Dual 35 mOhm)

Thermal Addendum

Introduction

This thermal addendum is provided as a supplement to the 10XS3435 technical data sheet. The addendum provides thermal performance information that may be critical in the design and development of system applications. All electrical, application and packaging information is provided in the data sheet.

Package and Thermal Considerations

This 10XS3435 is a dual die package. There are two heat sources in the package independently heating with P_1 and P_2 . This results in two junction temperatures, T_{J1} and T_{J2} , and a thermal resistance matrix with $R_{\theta JA mn}$.

For $m, n = 1$, $R_{\theta JA11}$ is the thermal resistance from Junction 1 to the reference temperature while only heat source 1 is heating with P_1 .

For $m = 1, n = 2$, $R_{\theta JA12}$ is the thermal resistance from Junction 1 to the reference temperature while heat source 2 is heating with P_2 . This applies to $R_{\theta J21}$ and $R_{\theta J22}$, respectively.

$$\begin{Bmatrix} T_{J1} \\ T_{J2} \end{Bmatrix} = \begin{bmatrix} R_{\theta JA11} & R_{\theta JA12} \\ R_{\theta JA21} & R_{\theta JA22} \end{bmatrix} \cdot \begin{Bmatrix} P_1 \\ P_2 \end{Bmatrix}$$

The stated values are solely for a thermal performance comparison of one package to another in a standardized environment. This methodology is not meant to and will not predict the performance of a package in an application-specific environment. Stated values were obtained by measurement and simulation according to the standards listed below.

Standards

Table 1. Thermal Performance Comparison

Thermal Resistance	1 = Power Chip, 2 = Logic Chip [$^{\circ}\text{C}/\text{W}$]		
	$m = 1, n = 1$	$m = 1, n = 2$ $m = 2, n = 1$	$m = 2, n = 2$
$R_{\theta JA mn}$ (1)(2)	27.13	18.31	35.53
$R_{\theta B mn}$ (2)(3)	14.31	6.54	23.61
$R_{\theta JA mn}$ (1)(4)	47.77	36.90	54.35
$R_{\theta C mn}$ (5)	1.38	0.00	0.91

Notes:

- Per JEDEC JESD51-2 at natural convection, still air condition.
- 2s2p thermal test board per JEDEC JESD51-7 and JESD51-5.
- Per JEDEC JESD51-8, with the board temperature on the center trace near the power outputs.
- Single layer thermal test board per JEDEC JESD51-3 and JESD51-5.
- Thermal resistance between the die junction and the exposed pad, "infinite" heat sink attached to exposed pad.

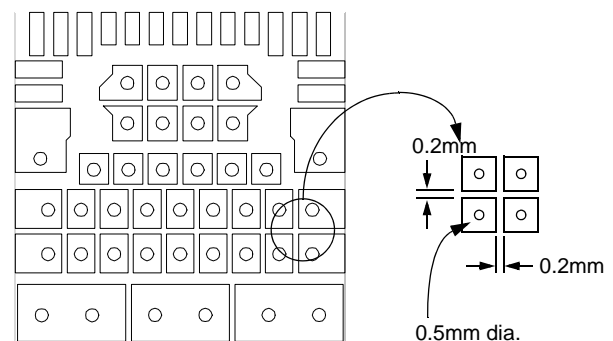
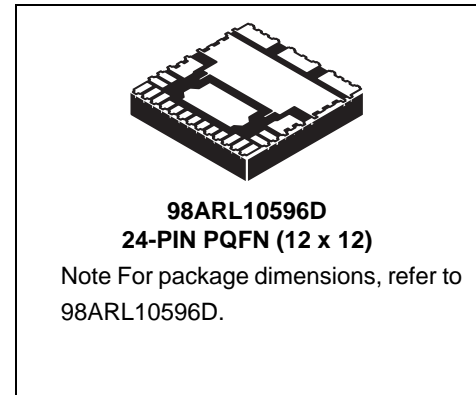
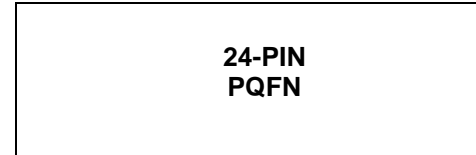
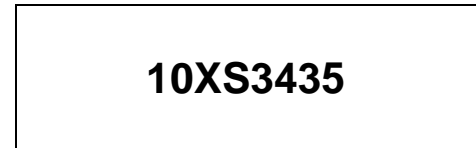


Figure 1. Detail of Copper Traces Under Device with Thermal Vias

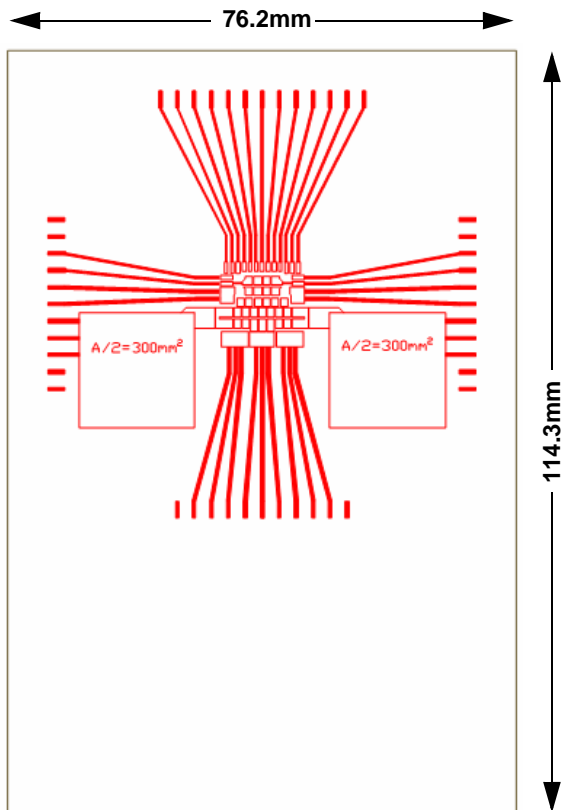


Figure 2. 1s JEDEC Thermal Test Board Layout

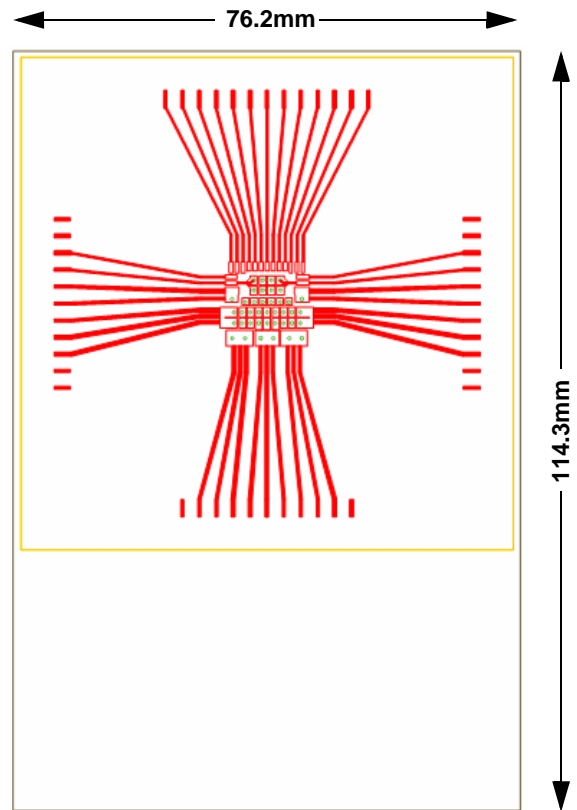


Figure 3. 2s2p JEDEC Thermal Test Board (Red - Top Layer, Yellow - Two Buried Layers)

Transparent Top View

MC10XS3435 Pin Connections
 24-PIN PQFN (12 x 12)
 0.9 mm Pitch
 12.0mm 12.0mm Body

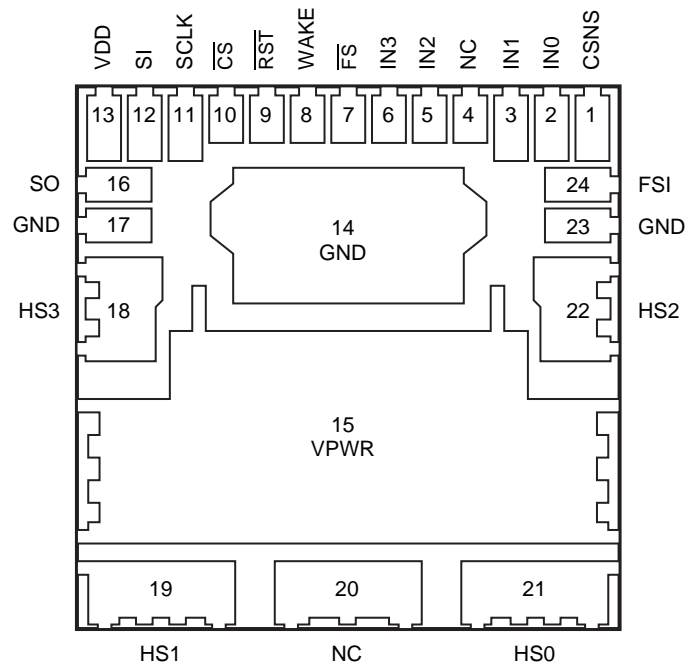


Figure 4. Pin Connections

Device on Thermal Test Board

Material: Single layer printed circuit board
 FR4, 1.6 mm thickness
 Cu traces, 0.07 mm thickness
 Cu buried traces thickness 0.035mm

Outline: 76.2mm x 114.3mm board area,
 including edge connector for thermal
 testing, 74mm x 74mm buried layers
 area

Area A: Cu heat-spreading areas on board
 surface

Ambient Conditions: Natural convection, still air

Table 2. Thermal Resistance Performance

Thermal Resistance	Area A (mm ²)	1 = Power Chip, 2 = Logic Chip (°C/W)		
		m = 1, n = 1	m = 1, n = 2 m = 2, n = 1	m = 2, n = 2
R _{θJA_{mn}}	0	47.77	36.90	54.35
	150	42.90	33.21	51.07
	300	40.95	31.78	49.63
	450	39.85	30.89	48.61
	600	38.96	30.21	47.90

R_{θJA} is the thermal resistance between die junction and ambient air.

This device is a dual die package. Index *m* indicates the die that is heated. Index *n* refers to the number of the die where the junction temperature is sensed.

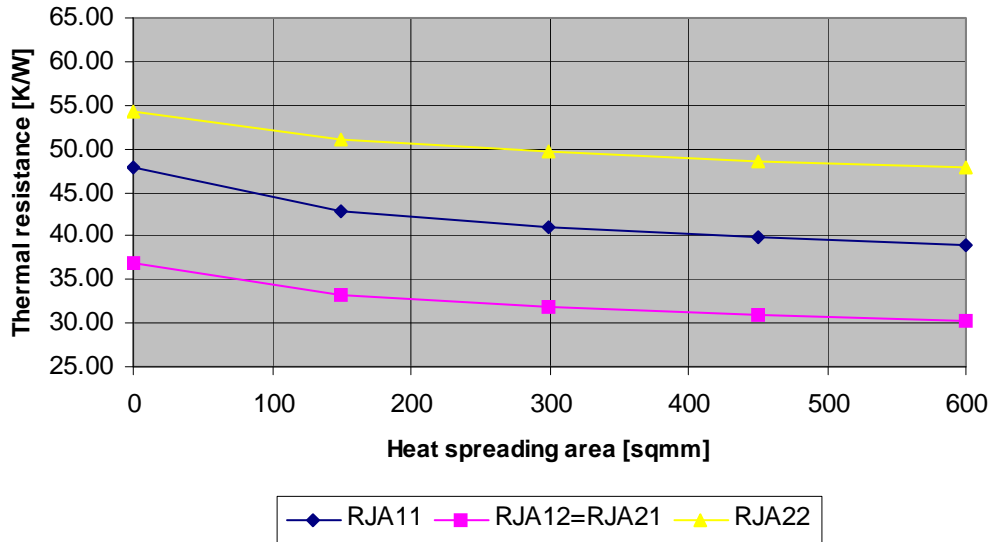


Figure 5. Steady State Thermal Resistance in Dependence on Heat Spreading Area; 1s JEDEC Thermal Test Board with Spreading Areas

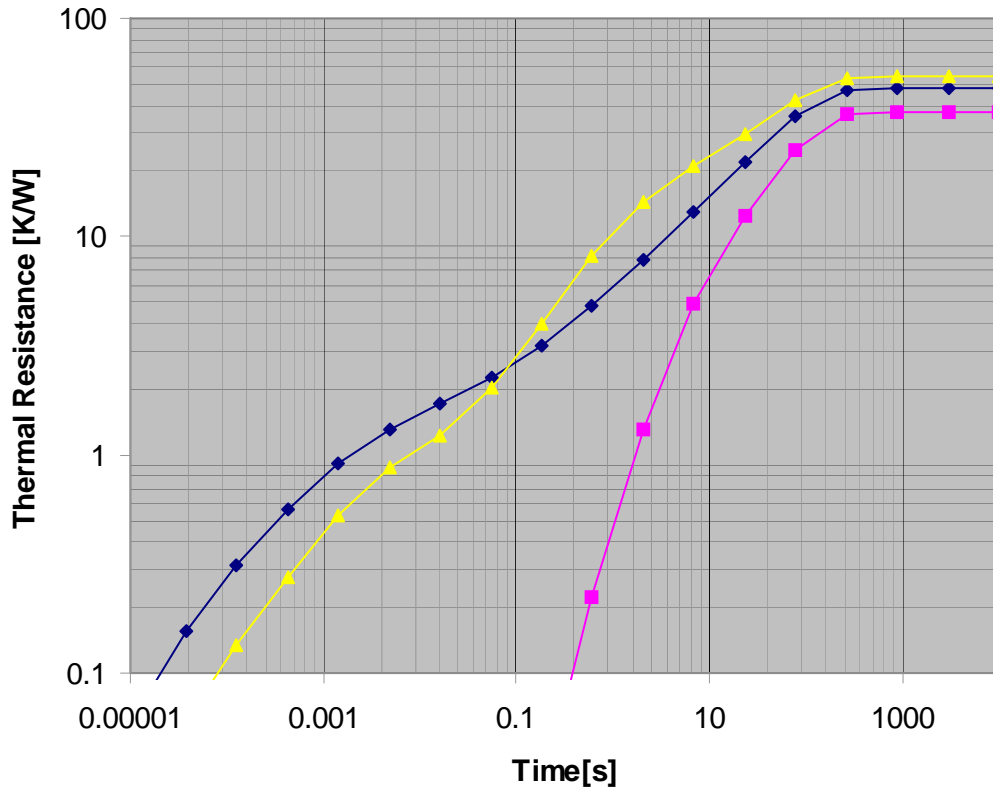


Figure 6. Transient Thermal 1W Step Response; Device on 1s JEDEC Standard Thermal Test Board with Heat Spreading Areas 600 Sq. mm

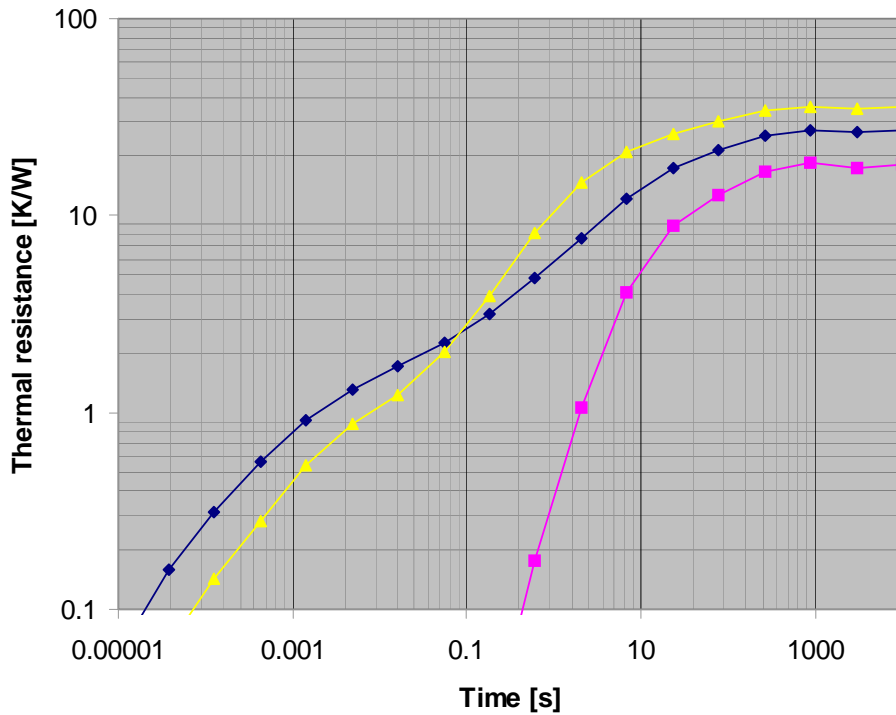


Figure 7. Transient Thermal 1W Step Response; Device on 2s2p JEDEC Standard Thermal Test Board

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