Freescale Semiconductor
Application Note

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Thermal Modeling and Simulation of 12V Gen3 eXtreme Switch Devices with SPICE

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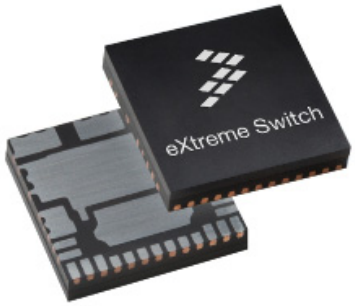

1 Summary

This Application Note presents a SPICE-based method for thermal modeling, simulation and design of a multi-channel power semiconductor switch on a Printed Circuit Board (PCB). The method allows rapid and simultaneous determination of the temperature of semiconductor junctions and the PCB track below the device, both under transient conditions and at steady-state. The model takes thermal cross-coupling between the device's channels into account.

SPICE models of 4 different devices and 2 different PCB design layouts have been developed. By combining the device models with those of different PCB layouts, followed by SPICE simulation, the best compromise between minimum PCB surface and sufficient heatsink properties can be found iteratively. The method was validated by comparing simulated with measured thermal impedance curves. Models of the following 4 devices are currently available: MC10XS3412DPNA, MC15XS3400DPNA, MC35XS3400DPNA, MC10XS3435DPNA

Contents

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2 Introduction

When a system uses power devices for load control or power conversion, the choice of the power semiconductors has broad effects on the module. Directly or indirectly the power components affect the system's efficiency, reliability, thermal performance and required thermal management, size, weight, cost, etc.

Often the primary figure of merit for a power component is its efficiency, and for a power transistor a primary feature is its on-state voltage, or, for a power MOSFET, its on-resistance and its ability to withstand high power peaks during short durations. Often the device is sized to meet a maximum operating temperature requirement. In that case the device's thermal behavior has a strong influence on its operating temperature. Therefore, a device's thermal behavior is one of the primary figures of merit. Having a good understanding of the thermal behavior allows the designer to optimize the device selection - choosing the device that is not oversized (and too expensive) and not undersized (and too hot and unreliable).

For a given application, the most critical thermal considerations are always associated with the worst case operating conditions. Often, worst case conditions occur during system transients such as voltage spikes, load faults, load overloads, etc. Therefore, it is insufficient to have only good steady state thermal characterization. One also needs good characterization of the system's transient thermal response to evaluate the system's transient thermal behavior.

These considerations become all the more important when the system requires numerous power components, in which case the power devices make up a significant portion of the module's features and cost.

3 Contents of the Application Note

This Application Note describes a modeling & simulation procedure which allows selection of the most adequate power semiconductor device for a particular PCB layout. Thanks to the use of a model-order-reduction (MOR) technique (see Ref. [6]), a reduced order model is obtained as a state-space model. This model has been transformed into an electrical equivalent circuit (SPICE-compatible). Section 4 describes the state-of-the-art of thermal modeling of power devices. Section 5 gives the general approach of the method, such as applied to the Freescale eXtreme Switch family. Section 6 gives a description of the model's limitations. Section 7 describes thermal modeling by an electrical equivalent circuit. Section 8 is dedicated to model validation. Section 9 shows a practical example of thermal model simulation using Cadence SPICE.

4 Today's Specifications and Software Tools

To complete the necessary steady state and transient thermal assessments, designers must rely on the thermal characterization suppliers provide. But here, the suppliers have a problem meeting customer needs. The thermal environment consists of the intended device plus the heatsinking the designer provides. Suppliers do not know and do not control how the device will be mounted and what thermal environment the device will experience. They are forced to provide characterizations that target either the expected usage or that are idealized. For the former, thermal characterization might be specified with a carefully defined PCB mounted in a carefully defined chamber. For the latter, the power device might be mounted to an “infinite heatsink”, where the thermal tab is kept at a fixed temperature.

The reality is that these generic or idealized conditions used in thermal specifications rarely match the conditions of the application. This forces module designers to apply the ratings to their systems with less rigor than they would like. The result can be an over designed system or unsubstantiated design decisions.

Good thermal characterization tends to be based on power transistor specifications, and those tend to be based on JEDEC standards. These standards assume that the specified power is applied uniformly to the die surface, that there is a single heat source on the die and target predicting the average die temperature rather than the temperature at a particular point of the die. However, many new devices integrate more than one power dissipating source onto the die. Models or thermal characterizations may not account for multiple power sources in a single package.

Characterization is often provided for a device on a PCB with specific features such as board and copper plating thicknesses, trace width, length and location, via features (if any), copper flag area (if any), etc. The device and its PCB are specified as a unit, so there is no clean way to separate the PCB portion of the thermal circuit from that of the component. A typical transient thermal response characterization does not define the model's accuracy range.

The transient thermal response is not easy to use unless it is converted to an electrical equivalent circuit that can be coupled to an arbitrary power stimulus.

The tools developed by Freescale solve the majority of these problems:

1. Independent thermal models for PCB and switching device are supplied
2. Temperature of the temperature sensor, located at the Over Temperature Shutdown (OTSD) measurement spot, is measured (not average T_J)
3. Cross-coupling between multiple power sources in a single (PQFN) package has been modeled
4. Indications have been provided with respect to the model’s accuracy range
5. Users can integrate their own PCB models and couple them to Freescale’s eXtreme Switch device models

5 SPICE Thermal Modeling of Freescale eXtreme Switches

Freescale's eXtreme Switch product family consists of Smart High-Side switches based on Power MOSFET technology. These devices typically contain 4 MOSFETs with associated drive, diagnostic, and protection circuitry. Most of Freescale’s eXtreme Switches are housed in a Power Quad Flat No-Lead (PQFN) package. They are suited for automotive lighting and DC-Motor applications. In some applications, the ambient temperature may reach the maximum specified level, but switching and conduction losses inside the MOSFET will cause an additional increase of junction temperature. It is nevertheless mandatory to keep the maximum junction temperature of a MOSFET within the authorized range, since otherwise device reliability may be impacted, eventually leading to device failure. In addition, the temperature of the PCB material below the power device should not exceed that of the PCB’s temperature grade.

PCB material with a temperature grade >125°C is often considered as exotic and therefore expensive. This leads to a tendency to maximize the PCB's copper surface in contact with the power semiconductor package.

On the other hand, the PCB surface must be minimized to save costs. Hence, the ability to predict the thermal performances of a particular design layout is an important element when designing a cost-optimized and reliable system. Such a design procedure might consist of performing a simulation of a given layout and progressively improving it after having analyzed different simulation results. A Finite Element simulation is not adapted to such a procedure due to unacceptably long simulation times. Moreover, the amount of information made available by a finite element simulation is extremely high. This may be interesting for the semiconductor manufacturer, but not necessarily for a system design engineer just trying to select the most suitable switching device among several available types. The solution to this problem is to use simple but accurate thermal models, the simulation of which can be performed in less than 1 minute on a standard PC. To make this approach accessible to a large public, the universal circuit simulator SPICE was selected by Freescale.

6 Terminology, Assumptions and Restrictions

The most commonly used parameter describing thermal performance of a semiconductor device in its environment is the thermal resistance from junction to ambient, $R_{\theta(JA)}$. However, in data sheets this parameter is a measure of the thermal performance of the IC package mounted on a specific test board, usually those defined by JEDEC. When JEDEC conditions are not followed and the excursions from the standard are not documented, test variations can have a significant effect on the value of $R_{\theta(JA)}$.

The measurement of $R_{\theta(JA)}$ is usually performed by injecting a known power, usually 1W, into the junction of the test chip. The junction temperature is estimated by monitoring a temperature sensitive parameter such as a diode forward voltage. The difference in measured ambient temperature compared to the measured junction temperature is calculated and is divided by the dissipated power, giving a value for $R_{\theta(JA)}$ in °C/W.

Unfortunately, $R_{\theta(JA)}$ is often used by system designers to estimate junction temperatures of their devices when used on PCBs with layouts other than those defined by the JEDEC standards. The test board is simply considered as a heat sink that is soldered to the leads of the device. Junction temperature is computed accordingly to the expression:

$$T_{junction}=T_{ambient} + R_{\theta(JA)}* P$$

The thermal resistance $R_{\theta(JA)}$ is decomposed in 3 contributors: thermal resistance from junction to case, $R_{\theta(JC)}$, thermal resistance from case to (heat)sink, $R_{\theta(CS)}$, and thermal resistance from sink to ambient $R_{\theta(SA)}$ In most cases, $R_{\theta(CS)}$ is small compared to $R_{\theta(JC)}$ and $R_{\theta(SA)}$ and we will neglect it from now on.

$$T_{junction}=T_{ambient} + (R_{\theta(JC)}+ R_{\theta(SA)})* P$$

This approach is not always valid when a different PCB design layout would be modeled by only changing the value of $R_{\theta(SA)}$, since changing the design of the board also influences the amplitude of the heat flow from junction to case, and therefore the effective value of $R_{\theta(JA)}$. To guarantee the complete transmission of the heat flow from the device, through the drain terminal, to the PCB, the device's thermal model contains both active components and RC-chains. As a consequence, the simulated temperature of the drain-node is only valid when the drain terminal is coupled to a realistic PCB model (RC Model).

Most electrical equivalent circuit representations of thermal behavior are made from RC ladder networks, either from the Foster-type (chain of paralleled RCs) or the Cauer-type (node to ground capacitances). This approach allows to model one-dimensional heat flow and is therefore well adapted for packages with 1 power semiconductor inside. However, Freescale eXtreme Switches contain 4 MOSFETs localized next to each other on the same substrate as shows the exploded view of Figure 1.

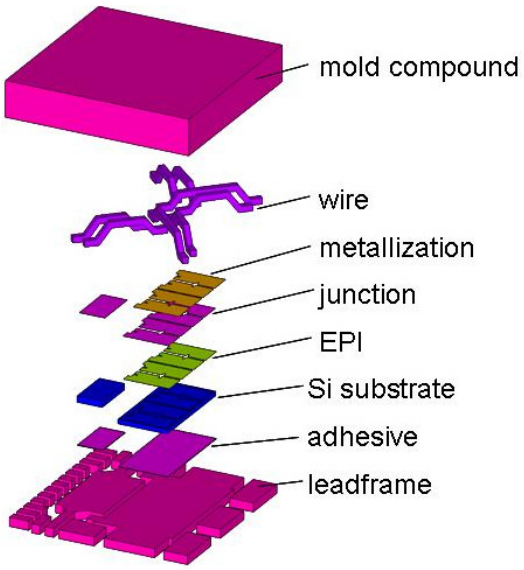

Figure 1. Exploded View of a Freescale eXtreme Switch

Consequently, additional horizontal heat flows exist, leading to mutual thermal coupling between the 4 channels. This is not easy to account for by a Cauer- or Foster type network. Starting from a Finite-Element computation, the order of the thermal heat equation (>100,000) is greatly reduced (about n=60) by application of Model Order Reduction (MOR) techniques. The MOR model is represented by a state-space equation of an order of about 60. The required amount of state variables was determined by applying an error estimation method [7]. Freescale thermal SPICE models have been extracted from the MOR-Model by an automated procedure that directly translates the state-space equation into an electrical equivalent circuit. It not only contains a passive RC ladder network, but also active sources. Thanks to this approach the temperature of any transistor junction can be predicted by simulation, regardless if it is activated or not. Experience shows that the thermal coupling between the 4 channels is not negligible, leading to a rapid heat-up of inactive channels if any other channel is powered.

However, the Freescale model of the PCB ($R_{\theta(SA)}$) is built up from a classical Foster network, since it was only intended to model a single heat propagation path from PCB to ambient.

7 Simulation of Thermal behavior with Electrical Equivalent Circuits

The proposed procedure of thermal model generation and electrical equivalent circuit simulation is demonstrated on one of Freescale's quad high-side switches for automotive applications. The 4-channel devices are housed in the thermally enhanced Power Quad Flat No Lead (PQFN) package. Two separate thermal models are available: one for the device and one for the associated PCB. The device model provides ports for conveying temperature of each of the 4 MOSFET junctions as a voltage. Device model and PCB model share a common node, the voltage of which represents the temperature of the connection point between the device's drain terminal and the underlying PCB land (see the drain pad in Figure 4). The PCB model accounts for the heat convection of the system into the ambient air.

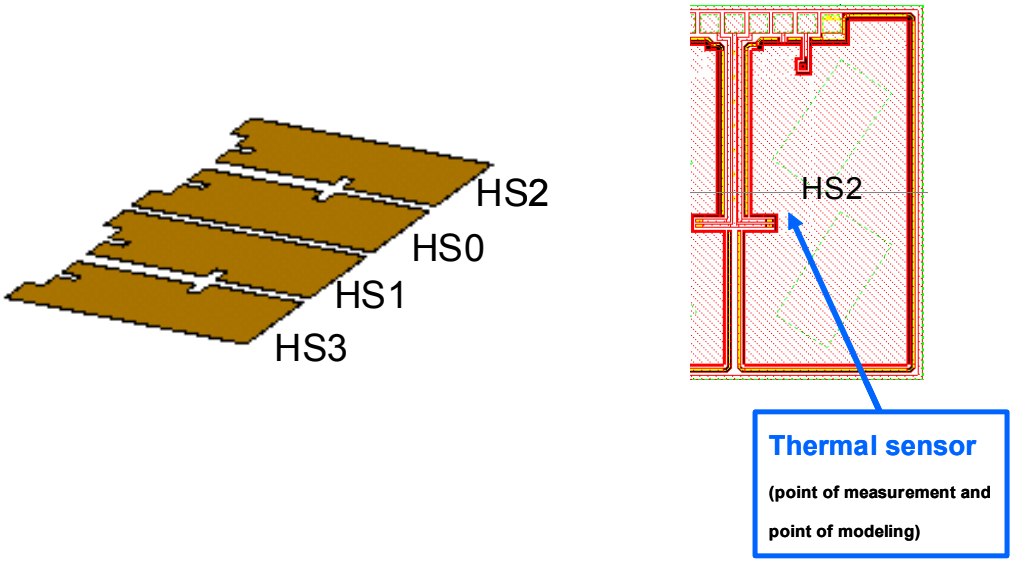

Figure 2. eXtreme Switch Power Die & Junction Temperature Reference Location

As shown in Figure 2, Channels HS3 and HS2 are located at the outer side of the package and HS1 and HS0 at the inner side of it. In order to be able to compare the computed junction temperature with the measured one, the temperature at the location of the junction's integrated temperature sensor (diode) was modeled. It is located at the end of the notch (Figure 2) made in the top metal to provide galvanic isolation from the top metal. The drain temperature was modeled at the spot indicated in Figure 3 (right picture), located on the back of the package.

The overall system model is obtained by connecting the sub circuits of the device and PCB (Figure 4). The voltage at each of the four terminals of the thermal device model represents the temperature of each channel's junction.

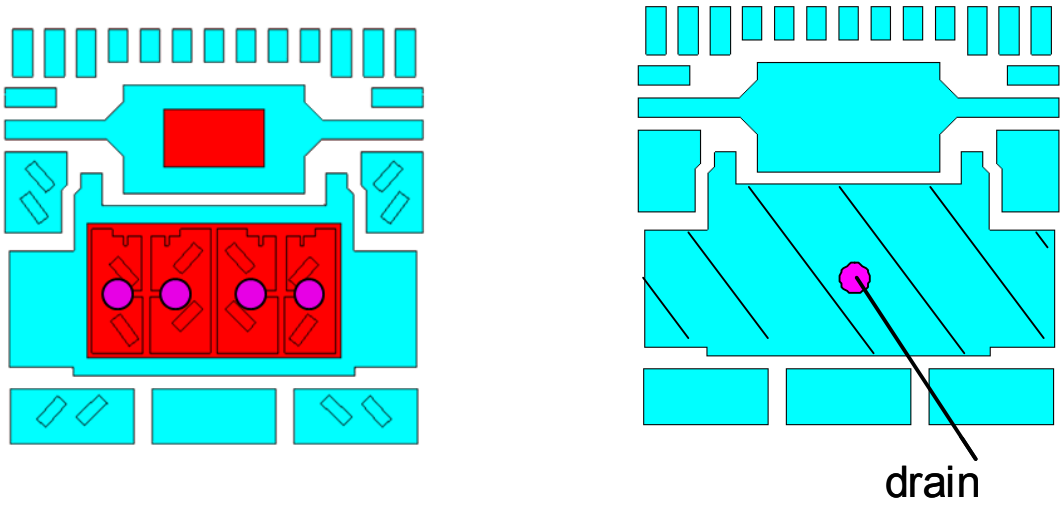

Figure 3. Location of the Temperature References on the Power Die and Drain Tab

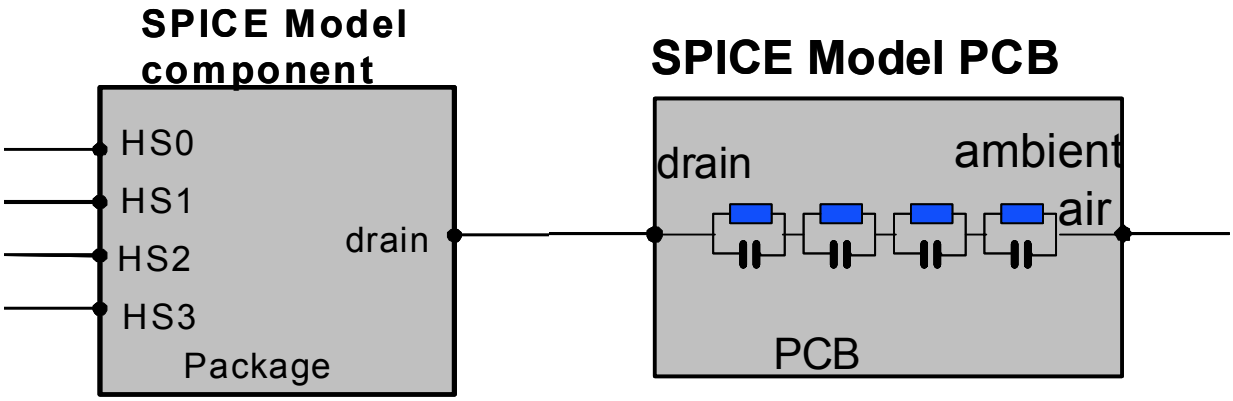

Figure 4. Representation Spice Symbols (.subckt) Of The Extreme Switch Device (left) and the PCB (right)

The output node of the device model called “drain” (Figure 4, left), represents the drain temperature and is connected to the input node of the thermal PCB model (Figure 4, right). This approach allows connecting any other PCB model to a given device model by replacing the associated SPICE PCB model (.subckt). A voltage source, the voltage of which is determined by the PCB’s ambient temperature, must be connected to the node at the right of the PCB model (Figure 4). However, for the purpose of computing the thermal impedance, it is convenient to set it to 0 (=0°C).

Two different PCB design layouts have been modeled. The models are available on the Freescale internet site (www.freescale.com) in the filename “AN4146spice.zip”. In Figure 5, the JEDEC 2S2P (2 signal /2 power layers), described in JESD51-7, is shown. The Coupon board (Figure 6) has higher thermal conductivity than the 2S2P board, and its thermal resistance is close to those usually found in typical applications. It is therefore recommended to use the thermal model of this PCB for quick evaluation of thermal performance of a particular eXtreme Switch device in a customer environment.

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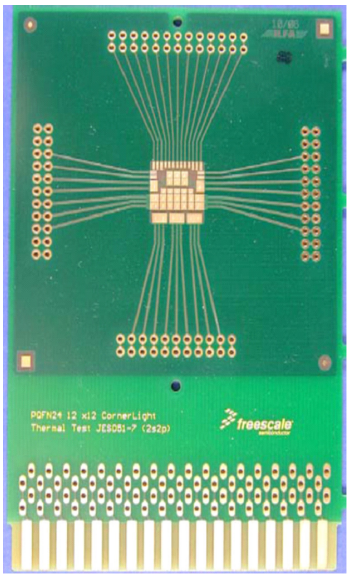

Figure 5. : Printed Circuit Board #1 (Medium Thermal Conductivity, JEDEC 2S2P)

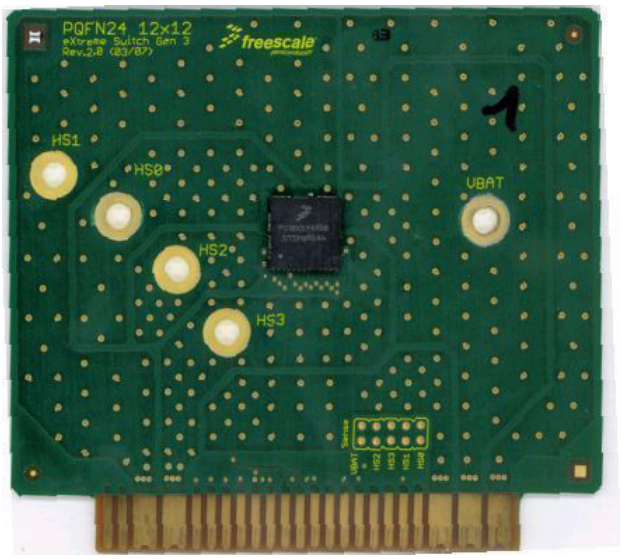

Figure 6. PCB #2 (coupon Board; High Thermal Conductivity) with eXtreme Switch Mounted

To allow the greatest user flexibility, these models provide a thermal tab (“node drain” in Figure 4). Models of any user defined thermal circuit can be connected to this thermal tab. Behavior inside the device is modeled by the device's model and behavior outside the device is modeled by the PCB's model. Some simplifying assumptions where done, in order to split the system model into two pieces at the device-to-PCB interface. They are:

1. All of the device's power passes through the thermal node. In other words the heat dissipated from the package's other surfaces is assumed to be negligible. The quality of this assumption depends on the thermal qualities of the PCB. The better the thermal characteristics, the better the assumption is.
2. The tab-to-PCB interface is assumed to be at a single, uniform temperature. The use of a single thermal node for the tab temperature mandates that there be a single temperature at that node, which spans the entire backside of the package. The temperature gradient across the thermal tab is assumed to be very small.

Heavy wire bonds connect the power die to large pads on the lead frame. The large PCB traces normally connected to those pads provide an alternate thermal path from the package to ambient. The error induced with an alternate PCB model depends on how closely the modeled PCB compares with the one used in creating the model. Consequently, the models are not recommended for PCB layouts with thermal properties that are worse than those of the (JEDEC) 2S2P PCB.

8 Model Validation

Before release, each model is verified by comparing simulation results with actual measured data. This section illustrates the process using the MC10XS3412. This device has two 10 milliohm and two 12 milliohm channels. The transient thermal impedance of each of the 4 different channels was computed by individually stimulating them with a stepped 1W power source. This emulates the effect of switching and conduction losses occurring in each channel. The associated junction temperature can be obtained by SPICE simulation, along with that of the common drain terminal, connected to the underlying PCB track. In order to validate the described model, channel HS0, situated in the middle of the device package, and channel HS2, situated more on the periphery, were stimulated by a 1W power dissipation, modeled by a stepped current source. Since thermal impedance Zth equals the ratio of the junction temperature and power (Zth=Tj/P), the observed temperature increase (Y-axis) equals thermal impedance. Figure 7 gives thermal impedance of junctions HS0/HS1 for a device on the JEDEC 2S2P board (PCB #1). The procedure was repeated for the coupon board that has better thermal properties (Figure 8).

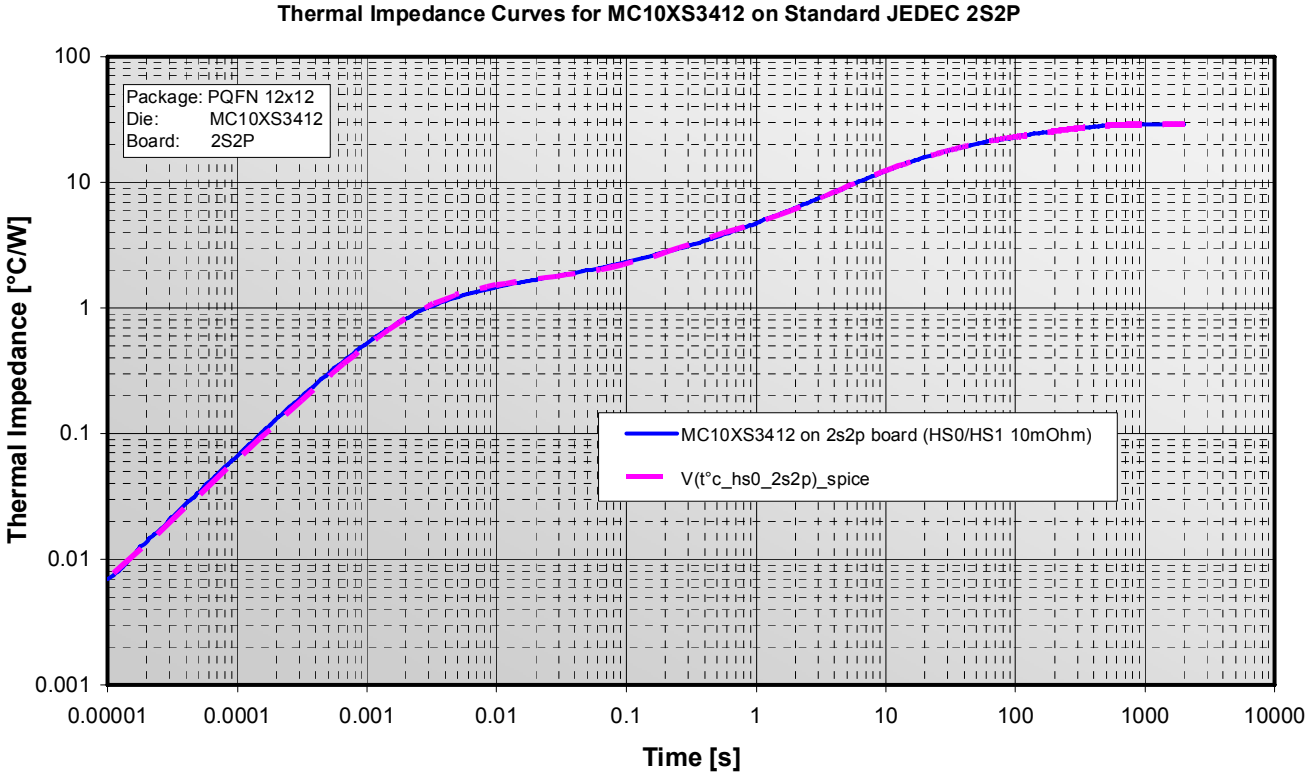

Figure 7. Measured and Simulated Thermal Impedance of the MC10XS3412 on 2S2P PCB

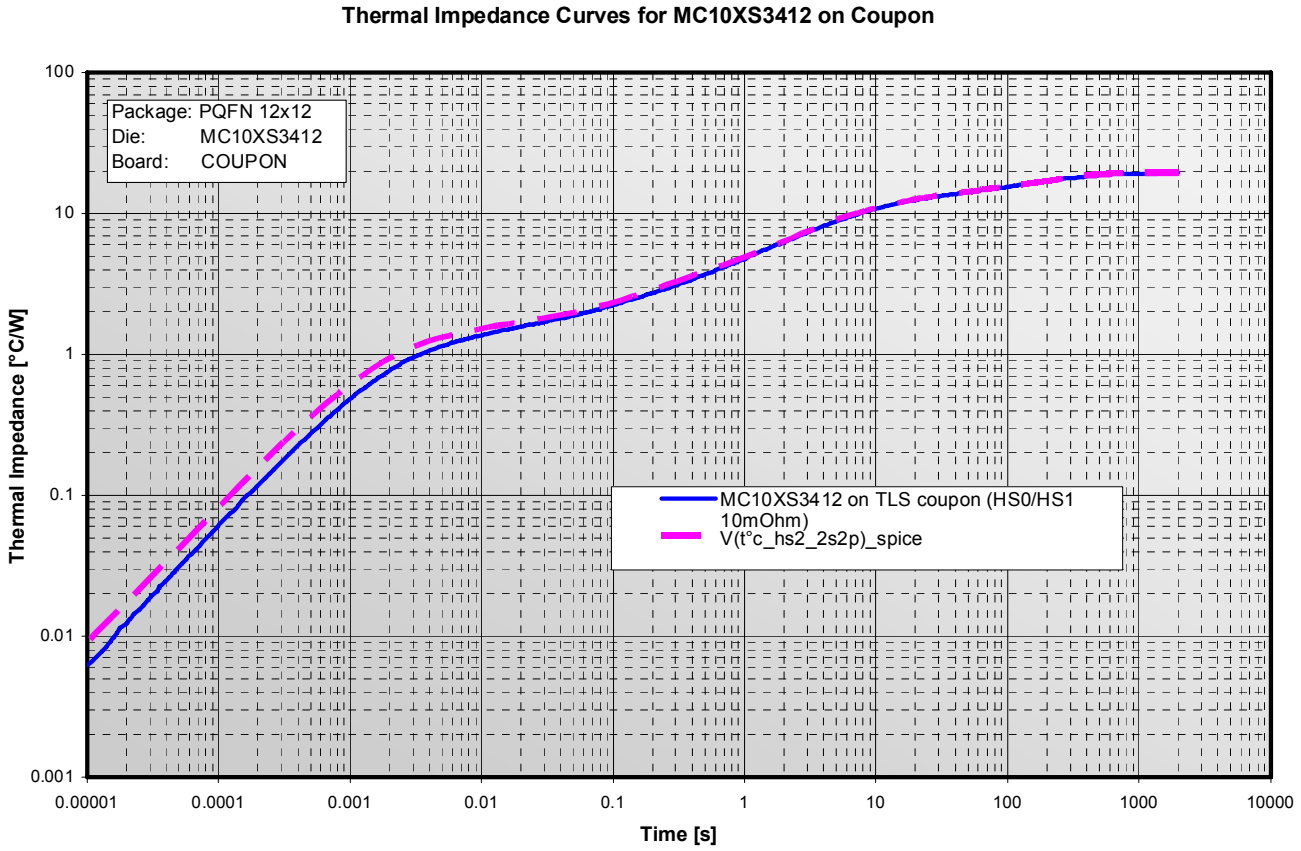

Figure 8. Measured and Simulated Thermal Impedance of the MC10XS3412 on Coupon PCB (#2)

Comparing Figure 7 and Figure 8, it can be observed that the steady-state thermal impedance of the coupon board (Fig. 8, about 19°C/W) is considerably lower than that of the 2S2P board (Figure 7, about 30°C/W). The fit between computed and measured data is good down to about 300µs, but in practice, it is recommended to use the models for thermal events with time constants > 1ms only. Moreover, the measured data were obtained at a sample rate of about 1ms and consequently any comparison at times below 1ms is invalid.

The steady-state accuracy of 4 different quad devices on the high thermal conductivity coupon and the 2S2P PCB was evaluated by comparing SPICE simulated temperature with junction temperature measurements. The results are summarized in the table in Figure 9.

Steady-State Error 1W step response - Thermal Spice Models			
		ABS(error)- coupon (%)	ABS(error)- 2S2P %
15XS3400	HS0	5.6%	3.0%
	HS1	5.6%	3.0%
	HS2	6.0%	4.5%
	HS3	6.0%	4.5%
10XS3412	HS0	<1%	<1%
	HS1	<1%	<1%
	HS2	<1%	<1%
	HS3	<1%	<1%
35XS3400	HS0	0.5%	5.5%
	HS1	0.5%	5.5%
	HS2	0.6%	7.0%
	HS3	0.6%	7.0%
10XS3435	HS0	4.6%	0.1%
	HS1	4.6%	0.1%
	HS2	4.7%	4.4%
	HS3	4.7%	4.4%

Note: ABS=absolute

Figure 9. Steady-State Error of the SPICE Thermal Models for Four Devices and Two Different PCB Layouts

The accuracy that a user will obtain when using Freescale's thermal SPICE models in a particular application will depend on a several factors among which the selected step size and algorithm, the parameters governing the numerical integration step (ABSTOL, VNTOL, CHGTOL, GMIN, PIVTOL,.), the time constants of the application the eXtreme Switch is embedded in. With a good quality PCB model and correctly tuned simulation parameters, similar results can be attained for other applications.

The Freescale models are flexible and allow users to estimate the device temperature behavior under realistic application conditions but have the following restrictions:

- Thermal conductivity of device and PCB materials changes invariant over ambient temperature
- Position of modeled junction temperature = temperature of the power die's poly silicon diode (sensor)
- Uniform heat flow out of the device's drain terminal modeled (independently of the underlying PCB)
- Model extracted at a fixed operating temperature of 150°C
- Convection or radiation (non linear over temperature) from package top is not modeled
- Only valid for exposed-pad type packages
- No upward heat flow (from PCB to device)
- Model appropriate for time constants from 1ms to steady-state

9 Using the Thermal SPICE Models with Orcad® PSPICE

In order to simulate thermal behavior of a particular eXtreme Switch device, its thermal model has to be downloaded from the Freescale web site (http://www.freescale.com).

Although the example below was given for use with Orcad® PSPICE, the models are Berkeley-SPICE compliant and may be used with any simulator. Care must be taken for selecting the right simulation parameters (step-size, algorithm, convergence criteria etc.)

The models can be found on the Freescale web site (http://www.freescale.com) under keyword search (Enter Keyword) enter **AN4146SPICE**.

Once downloaded, the model file must be put in an appropriate folder (in the example below: the file **MC10XS3412_Th.lib** was downloaded to **D:\Extreme_switches\Eswitch_models\MC10XS3412_Th.lib**). Where “D:” is the drive letter and is computer specific.

In the example below, the subvariety called MC10XS3412 is contained in that file.

In a similar way, the PCB model subvariety “coupon” is contained in folder **D:\Extreme_switches\PCB_models\PCB.lib**

** Orcad PSPICE syntax

** thermal simulation**

**Freescale 12V ”eSwitches”

.INC "D:\Extreme_switches\PCB_models\PCB.lib"

* this is the PCB library

*containing 2 PCB layouts [2s2p-PCB.lib, HPCB.lib (coupon)]

*

.INC "D:\Extreme_switches\Eswitch_models\MC10XS3412_Th.lib"

* this is a device of the device library

* (4 quad devices)

*

X1 1 2 3 4 5 MC10XS3412

* Thermal component model

*

X2 5 9 coupon

* selected PCB model

V1 9 0 DC 25

* Ambient Temperature

*

I_1 0 1 PWL 0 0 10u 1

* power step stimulus (1A of current means injection of 1W of power dissipation)

.TRAN 200n 1200 0.1

*

.probe

.OP

.END

The net list of PCB model sub circuit “coupon” is given below. It is a Foster network (paralleled RC components):

.SUBCKT COUPON N1 N2

* N1 = package drain pad *

* N2 = ambient air *

* thermal RC ladder for the Coupon (extracted from measured data) *

R1 N1 1 0.975272

C1 N1 1 0.00138072

R2 1 2 1.30195

C2 1 2 0.148587

R3 2 3 4.94709

C3 2 3 0.533366

R4 3 4 5.21198

C4 3 4 2.33565

R5 4 N2 6.45952

C5 4 N2 31.5306

.ENDS

Node N1 is an input node of the PCB model.subckt. It can be seen that the last node of the device node 5 is connected to the node of the PCB model. This is because the heat flow coming out of the device model will enter the PCB. Node 5 also is the output node of the device thermal model, since the PCB is thermally coupled to the device’s drain tab in a strong way.

An excerpt of device model subvariety “MC10XS3412” is given below:

.SUBCKT MC10XS3412 HS0 HS1 HS2 HS3 PCB

* thermal channels *

F_1_1 481 0 VF_1_1 0.

VF_1_1 1 HS0 0V

E_1_1 1 5 481 0 0.711494

..

..

..

.ENDS

It is important to notice that the mapping between channel numbers and the order of the sub circuit nodes (HS0, HS1, HS2, HS3) does not follow the order of the channels as physically present in the device package HS3, HS1, HS0, HS2).

The last node, (called PCB in the subvariety, and node 5 in the main circuit) is the interface between the models of device and PCB. Refer to **Figure 4** for circuit representation.

In the given example, a power source of 1W (modeled by a DC current source of 1A), located between nodes 0 and 1 inject power into junction HS0. No power is injected in the other junctions. Since cross-coupling between the channels has been modeled, the unpowered channels will nevertheless heat-up. The ambient temperature is set by a DC voltage source, connected to the output node (node 9) of the main circuit.

Power dissipation can be computed either off line (as in the above example), or on line, but Freescale presently does not supply electrical models of power dissipation occurring inside eXtreme Switches. However, in AN3740 (www.freescale.com), an easy-to-use method is described for computing switching and conduction losses of the four devices mentioned in this Application Note.

Simulation of the circuit will allow to compute junction temperature of all of the four junctions, along with that of the PCB land connected to the device's drain tab.

10 Conclusion

A procedure for thermal modeling & SPICE simulation of Freescale's eXtreme Switches (High Side Switches based on Power MOSFETs) on several PCBs was presented. Generation of SPICE-compatible reduced-order models, extracted from finite element models has been described. Thermal impedance of the MOSFET junctions of a PCB-mounted device were correctly predicted. This procedure provides a method to cost-optimize a PCB design layout without having to perform time consuming Finite Element Modeling (FEM) simulations. The method has many advantages:

"MODULARITY: Thanks to the separation of the thermal models of device-package and underlying PCB, the influence of the PCB layout may be evaluated very quickly. This allows a designer to use his own PCB models.

"SPEED & FUNCTIONALITY: The influence of electrical or thermal parameter variations can be evaluated by performing (parametric) SPICE simulations. Phenomena, such as the influence of an increased supply voltage or various load types on power dissipation can be simulated in a moment's notice.

Models are available on the Freescale Internet Site (www.freescale.com) by searching for **AN4146SPICE**. At the time of this writing there are models of four GenIII eXtreme Switches (MC10XS3412, MC10XS3435, MC15XS3400 and MC35XS3400).

11 References

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