Using Allegro PCB SI GXL
to make your multi-GHz serial link work
right out of the box

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Using Allegro PCB SI GXL (630) to make your Multi-GHz Serial Link work right out of the box

Abstract:

Today's Multi-GHz serial links come in many shapes and sizes. While industry-wide specifications strive to define a "box" that fits everyone's design goals, many product specs find that box too confining. And that's when design tools help out; allowing you to stretch the pre-defined limits. This session shows how Allegro PCB SI GXL and lab characterization were used to design an external Serial-ATA (SATA) configuration that literally did go "outside the box" using non-typical cables and connectors. Measured S-Parameters of the passive interconnect played a key role in accurately modeling the link and determining the frequency limits of the desired components. Behavioral MacroModels were built to represent the corners of SATA serdes devices while ensuring fast signal integrity (SI) analysis when using both time domain simulation and channel analysis. Learn how these emerging technologies were used to meet Multi-GHz product performance goals while realizing savings in both cost and schedule.

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About the Authors

Donald Telian is an independent Signal Integrity Consultant serving the electronics industry around the globe. Building on over 22 years of SI experience at Intel, Cadence, HP, and others, his recent focus has been on helping customers correctly implement today's Multi-GHz serial links and has published numerous works on the topic. Donald is widely known as the SI designer of the PCI bus and the originator of IBIS modeling and has taught SI techniques to thousands of engineers in more than 15 countries. Donald can be reached at: telian@sti.net

Hamid Kharrati graduated from University of California, San Diego, in 1991, and has worked in Engineering Design Services since then. Responsibilities have included board design, ASIC design, FPGA design, Firmware design, and project management. Hamid can be reached at: hkharrati@A2eTechnologies.com

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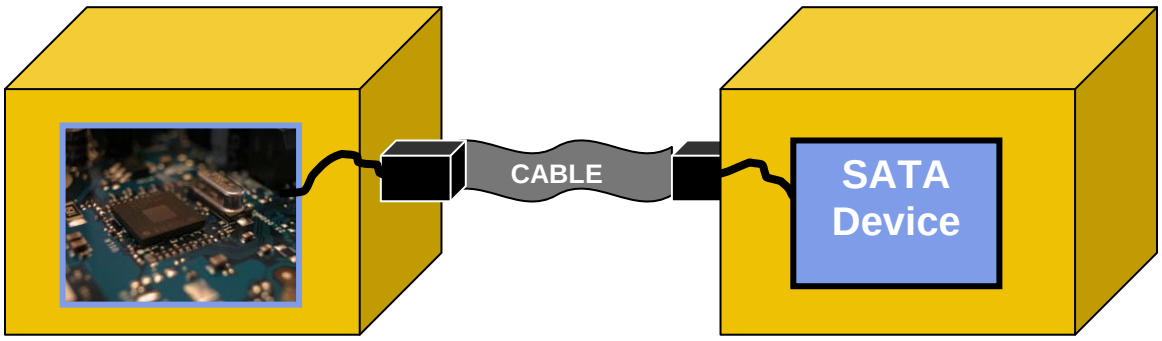
Using Allegro PCB SI GXL (630) to make your Multi-GHz serial link work right out of the box

Introduction

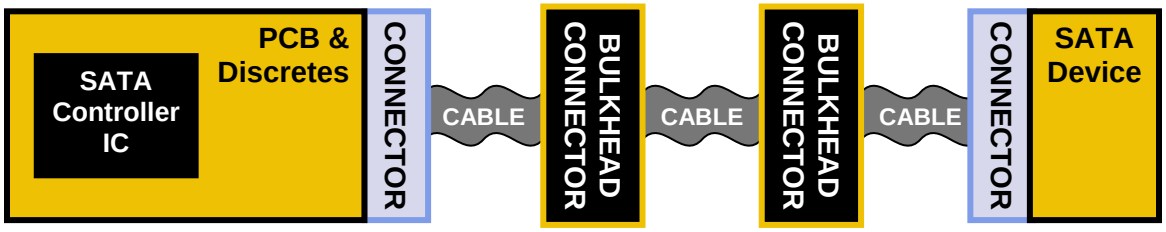
This paper details the Signal Integrity (SI) analysis of an external 1.5 Gbps SATA interface. The analysis was warranted because the high-speed interface uses non-standard connectors, cables, and under-specified silicon devices. These challenges present an excellent opportunity to use new design tools and techniques to study if the perceived limits of SATA interconnect can be stretched to meet the product's goals. As such, the paper shows how to apply design and measurement tools to guide Multi-GHz design choices and predict and quantify the proposed system's behavior.

Product Design Requirements

Per the diagram below, the product design contains a circuit board (at left) that will be mounted in an enclosure and interconnect to a Serial ATA (SATA) device in another enclosure. Heavy duty bulkhead connectors are mounted on each enclosure, causing the desired end-to-end SATA interconnect to be complex and non-standard.



Since it is necessary to connect each board to the bulkhead connectors, additional cables and connectors are needed, as shown in the following diagram.



The specifics of the SATA device at the far end (right side in the figure) are unknown, yet assumed to have PCB characteristics similar to the SATA Controller PCB at left. Between the two PCBs there are 3 cables and 4 connectors, with an overall length of roughly 35 cm (~14 inches).

The primary aim of the analysis that follows is to determine if the proposed system interconnect can function at the Gen1 SATA data rate of 1.5 Gbps, and if so with what margin.

Analysis Tools Used

The analysis was performed using the following tools:

- Cadence Allegro PCB SI 630 GXL tool suite (used for modeling and simulation, specific tools: SigXplorer, Model Integrity, and PCB SI including Channel Analysis and S-Parameter simulation)
- Agilent E5071B 4-port Network Analyzer (used to capture the S-Parameters of the prototyped cable assemblies, thus creating a model for simulation)

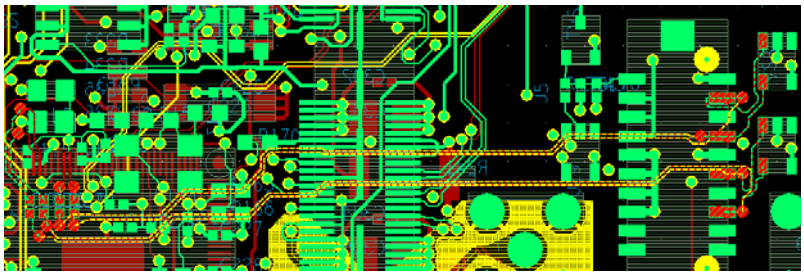
Modeling the SATA Interface

To analyze the serial link it will be necessary to create models of these elements:

1. The PCBs (including etch, vias, an discrete components)
2. The SATA Transmitters (Tx) and Receivers (Rx)
3. The 4 connectors and 3 cables that interconnect the PCBs

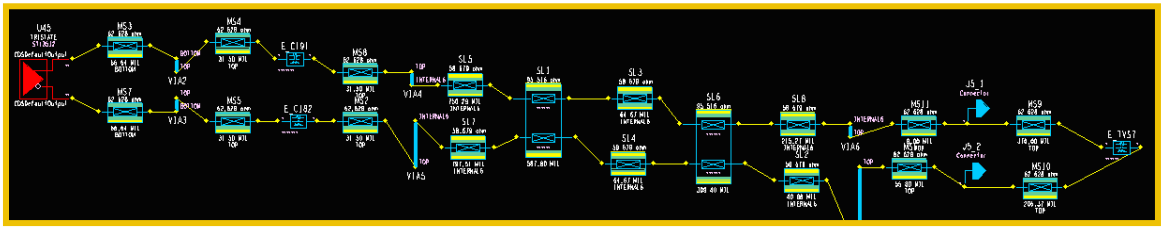
The modeling approach for each of these portions of the link is described next.

The PCBs:
Analysis began with the SATA Controller board already routed, as shown:



The SATA signals are shown highlighted in red. From the layout, note that the signals come off the IC pins (at left) through the AC capacitors and then route about 2 inches to the off-board PCB Connector connectors. ESD blocking components are farthest to the right and represent an additional load on the nets. The upper pair is the Tx signals, the lower diff-pair the Rx.

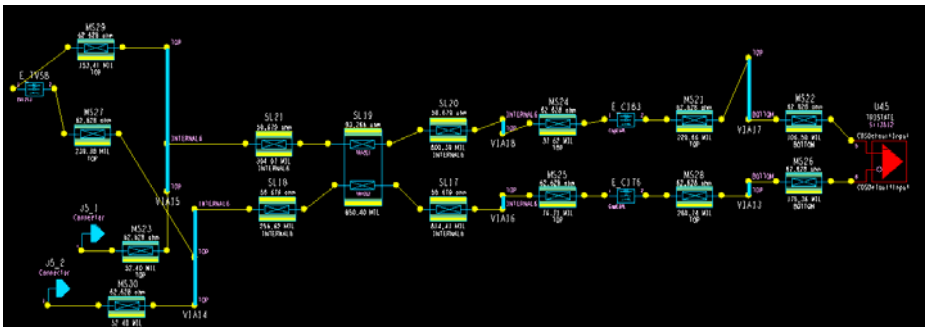
To setup the board, voltages were applied and the stackup entered. The Tx diff-pair is then extracted from the layout into the SigXp tool which allows us to easily modify the nets, swap models, etc. All SATA interface elements will be combined on this canvas for the final simulation.



In the canvas, the transmitter is shown in red at the left end. The signal then vias to the other side of the board where the AC caps are placed. The next via pair carries the signal to the inner layer where most of the trace is routed (note that the tool extracts the long parallel runs as differential stripline). The next via set carries the signal up to the PCB connector and then mismatched traces route to the ESD device.

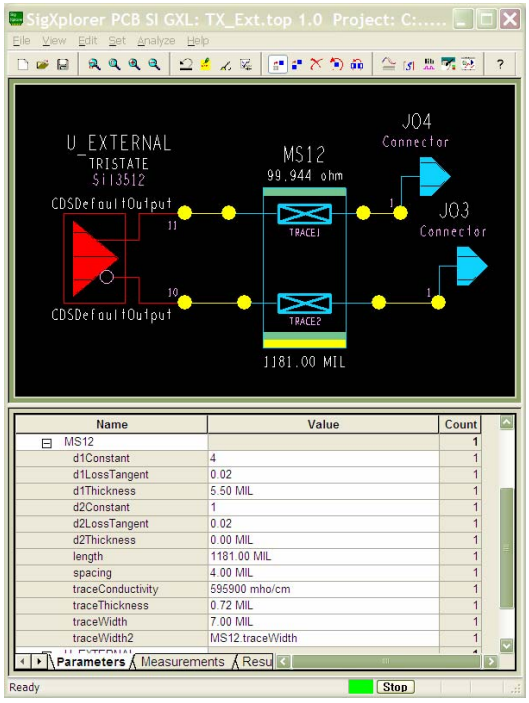
In this extraction, to save simulation time the series capacitor is modeled with only its ESR and ESL in place (no capacitance needed – 10nF is ~20mOhms at 750 MHz). Typical ESx values of 20 mOhms and a mounted inductance of 1.3nH are used. The ESD device is modeled as an Espice model using values from its datasheet and typical package parasitics.

A model of the Rx channel is extracted in a similar fashion as shown.



It was noted that the SATA diff-pairs on the Controller board could be routed with more precision (less skew), as can be seen in the various mis-matched lengths in the Tx and Rx paths. Using SigXp, it will be easy to quantify the improvement in signal quality if more careful routing is used.

The PCB trace in the far end SATA device was unknown and approximated by a 3 cm (1181 mils) trace from the connector to the device's controller IC. These models can be easily made and modified in SigXp. An example of the far end Tx path is shown next.



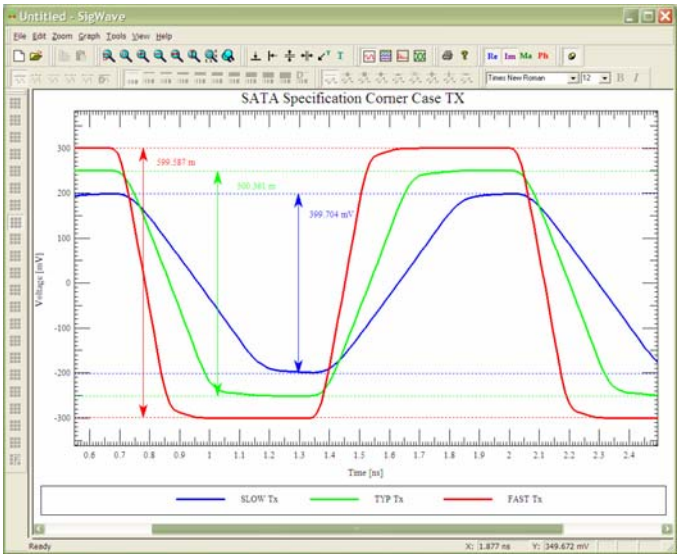
The Tx and Rx:
Since IC models were not available and the far end component was not determined, "spec" models were derived to represent typical Gen1 behaviors as well as the corners of electrical performance that might be expected per revision 2.5 of the SATA Specification. These models can be referred to as SATA MacroModels and are implemented using behavioral SPICE-like elements.

The key parameters for implementing the SATA Tx/Rx models are taken from both the SATA spec and Controller IC Datasheet, and are listed in the following Table.

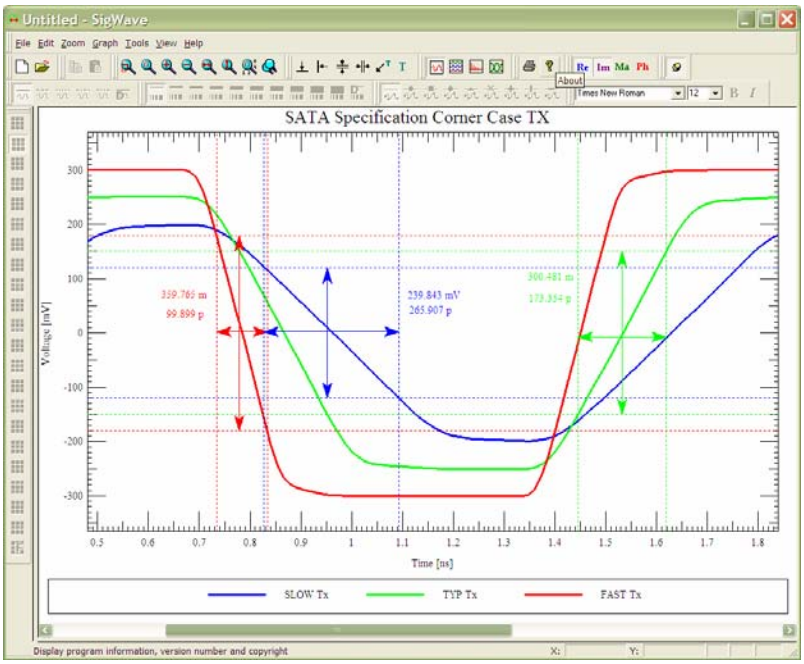
	min	typ	max	unit	notes
TX Specs					
Vp-p(diff)	400	500	600	mV	Controller IC has other options too
Pre-emph		~10%			not in specs, but typical for these comps
T_r/f	100		273	pS	20-80% rise fall times, assume at comp
ZdiffTX	85	100	115	Ohm	differential impedance
Vcm	200	300	450	mV	common-mode bias
Tx_skew			20	pS	mis-match in mid-point crossings for N&P
RX Specs					
Vp-p(diff)	325	400	600	mV	Controller IC actually has no max
T_r/f	100		273	pS	20-80% rise fall times, assume at comp
ZdiffRX	85	100	115	Ohm	differential impedance
Vcm	200	300	450	mV	common-mode bias

The Controller IC and the spec also list some Tx jitter characteristics, which will be entered into the simulation via the stimulus pattern.

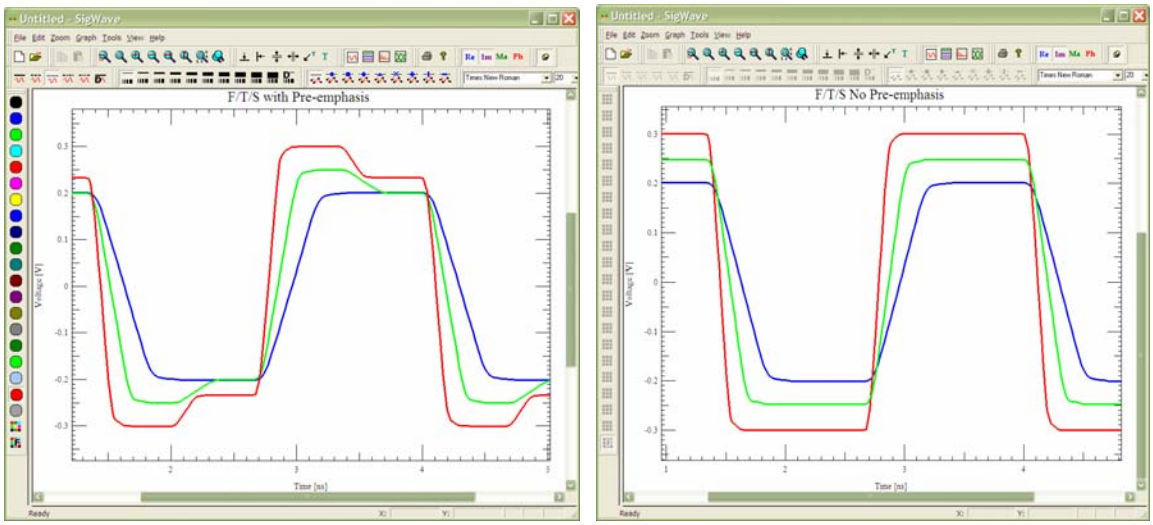
Implementing the MacroModels, the 1.5 Gbps Tx corner case model differential signals are shown driving simple 50 Ohm loads. Note the 400/500/600 mV peak-to-peak swing representing the slow/typ/fast corners.



This figure shows the 20-80% edge speeds.



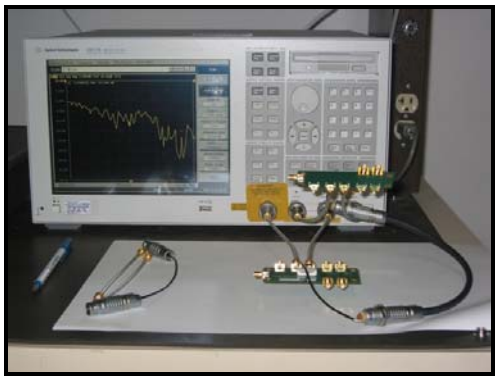
Transmit models with and without pre-emphasis were built to analyze performance against the various types of transmitters anticipated. The Tx models with ~10% pre-emphasis are shown at left. Note that pre-emphasis can only be seen when driving double-bits; the models will perform the same at the full data rate. The Tx models without pre-emphasis hold the specified levels constant (at right). Note that the slow corner is the same in both model sets in order to assess the worst case eye height.

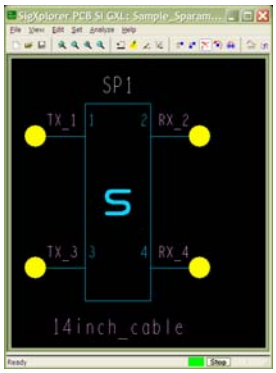


The Rx models are simpler than the Tx, and simply represent a passive load at the specified impedance. In addition, typical package models for the Tx and Rx are included.

The Cables/Connectors:
Deriving a model of numerous cables and connectors represents an interesting design choice. Since some of the cables and connectors involved were undetermined, the design team elected to prototype a couple viable options and measure their performance. This was done by extracting a 4-port end-to-end S-Parameter model of the interconnect using a Vector Network Analyzer (VNA). The extracted model is expected to be both more accurate and lest costly to derive when compared with field-solving 3D models of each sub-section of the interconnect and then cascading them together.

The behavior of each option prototyped is captured by the VNA (at left) in Touchstone format and imported into the simulator to appear as an S-Parameter Black Box model (at right).





When measuring characteristics of a system with a test fixture and a VNA, the most challenging tasks were devising the text fixture, and making consistent measurements.

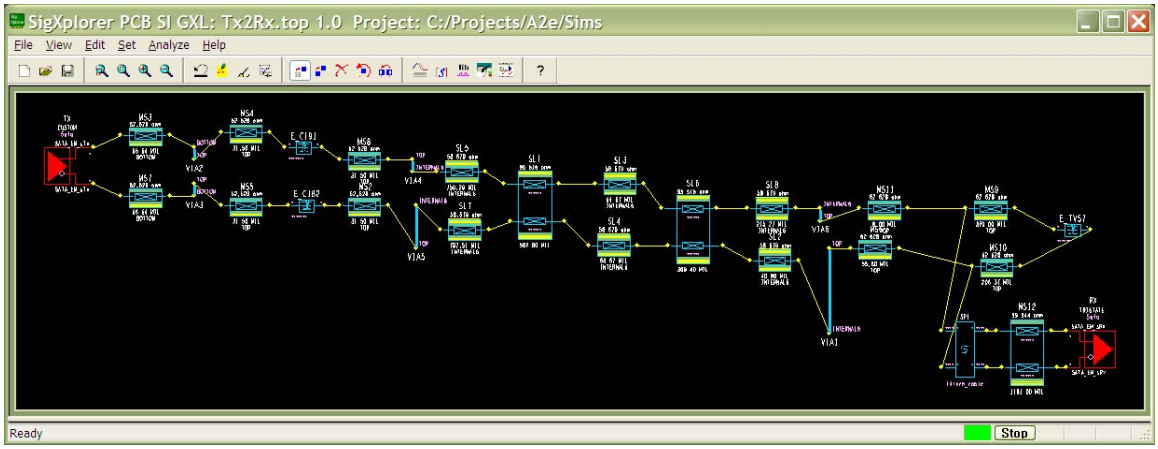
Initially we attempted to make measurements by soldering coax cables to connector pins, and running the coax cables directly into the VNA. There are at least two problems with that approach. First, the coax cables that were soldered to the connector pins could not be completely calibrated out. Attempt was made to use the same type of coax cable assembly during instrument calibration, but issues like slight cable differences and (solder) connections at the pins could not be compensated for. Second, this kind of fixture was not completely stable. Bending and moving the cables was impacting the measured cable harness characteristics.

To get around these issues, a custom PCB was designed. High quality semi-rigid coax cables and SMA connectors were used. Appropriate mating headers were used on the boards to allow various cable harnesses to be characterized with the same test fixture. The three VNA calibration terminations (open, short, and load) were designed into the custom PCB, and the exact trace lengths and shapes were used to connect the headers to the SMA connectors as those used to connect the calibration terminations to the SMA connectors. This allowed the test fixture influences to be completely taken out of the picture.

To characterize cable harnesses, the VNA instrument was first calibrated using the terminations built into the custom PCB. Then the cable harnesses were plugged into the PCB, and a 4-port measurement was made. With this text fixture, external influences were minimized. Bending cables, and touching various parts of the system (short of making direct contact with the traces that we were trying to characterize) made almost no difference in the measured characteristics.

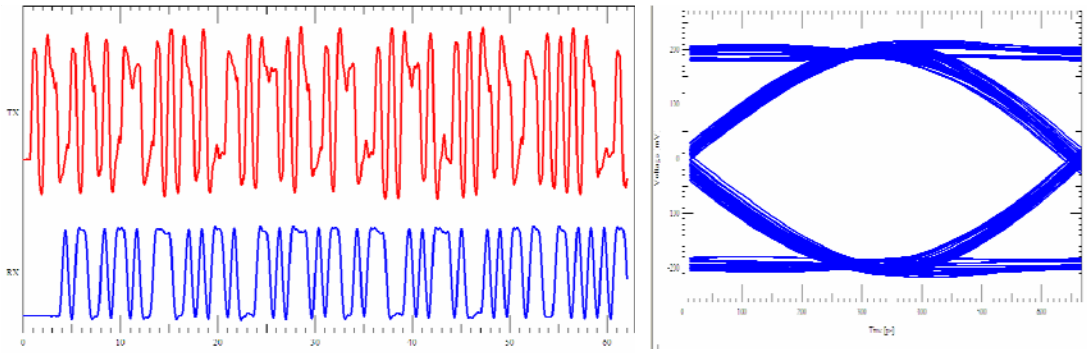
Putting it all Together

When all the models are combined, and end-to-end model of the external SATA interface can be assembled as shown.



Note the behavioral "spec" MacroModels in red on the ends of the net, the PCB route extracted from the Controller board, the S-Parameter black box model of the cable/connector assembly, and the simple 3 cm trace to the Rx at the far end in the external drive.

Using a placeholder S-parameter model and a 60nS random bit pattern with a bit of jitter, we can produce our first waveforms to confirm that the modeling process is working (left). From this simulation we can plot an eye diagram at the Rx (at right).



And with that, we're ready for corner case analysis of the two cabling/connector options.

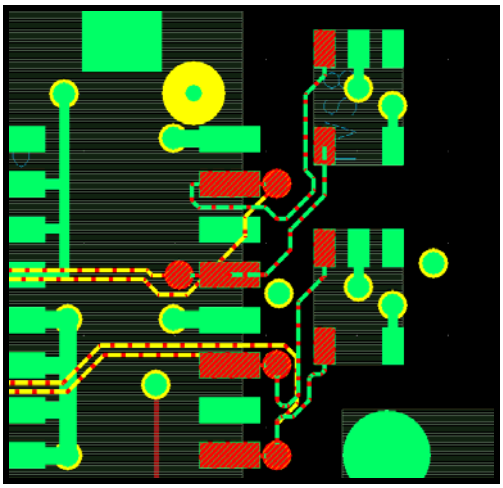
Routing Analysis

With the models assembled, we can quickly analyze the effects of a few less-than-ideal GHz routing practices noted on the differential pairs:

1. Stubs
2. Route Skew
3. Vias

The presence of these three problems can degrade the signal quality of the SATA signals. As shown in later sections, fixing these problems adds 7% more margin into the design.

Stubs
Stubs were noted in the Tx and Rx paths on the PCB in the form of extra routes to the ESD devices as shown:

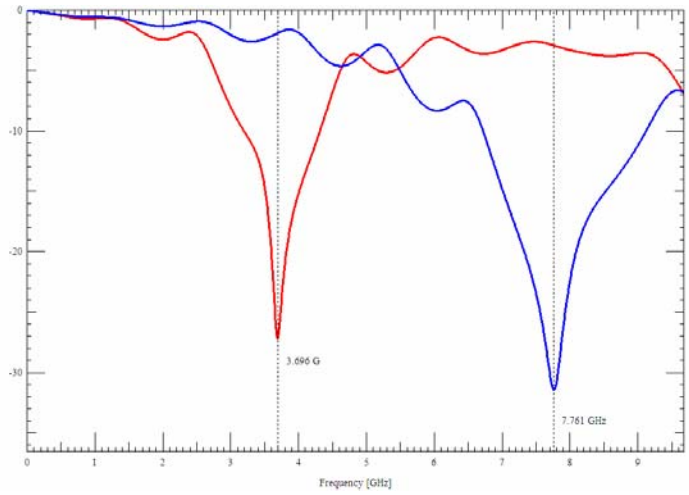


The energy in signals traveling through the nets will be divided between the connector path and the stub, causing a canceling of the signal when the stub is equal to a ¼ wavelength of the frequency. The length of stubs that will cause this problem are:

$$\text{Length\_stub} = (\tfrac{1}{4}) * (\text{Vel\_pcb/freq}) = (\tfrac{1}{4}) * (5.9 \text{ in/ns} / \text{freq})$$

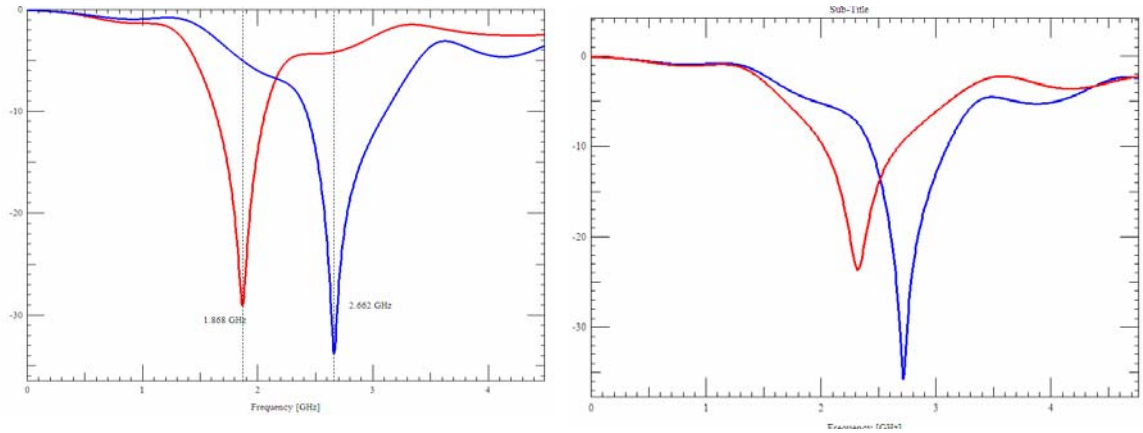
For our maximum frequency of 0.75 GHz, the equation suggests that stubs of about 2 inches will be problematic. (This agrees with Eric Bogatin's rule of thumb that approximates worst-case stubs as 3/bit-rate, or 3/1.5 = 2 inches.) Though our stubs are all less than ½ inch, the following analysis is provided to determine if it's acceptable to leave the stubs as is, or if they should be re-routed placing the ESD device in series instead of on a stub.

Plotting the frequency response without the ESD devices installed (bare stubs) we indeed see about a 30 dB loss at two frequencies related to the length of the two different stubs as shown.

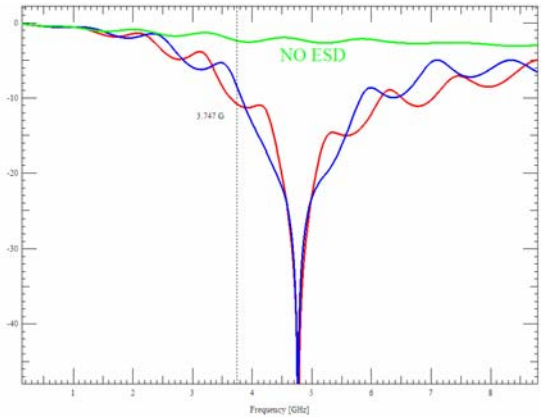


Doing the math we can derive the lengths of the stubs to be 400 mils and 190 mils, which is exactly the physical lengths of the two mismatched dangling stubs to the ESD devices.

At first, these nulled frequencies seem too high to be of concern to our 750 MHz SATA signals. However, when the ESD device model is placed into the simulation, the two frequency dips move into the range of interest either on or near our 3rd harmonic (Tx routing at left below, Rx routing at right). Due to this, slight changes in the (under-specified) parastics of the ESD devices can shift the failing frequencies within the ranges shown and cause problems.



Routing the net with the ESD device in the series path (IC->ESD->Conn) we can remove the effect of the dangling stub. Now the insertion loss only reflects the LC of the ESD package/device. This is plotted next, along with the well-behaved loss we would see with the ESD device removed and the lengths matched (in green).



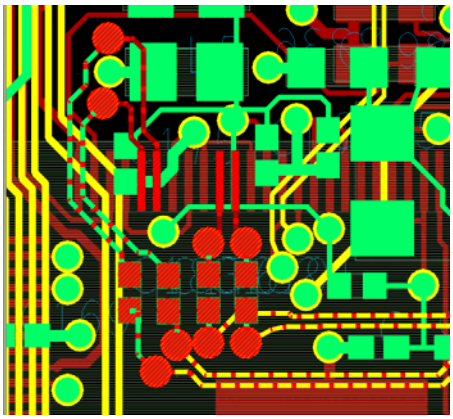
This frequency domain analysis suggests that the ESD devices should be routed in the series path to the connector rather than on a stub.

Route Skew

While the Rx pair appears well-matched in length, the Tx pair is mis-matched by 300 mils (about 1/3 of an inch or 60pS). Mis-match in differential nets converts the differential signal into a common signal. At our data rate, 60 pS represents about 1/10 of the bit time and hence 1/10th of the differential signal is lost. Since length matching is simple to do in the layout tool AND the nets should be re-routed per above, matching the pairs to within 30 mils will improve the pair's differential performance.

Vias

Note that the vias in the Tx path (pair at right, below) are much cleaner than the Rx path as the nets break out of the SATA Controller. The Rx vias can easily be placed in a manner similar to the Tx vias by moving the single via in the way. In general, it's always advisable to route differential pairs with as much symmetry as possible.

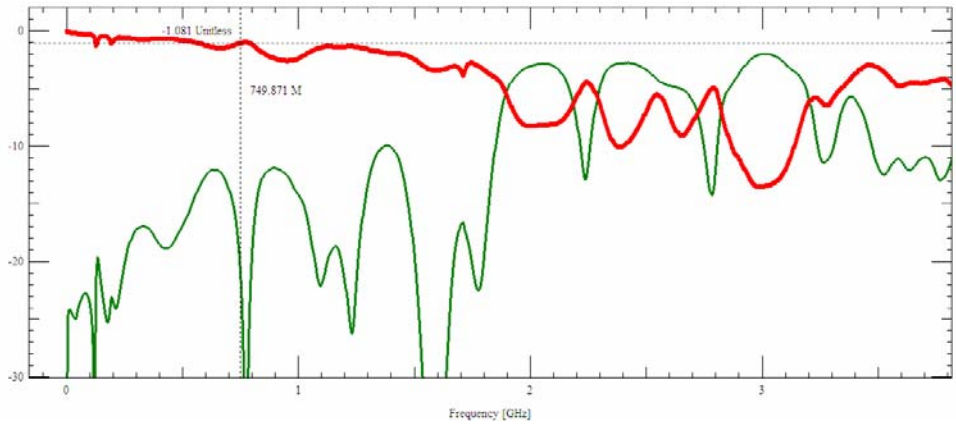


Signal Integrity Analysis

Cable Option 1: Twisted Pair

This cable was prototyped as shown and measured on the VNA to produce a model for analysis. The twisted pair lengths and path are: PCB Connector – 12cm – Bulkhead – 20cm – Bulkhead – 12cm – PCB Connector.

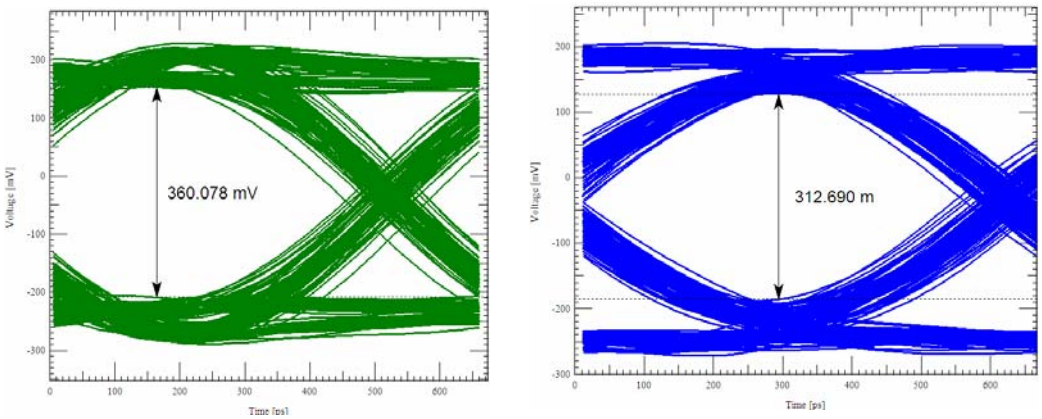
Examining the transmission (insertion) and return loss, S21 and S11 respectively, we see that this cable/connector combination exhibits very little loss at our operating frequency. As the plot shows its loss is only about 1 dB down at 750 MHz, so we expect to see about 10% signal loss through the cable. At the higher frequencies observe how the assembly's reflected return loss dominates its transmission ability even as early as 2 GHz, so it would likely function poorly at higher rates. However, the transmission loss characteristic (S21) is basically linear up to around 1.8 GHz, so we have reason to be hopeful about the SATA signal behavior at 750 MHz.



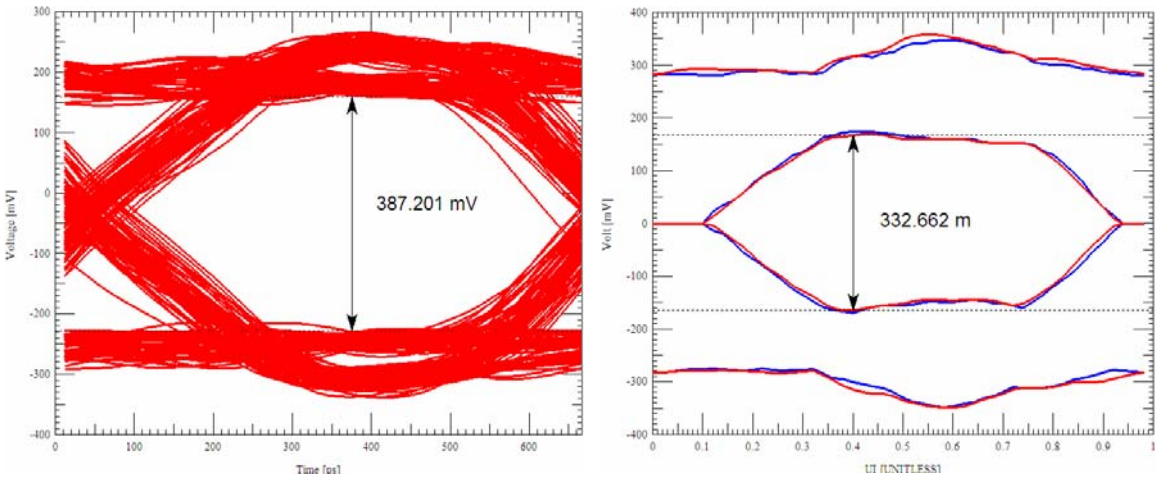
From this plot and the previous PCB plot we've seen about -1dB of loss from the cable assembly and a bit over -1 dB from the PCB route and components. As such, we might expect ~25% loss in the signal when it appears at the Rx. This means that if the Tx transmits its minimum signal of 400mV we would see around 300mV at the Rx, which is 25mV below the minimum SATA spec of 325 mV. (*Note: Assuming a Gen1m SATA device at the far end, this value becomes 240 mV, allowing 85 mV more margin in the analysis below. It may be possible to ensure the far end device meets this spec. The SATA Controller IC meets the 240 mV Gen1m spec.)*

For the simulations we'll focus mainly on the Tx path since its routing is worse than the Rx. Performance will be judged by testing the parameters that specify signal eye height and width.

Simulating the Tx pair path as routed at the SLOW corner across 250 UI with random jitter imposed (blue, at right) we see a 12mV violation of the 325 mV Gen1i SATA and the published Controller IC Rx specs. This plot agrees with the ~25% signal loss anticipated above. Simulating 250UI at the TYP corners (green, at left) yields an improved 360 mV eye height yet demonstrates both more ringing (due to the faster edges) and the dual DC band typical of pre-emphasis.

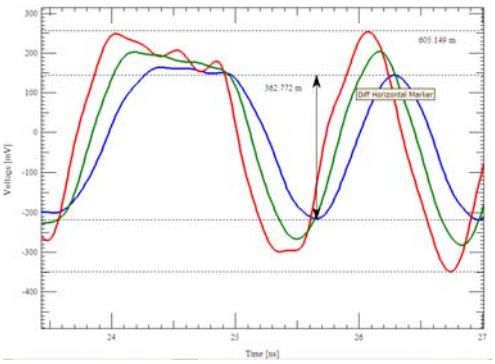


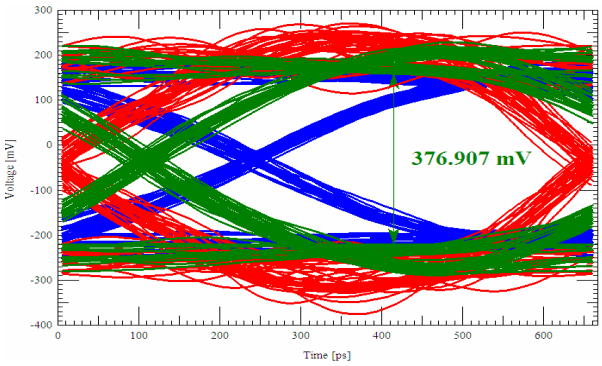
Simulating 250UI at the FAST corners (red, at left) yields 387 mV. Even more ringing can be seen in this signal, causing us to test the interconnect with longer bit streams. Using the Channel Analysis tool we can stimulate the interconnect with 10,000 (blue, at right) and 1,000,000 (red, at right) bit 8b/10b patterns. This tool draws only the outer "contour" of the eye. Note how well it matches the shape of the time domain simulation at left. In the FAST corner, the ringing causes a further collapse of the eye down to 333 mV. The slower edges of the other corners do not exhibit this type of collapse.



To further understand the signal behavior, remember that we're running "spec" corner models representing the edges of what might be seen using SATA compliant silicon devices. Looking at the corners we can see that the wider swings do press the limits of the 600 mV outer limit (see red waveform at left, FAST corner), yet the additional ringing induced by the fast edges causes the resulting eyes (at right) not to show as much

increased margin as you might expect. In the typical case, 50 mV of margin can be seen over 100 bits. (In the diagrams, red=FAST, green=TYP, blue=SLOW corners.)





In all, the system appears to perform acceptably with this cable at all corners and exhibits about a 4% violation in Gen1i eye height at the extreme SLOW corner.

SATA spec has generous jitter requirements allowing a Total jitter (Tj) of 0.6 UI (400 pS) across 250 UI, and of that 0.35 UI (233 pS) can be Deterministic jitter (Dj) contributed by the interconnect. Furthermore, this is specified at the Rx connector rather than at the Rx component. The spec defines the relationship of the jitter components as follows:

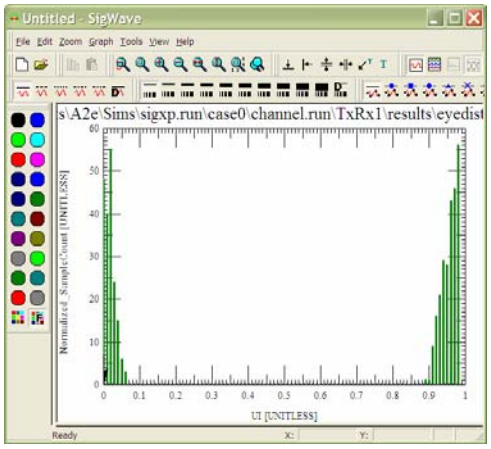
7.3.4 Jitter Budget

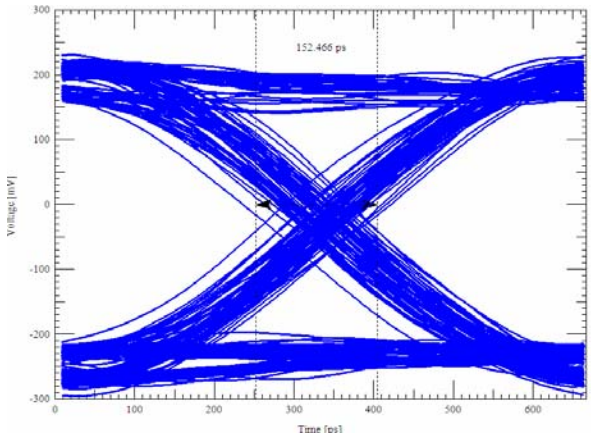
There are two types of jitter, random jitter (RJ) and deterministic jitter (DJ). Random jitter is Gaussian and unbounded. For ease, the standard deviation (RJ_σ) is multiplied by a factor which corresponds to the target BER. For a target BER = 10^{-12}, the associated multiplication factor for Serial ATA is 14.

Total jitter (TJ) is peak-to-peak and defined as:

$$TJ = (14 * RJ_\sigma) + DJ$$

A guardbanded simulation of the interconnect with 1000 UI and measured at the Rx device shows a Dj of only 0.16 UI (106 pS) as shown in the well-behaved jitter distribution at left. Tj is a bit harder to measure because it adds in Rj from the component. Adding in the one sigma Rj from the Controller IC device of 9.5 pS multiplied by 14 becomes 126 pS. The time domain simulator allows entry of this Guassian jitter value, and then the simulation of 250 UI. At right, we see a picture of the more random Tj measured across 250 UI to be about 152 pS (0.22 UI). Based on this, it appears that jitter is not a problem in this system.





Combining all measurements into a table we see decent margin against all specs except the Gen1i min eye height, as shown in the following table.

Cable 1			SIMULATED			MARGIN		
Parameter	**spec**	**units**	**min**	**typ**	**max**	**min**	**typ**	**max**
Gen1i Eye	325	mV min	312	360	333	**-13**	35	8
Gen1m Eye	240	mV min	"	"	"	72	120	93
Dj	0.35	UI max		0.16			0.19	
Tj	0.6	UI max		0.22			0.38	

If Gen1m devices are used, the margin looks much better.

If we need to allow Gen1i devices, we have a couple options to help us find more margin: (1) adapt the measured margins to the spec limits, or (2) re-simulate that corner with the suggested route changes. Let's try both.

(1) Specsmanship. Some margin can be found by noting that the 400mV minimum Tx amplitude limit *is specified at the connector, not at the silicon device.*

7.2.2.3.1 TX Differential Output Voltage

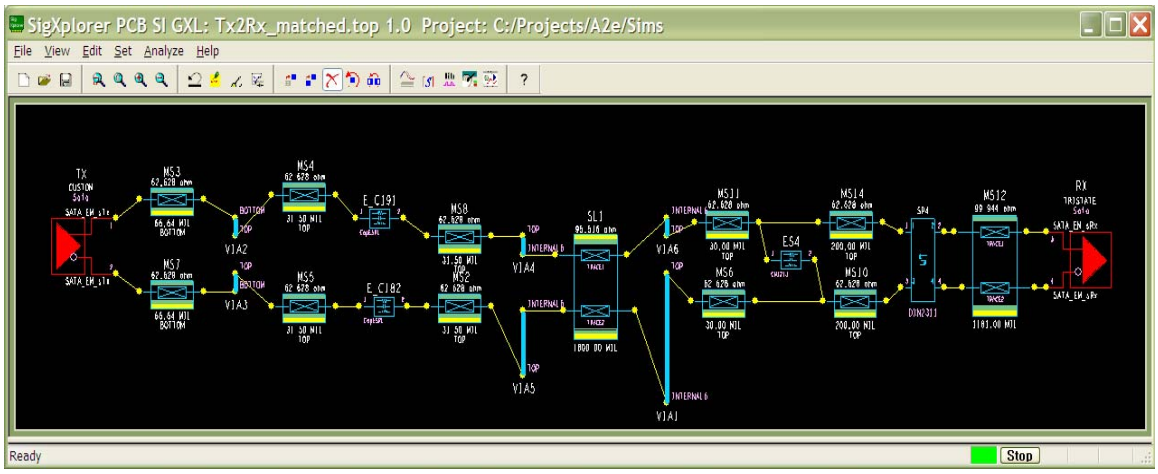
The differential voltage [(TX+) – (TX-)] measured at the Transmitter shall comply to the respective electrical specifications of section 7.2.

This is measured at mated Serial ATA connector on transmit side including any pre-emphasis.

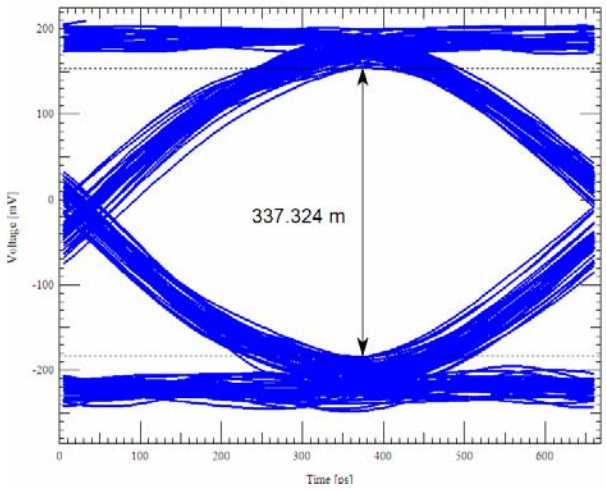
If we assume the 1+ dB lost in the PCB and vias is compensated by the transmitted device in order to meet spec then we get 10% more amplitude and the negative margin goes away. This seems reasonable, with the only hindrance being that *the SATA controller appears to spec the 400 mV at the device and not the connector*. Actually, there's no note in the spec describing its measurement point (it is difficult for an IC vendor to spec anything beyond what their component will deliver).

(2) Route changes. Incorporating the recommended routing changes yields the topology shown below in which the ESD device is now in series and the nets are better matched. The internal layer routing is now a matched 1.8" and 200 mils is allowed to route from

the ESD component to the PCB connector. All the original vias and layer changes are left intact.

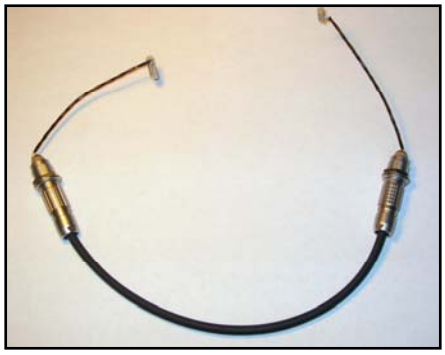


Simulating the SLOW corner shows a 7% improvement in the eye height margin, likely due to the loss improvement in the upper harmonics (as described earlier in the Route Analysis section), with the 250UI simulation now showing 337 mV.



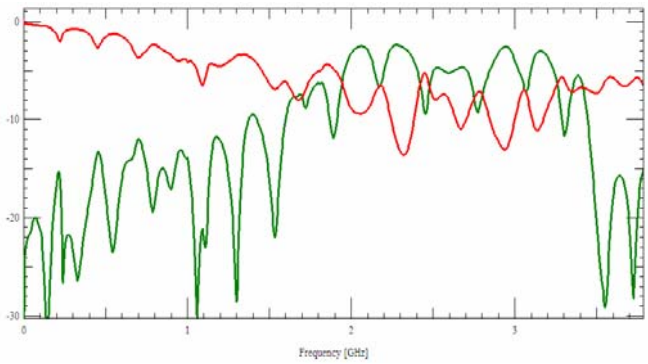
Cable 1 Conclusions. At 1.5 Gbps (750 MHz signal) this cable assembly shows acceptable loss. The interface functions decently as routed with the proposed cable, however the eye height is marginal. For better margin – and more importantly more predictable/reliable operation – use only Gen1m components and make the routing changes suggested in the Routing Analysis section.

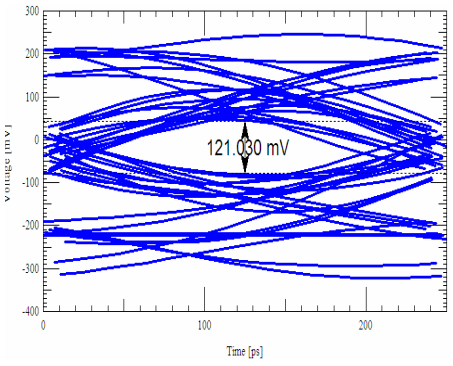
Cable Option 2: Low-Skew Cabling



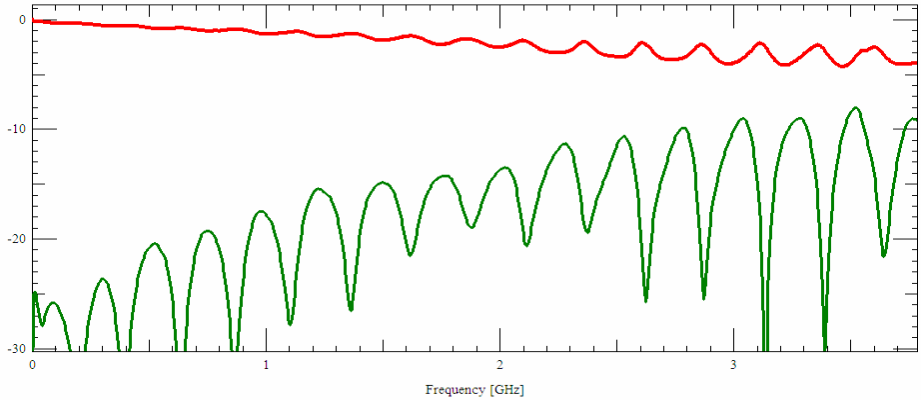
This cable used the same PCB Connector-Bulkhead connections as Option1, but was prototyped with a longer Bulkhead-Bulkhead section that used Low-Skew Cabling material. The cable lengths were: PCB Connector – 12cm – Bulkhead – 30.5cm (12") – Bulkhead – 12cm – PCB Connector.

Examining the transmission (insertion) and return loss (left below), S21 and S11 respectively, we see that this cable/connector combination is a bit longer and exhibits a bit more loss. Similar to the first cable option, at the higher frequencies this assembly's reflected return loss also dominates its transmission ability around 2 GHz. Driving just the cable at 2 GHz (at right) confirms that signal behavior becomes both erratic and exhibits quite a bit of loss.

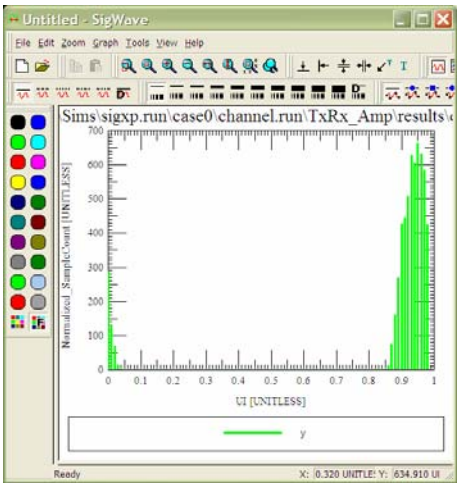


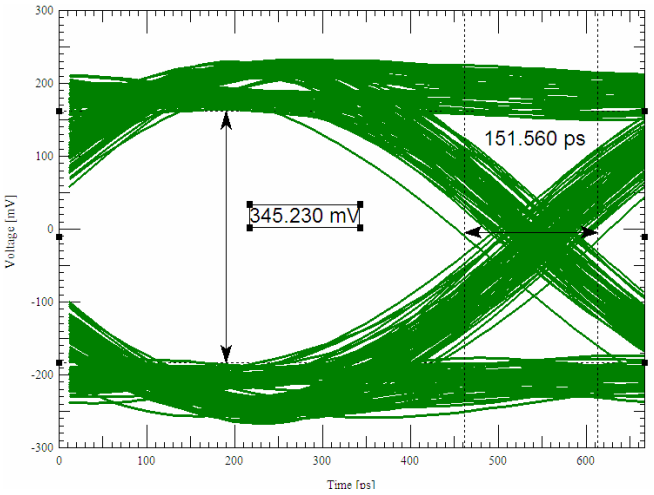


The similarity of this cable's response in the 2 to 3 GHz range to the first cable's response suggests that the S11/S21 crossovers are due to the presence of the Bulkhead connectors. Measuring a similar length of twisted pair from PCB Connector to PCB Connector (no Bulkhead connectors in the path) reveals that this is indeed the case (see plot below), suggesting that the Bulkhead connectors have a maximum operating frequency of around 1.5 GHz. It's not likely they would perform well in Gen2 SATA systems (3 Gbps, 1.5 GHz signal).

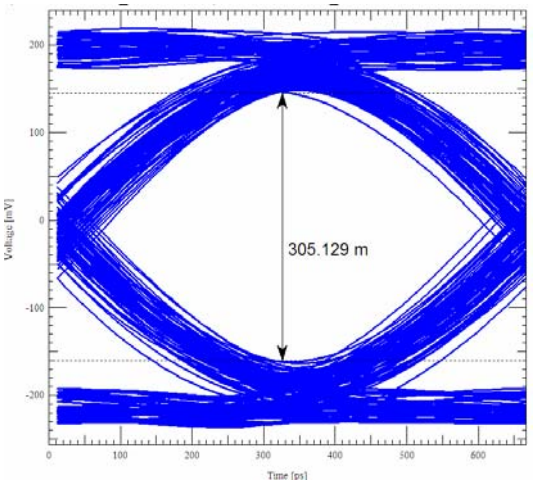


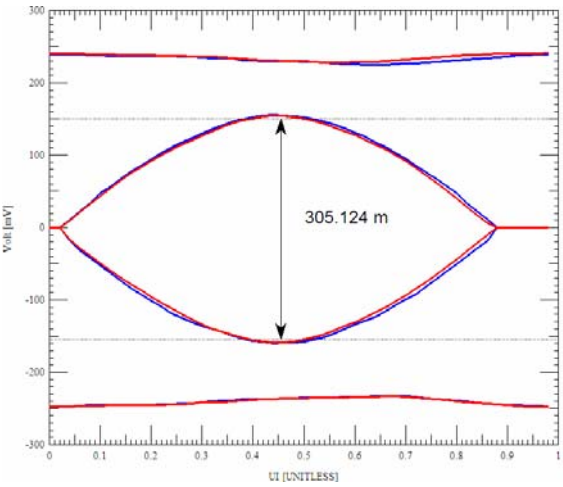
Testing Cable2's typical deterministic jitter (Dj) across 10,000 bits we find it similar to Cable1 at 0.18 UI (120pS) and demonstrating a well-behaved distribution (left). We again add the 126 pS Gaussian random jitter (Rj) across the spec's 250 UI and measure a similar total jitter (Tj) of 152 pS (0.23 UI, at right). Jitter is not expected to be a problem in this system. Due to the greater loss in Cable2, typical eye height is a bit lower than Cable1 at 345mV (also at right).





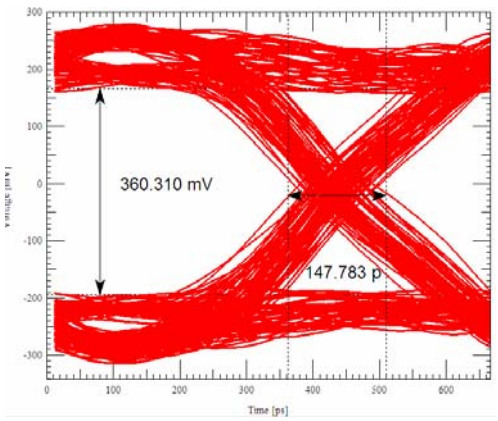
Checking the eye height at the slow corner follows the trend showing less margin due to the additional loss, with the slow corner (blue, at left) at 305 mV. As with Cable1, Channel Analysis shows that this value holds across both 10k and 1 million bits (at right) at the SLOW corner since edges are slow and ringing is minimal.

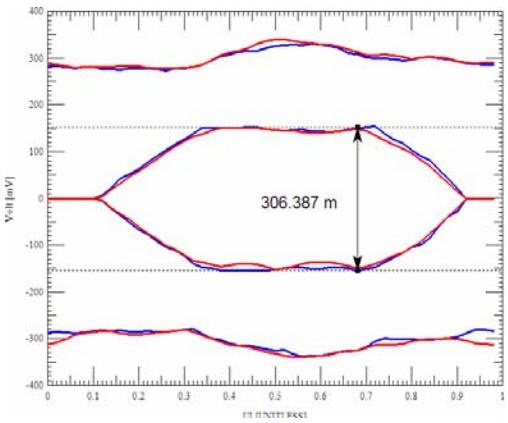




Testing the FAST corner we again see a 250UI eye height a bit lower than Cable 1 at 360mV. The wider band of ringing prompts another Channel Analysis which shows an additional eye collapse to 306 mV (at right). This is similar to the behavior of Cable 1, except this decrease causes a 19 mV violation of the Gen1i spec. This type of violation is less severe than a 250UI violation (as in the SLOW corner) since an Rx operates on a smaller group of bits (ie, it does not process a million bits at once). However, the

collapse is interesting to note, and reflects what would be seen using a long oscilloscope capture.





Rolling the results together for Cable 2, we can build the following Table.

CABLE 2			SIMULATED			MARGIN		
Parameter	**spec**	**units**	**min**	**typ**	**max**	**min**	**typ**	**max**
Gen1i Eye	325	mV min	305	345	306	**-20**	20	**-19**
Gen1m Eye	240	mV min				65	105	66
Dj	0.35	UI max		0.18			0.17	
Tj	0.6	UI max		0.23			0.37	

Cable 2 Conclusions. This longer cable shows more loss than Cable 1 and hence an additional decrease in eye height. Gen1i min eye height spec violation of 20mV was observed at the SLOW and FAST corners. The Bulkhead connectors were shown to limit performance above 1.5 GHz. Gen1m devices provide better margin for this cable, and the routing changes would improve margin as well.

Conclusions & Recommendations

Combining the results from both cables tested yields following Table.

			SIMULATED			MARGIN		
Parameter	**spec**	**units**	**min**	**typ**	**max**	**min**	**typ**	**max**
CABLE 1								
Gen1i Eye	325	mV min	312	360	333	**-13**	35	8
Gen1m Eye	240	mV min	"	"	"	72	120	93
Dj	0.35	UI max		0.16			0.19	
Tj	0.6	UI max		0.22			0.38	
CABLE 2								
Gen1i Eye	325	mV min	305	345	306	**-20**	20	**-19**
Gen1m Eye	240	mV min	"	"	"	65	105	66
Dj	0.35	UI max		0.18			0.17	
Tj	0.6	UI max		0.23			0.37	

Based on the analysis, we propose the following conclusions and recommendations:

1) The 1.5 Gbps external SATA interface can be made to work with the general lengths, components, and materials described.
2) Corner case eye heights violate SATA Gen1i specs by up to 6%, suggesting that only Gen1m devices be used.
3) Use of Gen1m components is recommended to take advantage of the relaxed receiver peak-to-peak min voltage swing of 240 mV. The controller IC meets this spec, and the component(s) used on the other end of the link should be chosen to meet this spec as well.
4) A few simple routing changes (see Routing Analysis section) should be made to eliminate stubs and match trace lengths and vias in order to gain ~7% more margin and better signal predictability.
5) SATA jitter specs are met and have good margin.
6) Cable 1 performed about 3% better than Cable 2, likely due to the longer length of Cable 2. Both cables performed similarly, with their upper frequency range response dominated by the Bulkhead connector characteristics.
7) Bulkhead connectors should not be used above SATA Gen1 speeds without further analysis. They likely will not function well for Gen2 (3 Gbps, 1.5 GHz signal).
8) Simulation with long bit streams confirms that the interface's deterministic jitter and eye height are well-bounded.

Summary

This paper has demonstrated a process for serial link design and analysis on a 1.5 Gbps SATA interface. Product requirements stretched the limits of typical SATA interconnect, warranting the need for advanced analysis. New design tools and techniques were explained and applied in order to quantify design margin. The desired interconnect was found to work acceptably given the requirements outlined in the recommendation section.