

Tel: 0118 971 1930 Email: info@alspcb.com



IR-Drop Analysis

by Chris Halford Advanced Layout Solutions Ltd chris.halford@alspcb.com

During printed circuit board design, a common request from many of our clients is that we make sure a particular connection 'can handle (n) Amps'. On the face of it this sounds like a very simple request, there are many tables and guidelines that will quickly identify the cross-sectional area of copper required. Unfortunately, these guides only provide a rule of thumb to prevent excessive current from damaging a PCB trace; they will not show that a power connection is fit for purpose.

Copper has the second lowest electrical resistance of all metals at 17 billionths of an Ohm per cubic metre. Although this would appear a very small figure, it translates to significant resistances for the thin copper foils used in printed circuit manufacture (typically 9 to 35µm thick). When current starts flowing in the copper foils that make up our power delivery networks (PDNs), this finite resistance has two detrimental impacts in the form of *IR-drop* and *increased temperature rise*.

The IR-Drop Problem

Static IR-drop describes the DC voltage that develops across a conductor as a result of its electrical resistance. This voltage is proportional to the current that flows though the conductor (V=I.R) and results in a drop in voltage available at the load devices (Vload = Vsupply – Vdrop).

Figure 1. Voltage Across Copper Conductor



The problem is made worse by the lower operating voltages common in core power supplies today. As silicon process geometries have reduced in scale over the years, so too have their operating voltages and noise margins. However, the power demands of many devices have not scaled accordingly and so Can your PCB traces and planes 'handle' your power supply requirements? IR-Drop analysis ensures that they can...

power-hungry devices, whilst operating at low voltage, can draw considerable current. For a given power plane, a larger current will result in a greater IR-drop voltage, and hence a lower voltage available at the load. Such voltage drops can cause major problems when distributing power across a PCB; when the drop becomes excessive the voltage at the load may fail to meet necessary device specifications.

Figure 2. IR-Drop & Tolerance vs. VDD



Consider a 10W nominal load device that is being supplied via a 15m Ω PDN (component pads, viabarrel plating, plane shapes, etc). In a 3.3V system the DC voltage drop would only be 45mV (-1.4%), and would generally be an acceptable loss. However, the loss increases dramatically for lower voltage devices of the same power dissipation. As Figure 2 illustrates, at 1.2V the loss is nearly -10% of supply and certainly out of spec, and at 1.0V it has dropped to -14%. A resistance of 15m Ω is excessively bad for a PDN, but clearly lower

voltage systems are far more sensitive to the quality of the power connections designed into the board. **The Temperature Rise Problem**

We have seen that the flow of current causes a voltage to be established across the power connections. This resistive power loss (I^2R) is dissipated by the conductors in the form of heat, and with significant resistances and/or very high currents, can be considerable. Furthermore, where connections are at their minimum width and current densities are highest the temperature can reach seriously high levels, damaging the laminate and ultimately melting the copper foil.

Surely the Answer is Simple?

One way to ensure that IR-drop and temperature rise problems are avoided is to use wide planes of thick copper for all power connections. Whilst this might be true, there are always trade-offs in printed circuit board design. Routing space is usually at a premium and unnecessarily large power connections will inevitably compromise the design in other ways. Using thick copper can have its drawbacks too, as it is incompatible with fine trace widths used on 'mixed' signal/power layers.

Although the calculations required to estimate IRdrop are not complex, actually carrying out the task manually is daunting. The reason for this is that the copper shapes usually end up being very complicated. In both plated-through-hole and microvia technology, holes are formed around the vias as they pass through the power planes. This 'Swiss cheese' effect, shown in Figure 3, can seriously compromise the performance of a power plane, and makes manual calculation very awkward.

Figure 3. 'Swiss cheese' Effect on Plane Shape



When power connections switch layers, or use multiple layers, then the problem is complicated further. The number, size and plating thickness of vias that connect the conductors and planes together must all be taken into account. This is an important requirement as a weakness in many power delivery paths is the connection from the high-power components' pads on the outer layers to the internal power planes beneath. The result: it is almost impossible to manually calculate the resistances in the resulting power structure, illustrated in Figure 4 below.

Figure 4. Voltage Drop Across Foils and Vias



The Solution...

At Advanced Layout Solutions Ltd we use the IR-drop analysis tools built into Allegro PCB SITM to verify that your power paths are within spec.

During the design process the Allegro tools are already aware of the copper thicknesses employed on the individual conductor layers and also the lengths of interconnecting vias. The tools assume standard via plating thicknesses (as defined in the IPC specifications) but can accommodate custom values on a via-type basis. This information, in combination with the layer artwork, allows the tool to completely model the power connections in three dimensions.

The user enters source and sink current information on a per-device or per-pin basis and then runs an analysis on all nets of concern.

The analysis breaks down the copper shapes into a mesh of small cells. The size of these mesh cells is critical to ensure that the copper shapes are resolved with sufficient accuracy. With a suitably fine mesh setting the copper shape will be modelled complete with voids (holes) and fine shape detail. Figure 5 shows the same copper shape 'meshed' using progressively finer mesh settings. As the mesh cell size decreases, more detail can be seen in the shape allowing voids in the plane shapes to be included in the simulations.

Once these shapes are analysed, the Allegro tools report three key pieces of information: **voltage drop**, **temperature rise** and **current density**. The latter makes for interesting viewing, but in reality our concerns lie primarily with the former two: Voltage drop - when maximum current is drawn, is the voltage at the load within specification? Temperature rise – is the power path capable of delivering the maximum supply current without

Figure 5. A Progressively Finer Mesh Size Reveals Detail in Plane Shapes.

excessive temperature rise?



The core supply pins on a BGA tend to be located near the centre of the array. This arrangement is shown in Figure 6, in which the voltage across a plane shape is shown as a series of isocontours. There is a small, gradual drop in voltage between the blue (voltage source) and green areas of the plane. However, a significant drop in voltage exists between the green and red area as the current has to traverse the 'Swiss cheese' voids in order to reach the power balls at the centre of the package. This is a very common problem indeed, especially on low layer-count BGA designs that use multiple supply voltages.

Figure 6. Voltage Drop on Plane Shape



As Figure 6 illustrates, IR-drop can be very clearly displayed, depicted as a gradual change in colour (voltage) across an area of plane. Switching the display to 'temperature rise' reveals local pockets of high current-density, in which there exists a risk of excessive heating. Figure 7 shows exactly this scenario, with increased current density between the BGA voids shown in cyan.

Figure 7. Current Density in 'Swiss Cheese'



The temperature analysis is particularly useful for ensuring that a sufficient number of parallel vias have been used in power paths. The source connection in Figure 8 (shown in red) is a single via which is grossly over-heated by the current demand of the processor.

Figure 8. Temperature Contours on Plane Shape



Summary and Conclusion

The new IR-drop analysis tools built into **Allegro PCB SI™** v16.x are proving to be an extremely valuable addition to our PCB design and signal integrity toolset. The tools highlight potential problems in power delivery paths, providing visibility for both IR-drop and 'hot-spotting' issues. The tools provide a basis for correctly designing high-current power connections by quantifying the amount of voltage drop and temperature rise that are to be expected, thus deterring the overengineering that often accompanies uncertainty.

► Remember that designing a PCB conductor to carry large currents is more involved than just choosing a particular cross-section of copper. Where high currents flow, there is always a temperature rise that must be considered. Over a distance of copper there is also a static voltage drop that must be accounted for in the system power supply budget. Finally, bear in mind that the entire budget cannot be eaten up by static IR-drop alone, as AC voltage fluctuations must also be allowed for.

If you would like more information on PCB design or signal integrity analysis, please contact:

Advanced Layout Solutions Ltd

Fronds Park, Frouds Lane, Aldermaston, Reading, Berkshire RG7 4LH, UK Tel: +44 (0) 118 971 1930 Fax: +44 (0) 118 971 1931 mailto:info@alspcb.com http://www.alspcb.com ©2009 Advanced Layout Solutions Ltd

Allegro PCB SI™, SPECCTRAQuest™ and Allegro™ are trademarks of Cadence Design Systems, Inc



