Modeling Analog Circuits with Routed Interconnect using AMS and Allegro SI

Application Note
Product Version 15.7
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Contents

Overview

The purpose of this application note is to describe how to extract routed transmission line parasitics from Allegro SI and include them in an Allegro AMS simulation.

Including Routed Interconnect in AMS Simulations

Scope

The scope of this application note is focused only on obtaining t-line values from Allegro SI and them including t-line values in an AMS simulation. It's assumed the reader has knowledge of Allegro PCB, Allegro SI and Allegro AMS.

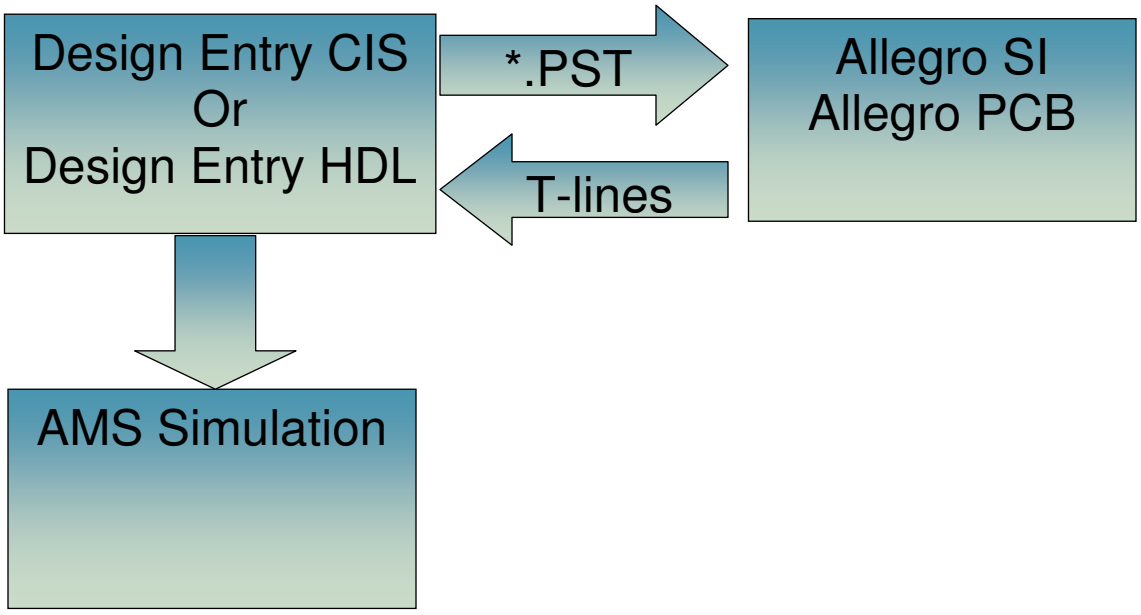
Acronyms

Allegro Design Entry CIS = DE-CIS
Allegro Design Entry HDL =DE-HDL
Allegro AMS=Allegro Analog Mixed Signal= AMS
Allegro PCB Editor=Allegro
Allegro Signal Integrity=Allegro SI
Signal Explorer=SigXP
T-line=Routed Interconnect on PCB

Flowchart

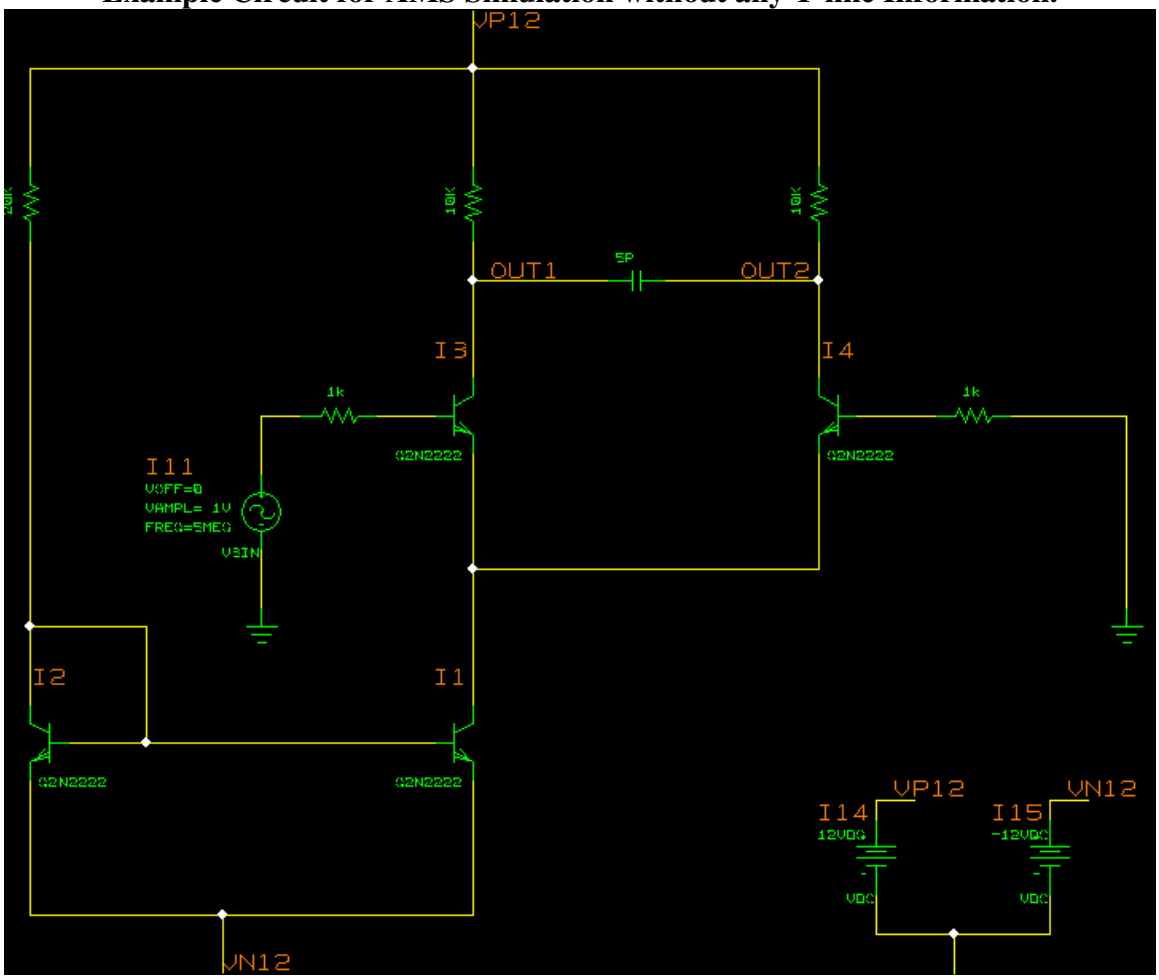
The process to include routed t-line values in an AMS simulation is:

1. Netlist the DE-CIS or DE-HDL AMS design to Allegro using *.pst flow
2. Define the materials and stackup
3. Place and route the board
4. Extract the desired t-line values.
5. Include the t-line values in the AMS Pspice netlist
6. Run the AMS simulation



Example AMS Circuit

Example Circuit for AMS Simulation without any T-line Information.



To include routed Tline parameters in this circuits AMS simulation the circuit must be netlisted into Allegro PCB and routed. The stackup and materials of the Allegro PCB database are taken into account when deriving T-line parasitics.

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Extracting Transmission Line Parameters in Allegro SI

Once the circuit is placed in routed in Allegro PCB there are 3 methods to obtain transmission line values.

1. Display Parasitics
2. Parasitics Report using the Allegro SI Probe function
3. Simulating in SigXP to create spice models for T-lines

Display Parasitics

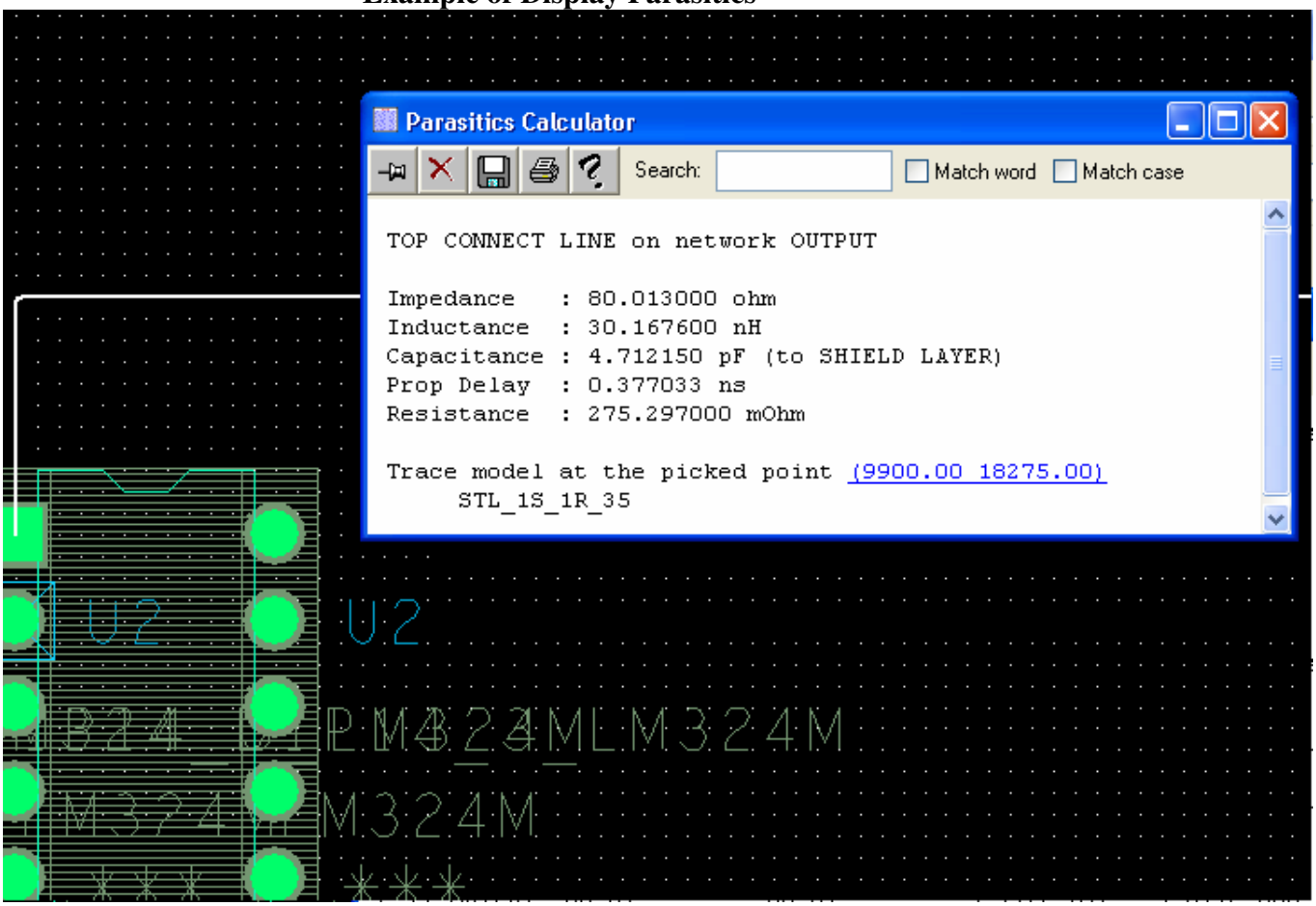
In Allegro SI Display Parasitics can be used to obtain information about a routed trace. These values are calculated for DC. For 2 pin nets L and R and C w.r.t shield layer are reported. For nets with 3 or more pins only C and impedance is reported. The self capacitance data shown in Parasitics is obtained from an empirical formula. This empirical formula is a single line model. The accuracy is good for standard single microstrip and single striplines within certain geometry ranges. The mutual capacitance in Parasitics is based on very simple "parallel plates waveguide" models, assumes homogeneous dielectric layers in between (no vias) and assumes that the distance between the plates is much smaller than the plates themselves. This method is good for fast estimates.

Procedure

1. Select the trace, from RMB choose display parasitics properties on the selection.
2. The Parasitic values for the selection will be displayed.

Including Routed Interconnect in AMS Simulations

Example of Display Parasitics



Parasitics Report using Probe

Allegro SI offers a probe function from which a parasitic report can be generated

- A report can be generated including all the nets on the board in one step.
- The net capacitance parasitic data of the net or xnet (including vias) will be shown in this report. Net capacitance is interconnect self capacitance including traces and vias. This data has been extracted from the field solver with rigorous solution. Net inductance and resistance is reported for 2 pins net only

Procedure

1. In Allegro SI under choose probe.
2. Either select the net(s) or use the browser button to choose from a list of nets
3. All nets of interest can be selected
4. Select the reports button
5. Under report types check Parasitics report.

This will result in a text based report listing the parasitics of the nets selected.

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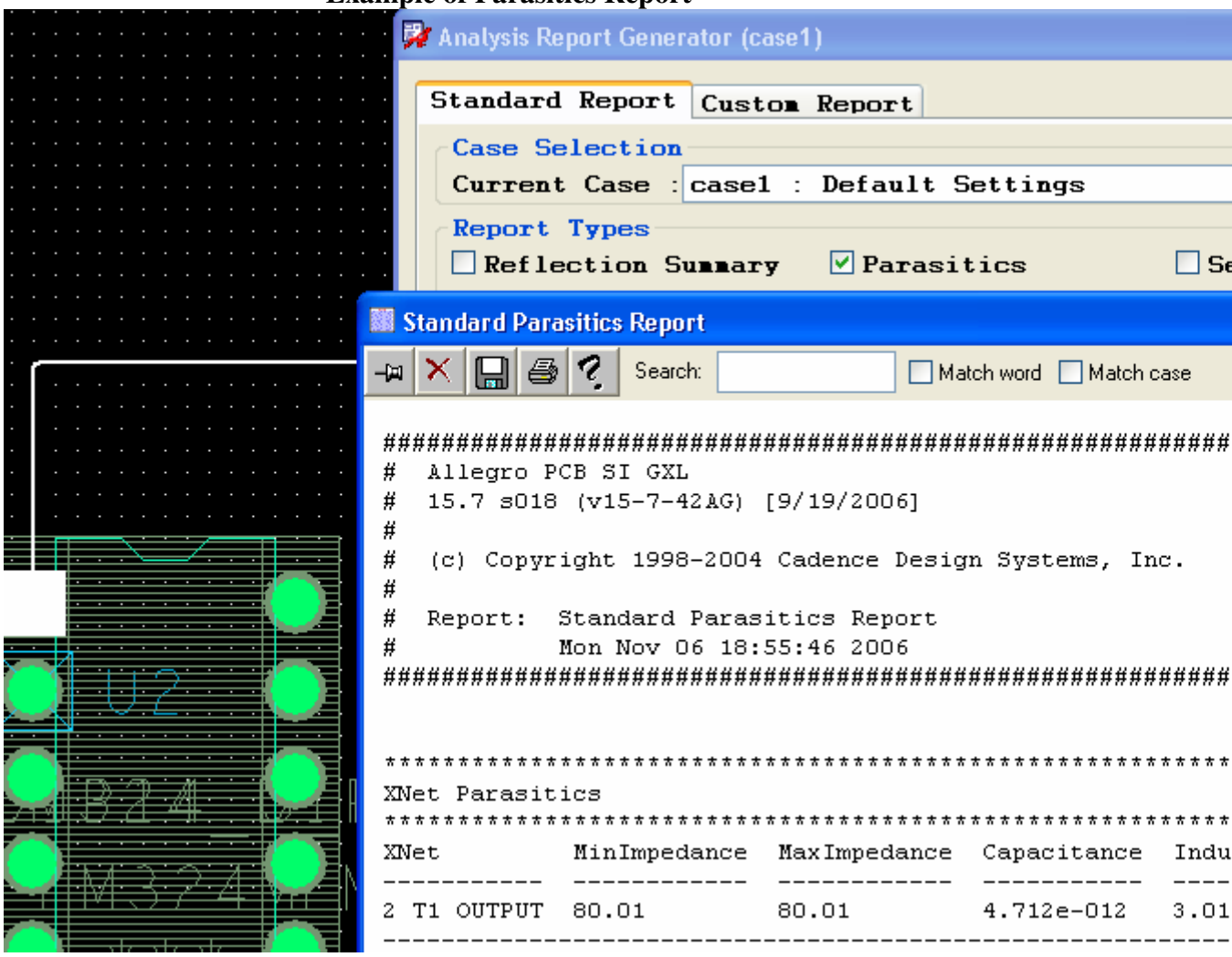
Example of Parasitics Report



Including T-line Parameters in the AMS Simulation

After obtaining the T-line values from view parasitics or the probe report they need to be included in the netlist for the AMS simulator. There are 2 approaches to accomplishing this.

1. Adding Tline symbols to the schematic circuit with the t-line properties obtained from Allegro SI
2. Editing the spice netlist to include the t-line values. This could be automated by using a program.

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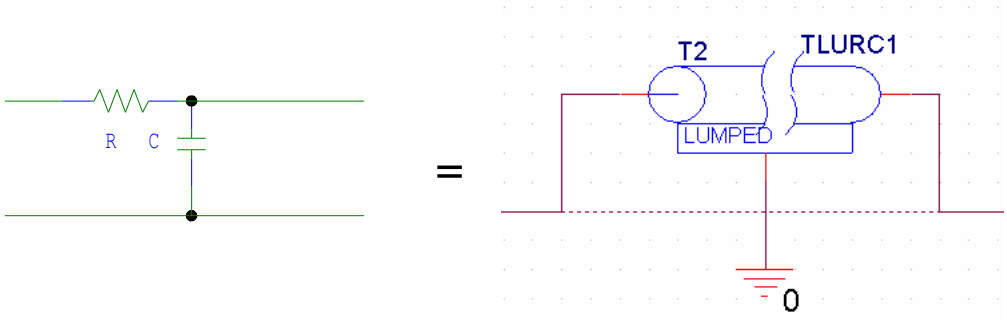
Adding T-line symbols to the schematic

Procedure

1. Insert the appropriate t-line symbol into the net on the schematic
2. Set the properties of the t-line symbol to the t-line values obtained from Allegro-SI
3. Regenerate the spice netlist and re-run the simulation.

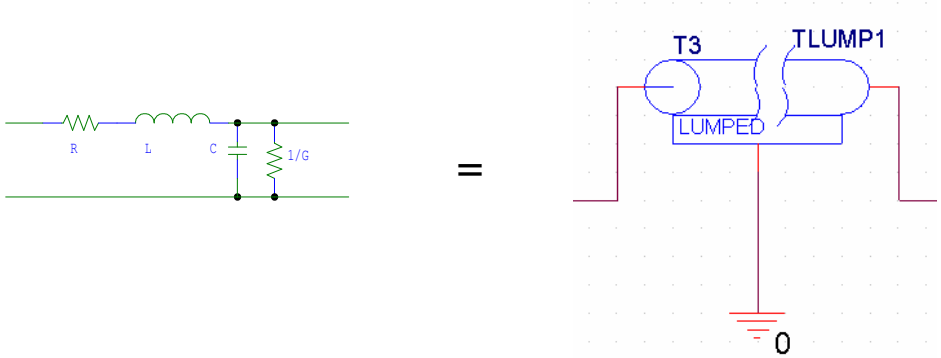
The t-line parts are found in the library tline.olb located in $CHDL_LIB_INST_DIR for DE-HDL or in $CDSROOT/tools/capture/library/pspice for DE-CIS
There are 2 types of t-line parts

1. Lumped RC models (TLURCx)
An RC line is a special case where R/L is large (or the series inductance is small). The simplest model for an RC line is a capacitor and a resistor.



Parameters R, C, LENGTH

2. Lumped RLCG models (TLUMPx)
When ωL/R>>1 or ωC/G>>1, the per unit length inductance should be included in the lumped model.



Parameters R, L, C, G, LENGTH

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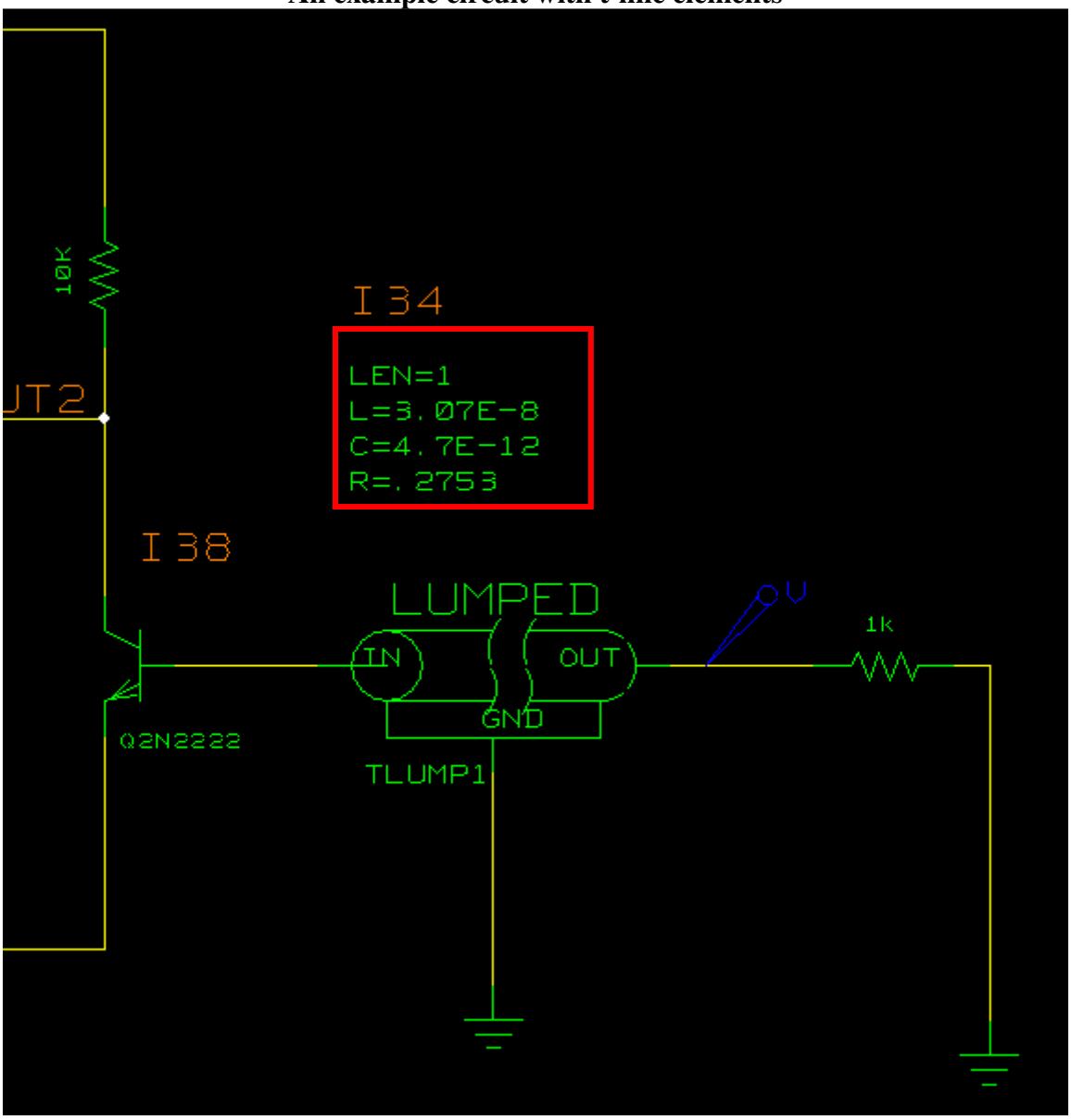
An example circuit with t-line elements



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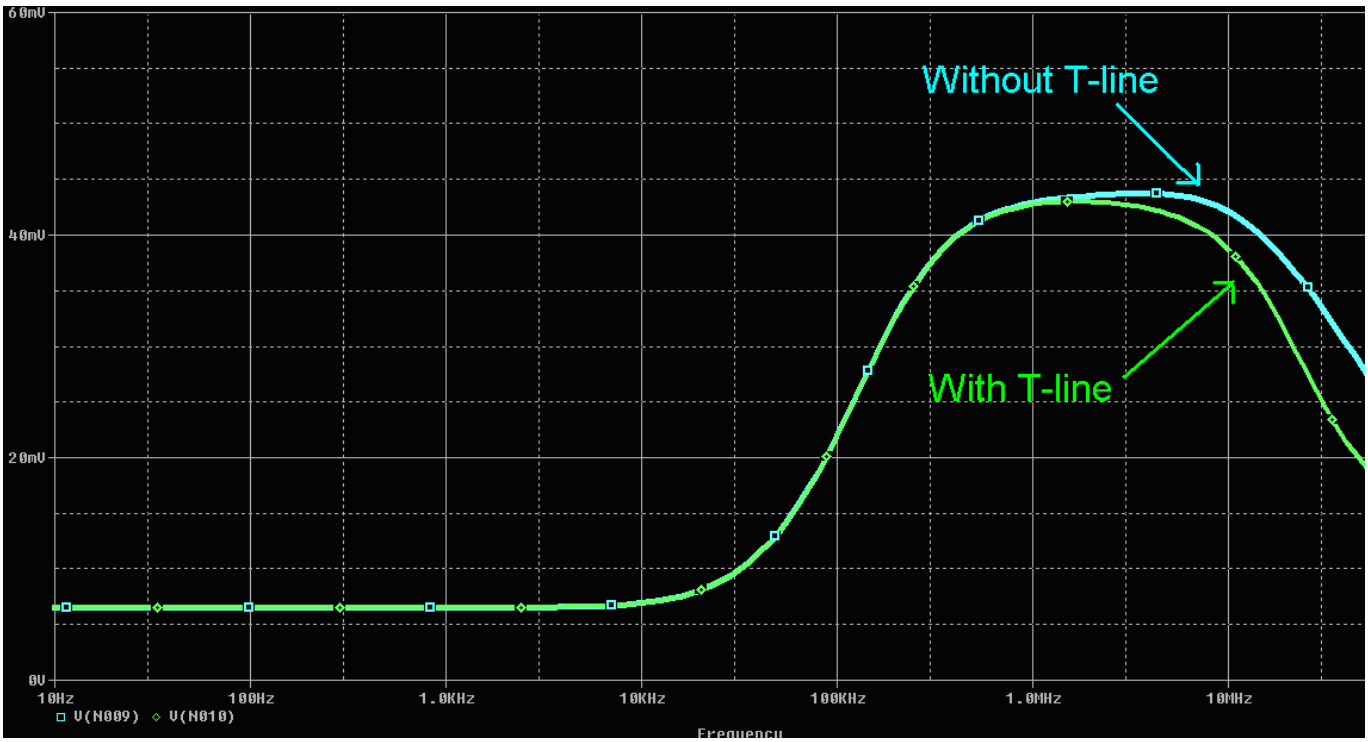
Simulation results with and without t-line values

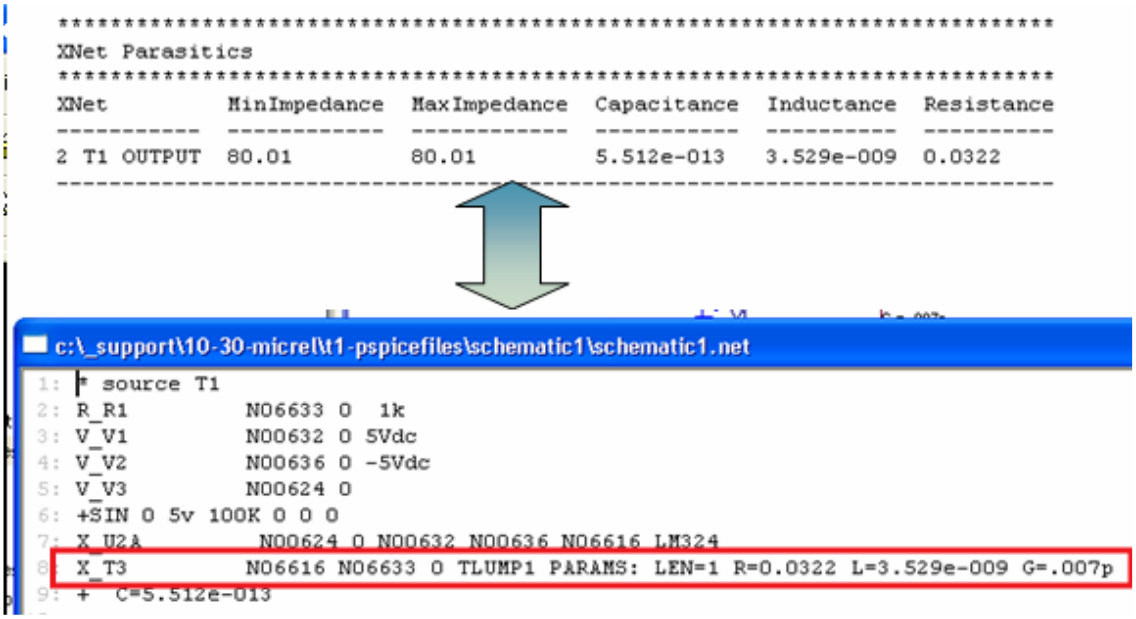


Editing the Spice Netlist

This process could be automated this by inserting the t-line values into the existing spice netlist for the circuit rather then adding the t-line parts to the schematic circuit. For example use the Parasitics report to get the transmission line values for all nets of interest. Then write a script to reformat the report and weave the values into the spice netlist. The details of automating this process are outside the scope of this appnote.

Including Routed Interconnect in AMS Simulations

Parasitics report converted to Spice netlist

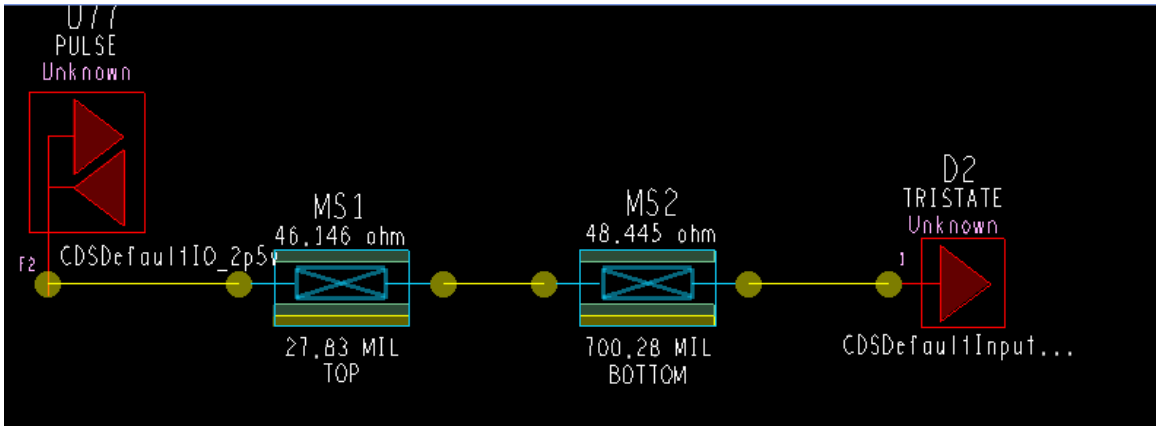


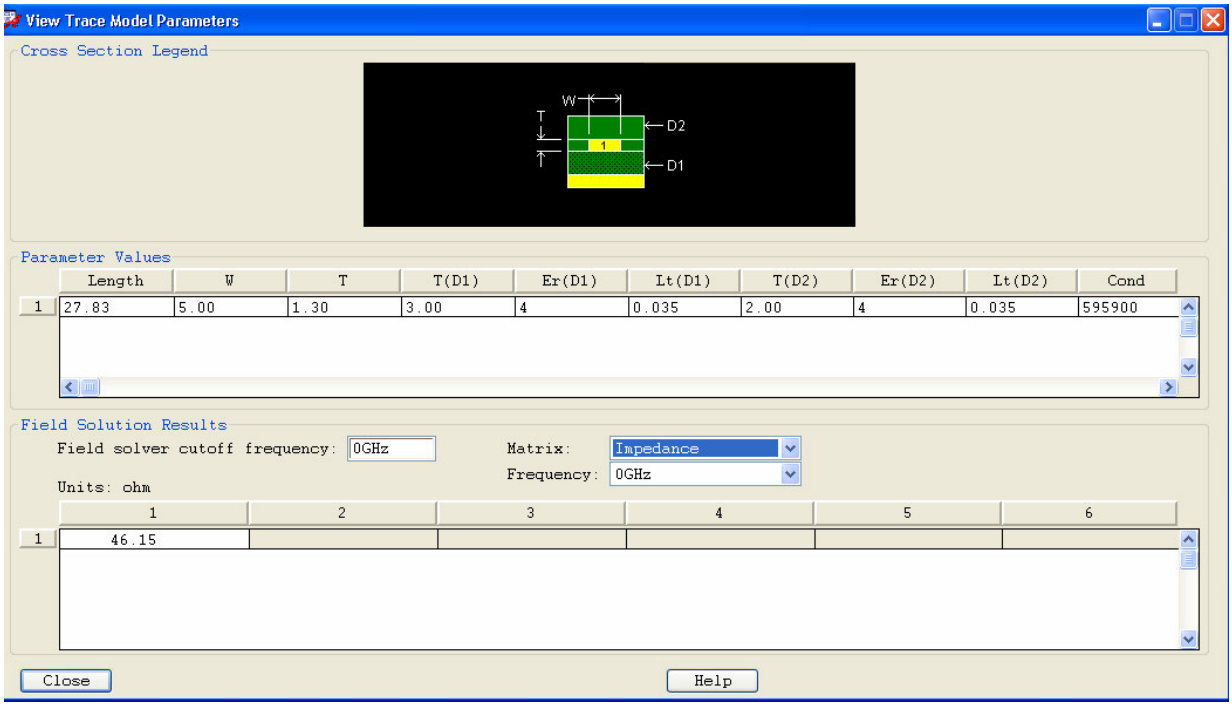
Simulating in SigXP to Obtain Spice Models for T-lines

Allegro SI offers the ability to extract a net into Signal Explorer to view its routed topology. Running a simulation from Signal Explorer creates Espice based models files representing the parameters of each microstrip, stripline, and via. Model Integrity can then be used to convert the Espice models into a spice model representing the T-line. Finally a schematic symbol can be created from the model and placed in the schematic used for AMS simulation. A benefit of this approach is it's not limited to 2 node nets. If a topology representing multiple drivers and receivers is used the resulting spice model will have multiple ports and subcircuits for each internal element. Like the data in the standard parasitic report, this data has been extracted from the field solver with rigorous solution is highly accurate.

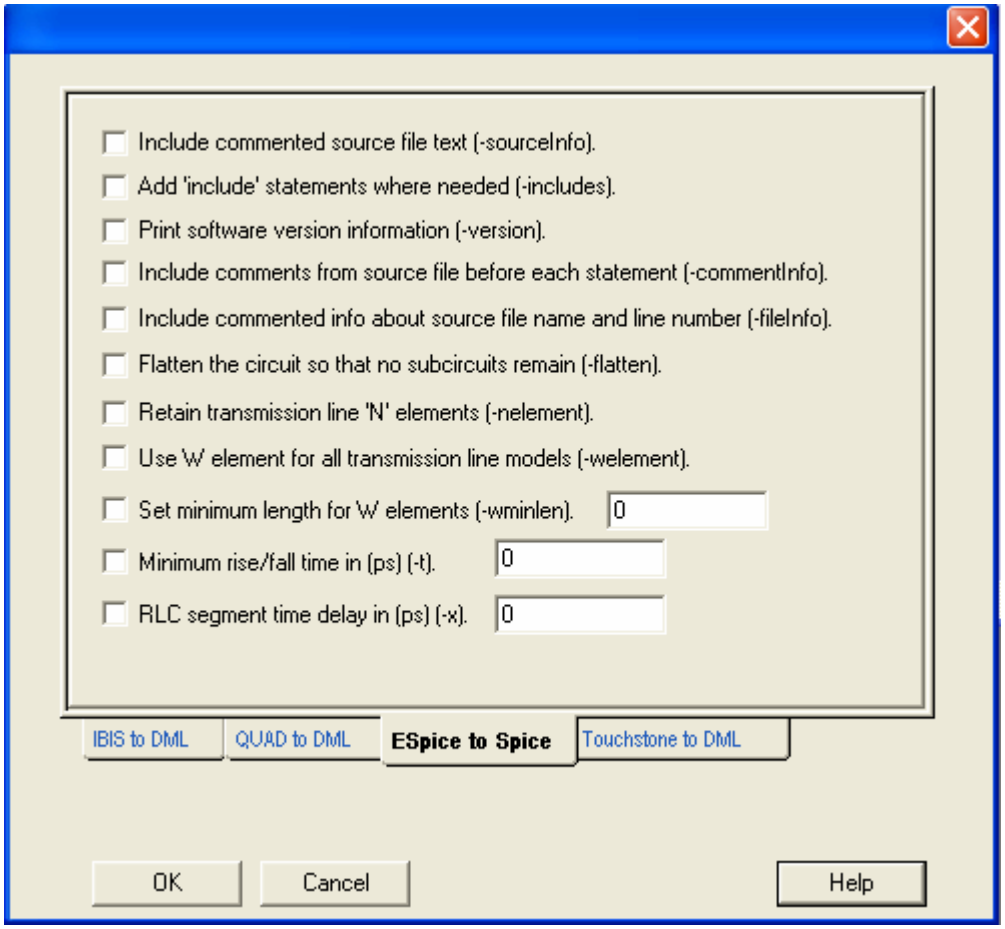
Procedure

1. In Allegro SI invoke the probe function.
2. Either select the routed net(s) of interest or use the browser button to choose from a list of nets
3. Select the view topology button
4. Signal Explorer opens displaying the topology. The numbers you get in the trace model parameters are per unit length values. The length that is used is 1 meter.





5. Run a simulation. This creates Cadence Espice files for the T-line elements in working_dir\sigxp.run\case0\sim1
6. Use model integrity to convert the cadence Espice files to a standard spice model file
    a. In Model Integrity open the interconn.spc file in the working_dir\sigxp.run\case0\sim1 directory
    b. Set the desired options for Espice to spice conversion



c. Select the interconn.spc file and from RMB choose Translate Selected→Generic Spice. This runs the command spc2spc. This creates a spice model file "interconnspc_gen.spc" which can be used in AMS simulation.

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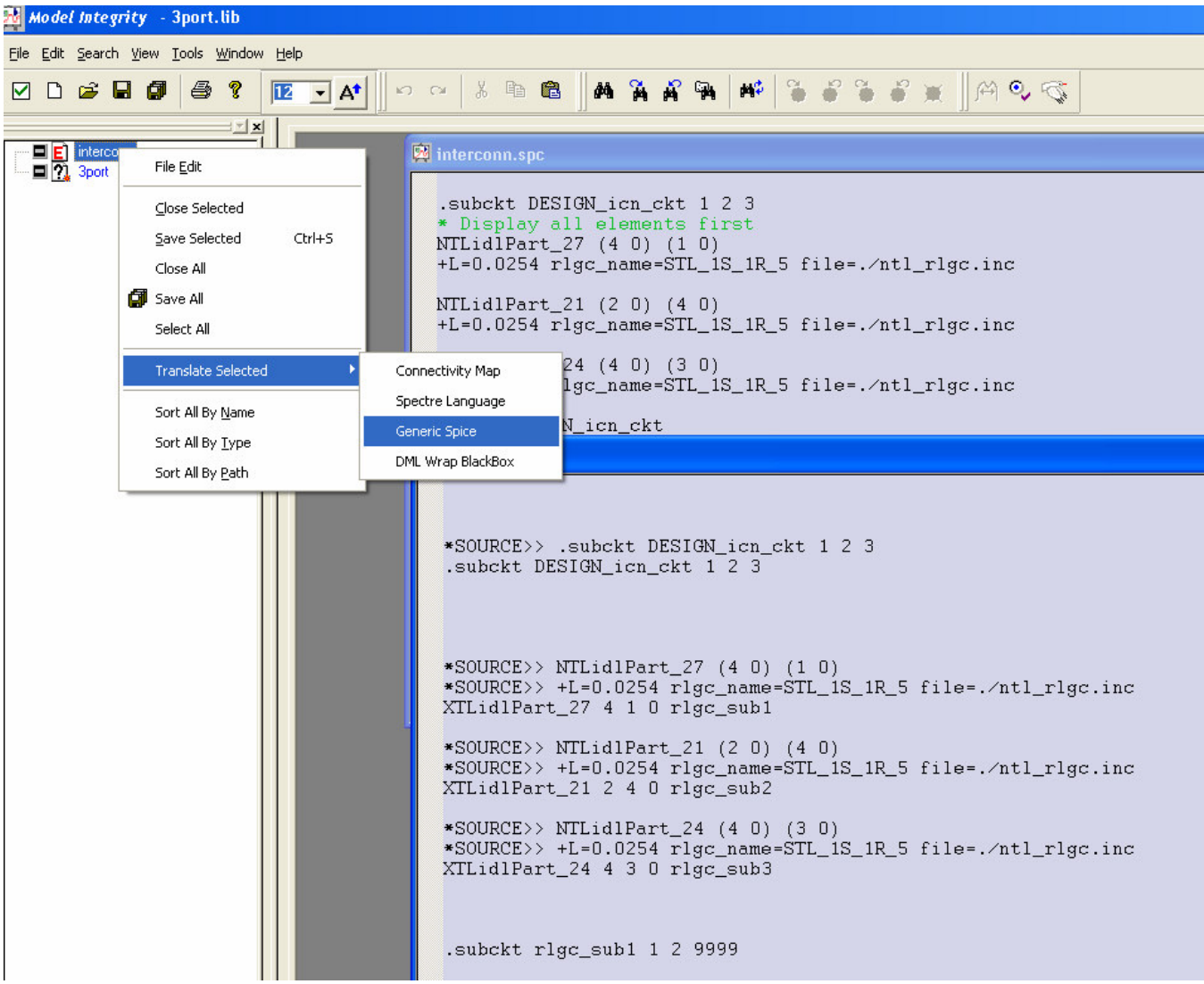


spc2spc models transmission lines as distributed lumped element models with the `-s` option, or in the case of single-line transmission lines, as T-models. By default, all transmission lines are modeled as distributed RLC element lines. Coupled transmission lines are modeled with mutual capacitances and inductor coupling coefficients (k-factors).

spc2spc determines the granularity of the distributed, lumped sections based on the modal propagation velocities in the transmission lines and the minimum transmission tile from the stimulus file. The propagation delay for a section is constrained to be 1/20th of the minimum transmission time in the system. This limits the lumped element approximation error to 4%. You can use a command line option (`-x=tau`) to override the default per-section delay to any non-zero value. You can use another command line option (`-t=tr`) to override the minimum rise and fall time used in the lumped section delay calculations.

spc2spc breaks inductive resistors (resistive inductors) into two series elements. It keeps skin-effect resistors as parallel elements to the series R-L elements when they are present.

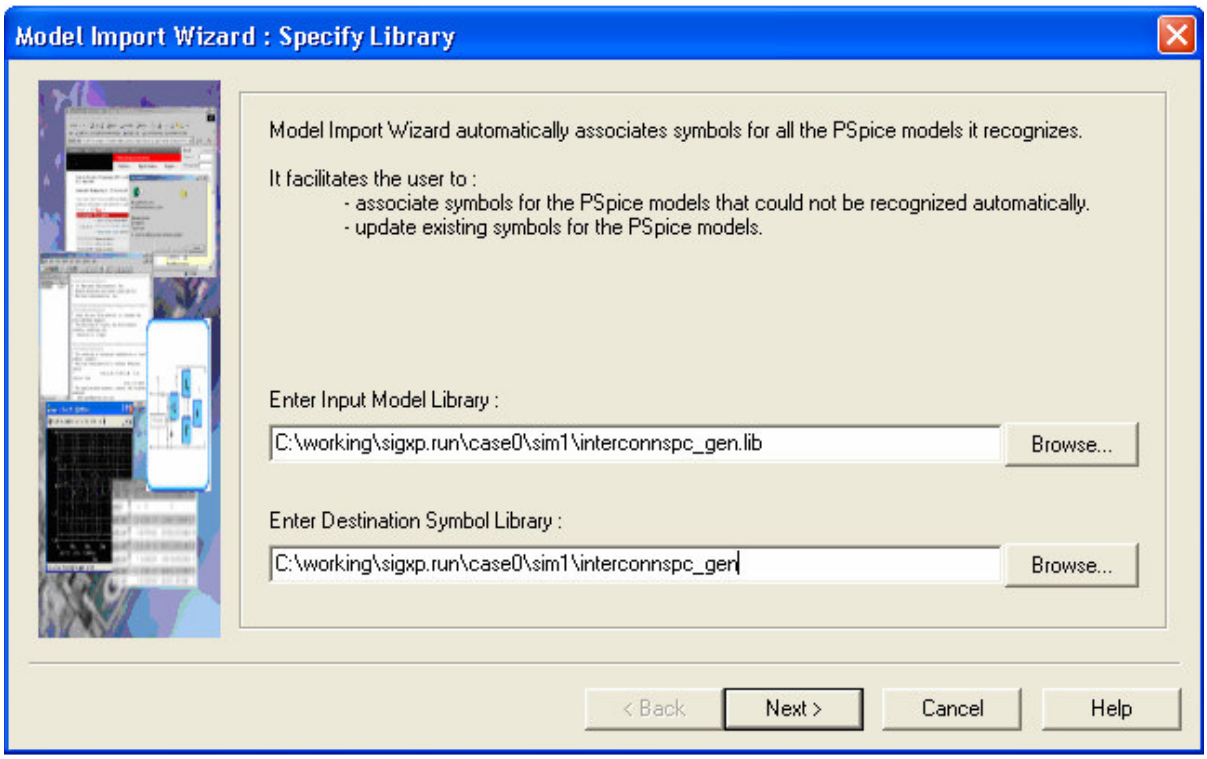
spc2spc can also be run from a command line. For full documentation on spc2spc see Model Integrity user's guide.

Creating Schematic Symbols for Spice models created from Model Integrity

With the spice model for the T-lines a symbol can be created to be placed into the circuit.

Procedure

1. Use the AMS model editor to create a schematic symbol for the spice model just created from model integrity. Note that the model file interconnspc_gen.spc needs to be renamed to .lib for model editor to recognize it. A suggestion is to also name the .lib according to the name of the Net/ T-line the model represents.



2 Place the symbol which represents the interconnect in the schematic and connect it to the appropriate nodes in the schematic

Circuit without Tline part

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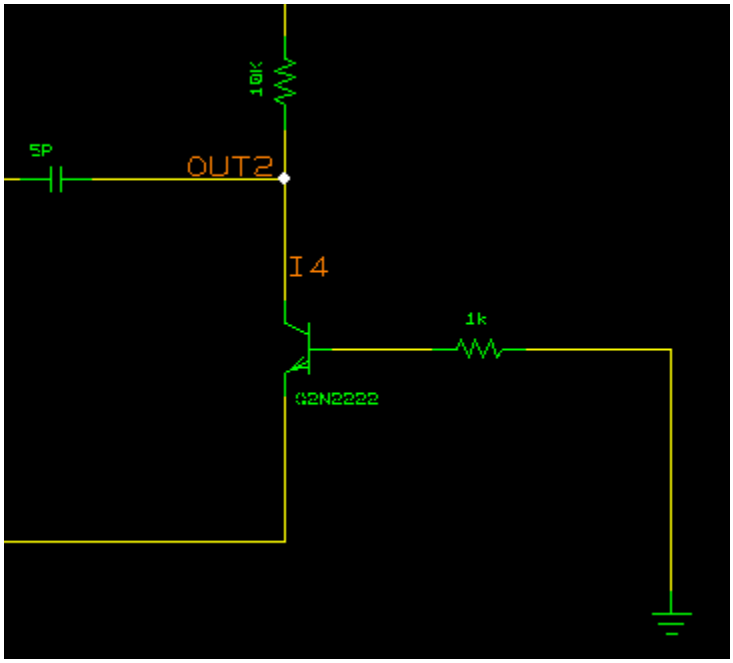
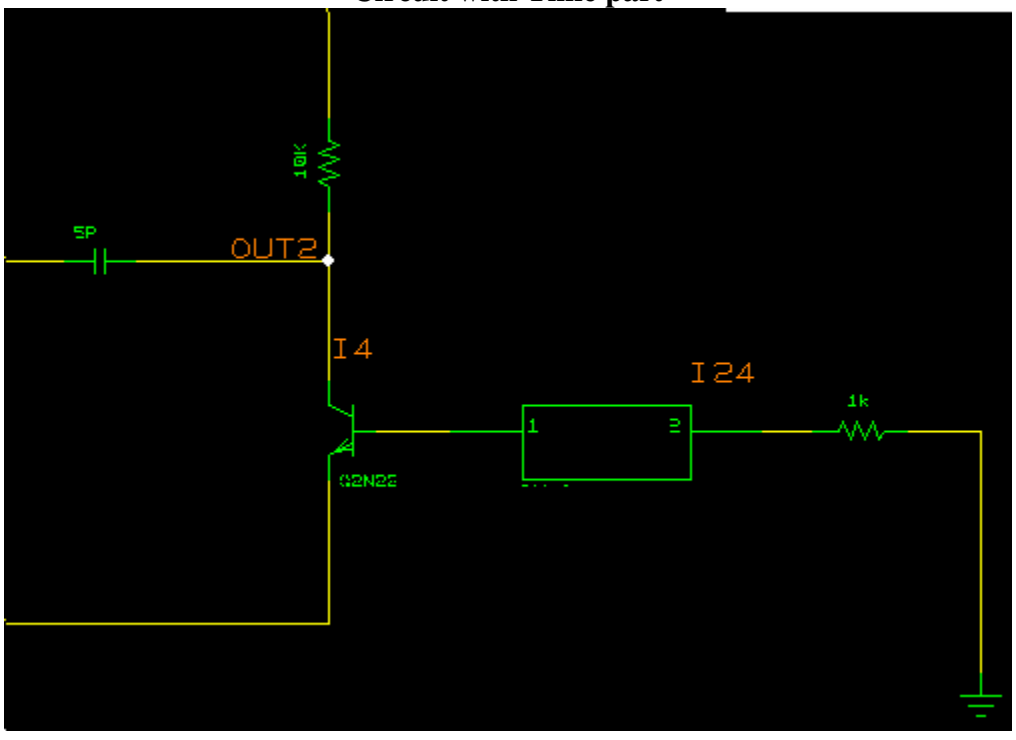


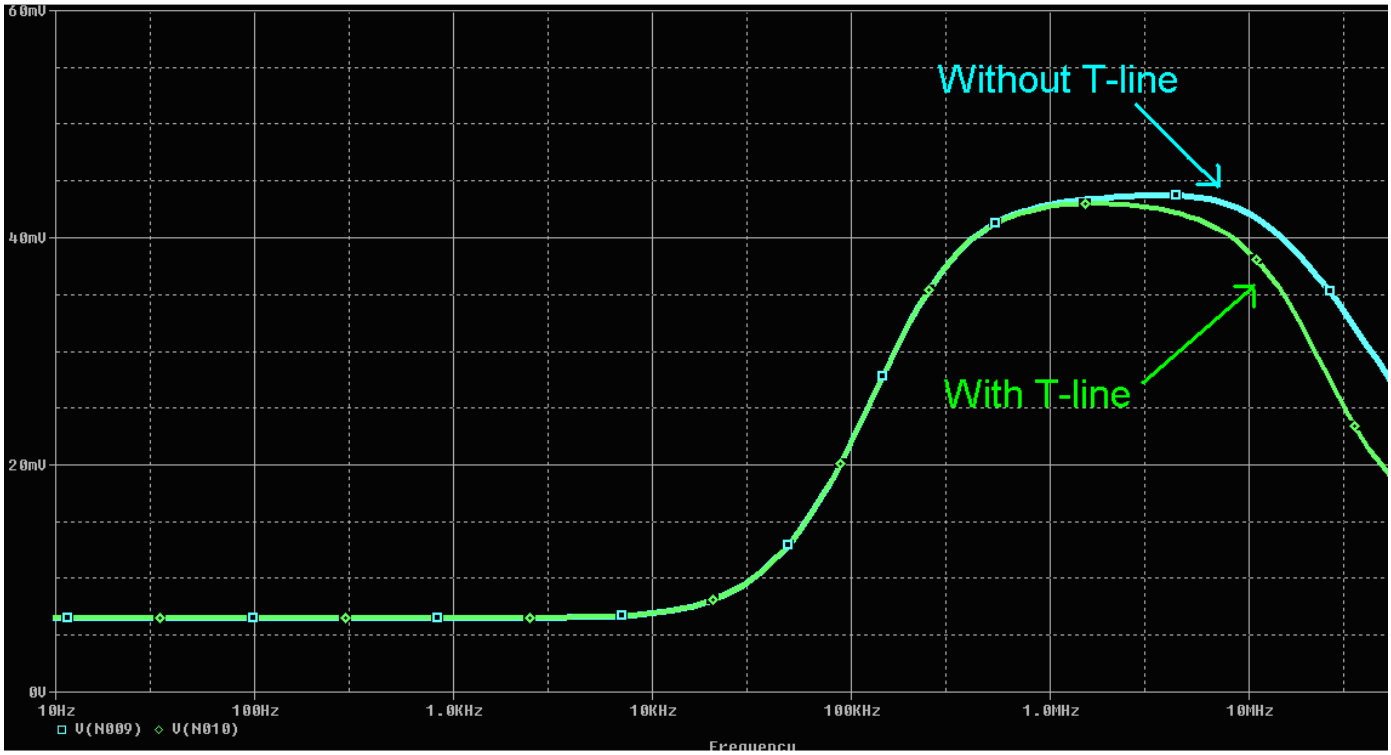
Circuit with Tline part



3. Add the spice models for the t-lines created in step 6 to the simulation settings and re-run the simulation.

Simulation results with and without t-line values

Including Routed Interconnect in AMS Simulations



Summary

It is possible to include routed T-line parasitics in an AMS simulation. Allegro SI offers different methods to obtain t-line parasitics. These t-line values can then be included in the AMS simulation. This process can be automated depending on how frequently this needs to be done.

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