



DDR2 and DDR3 Challenges

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Session # 8.4

9/17/2007

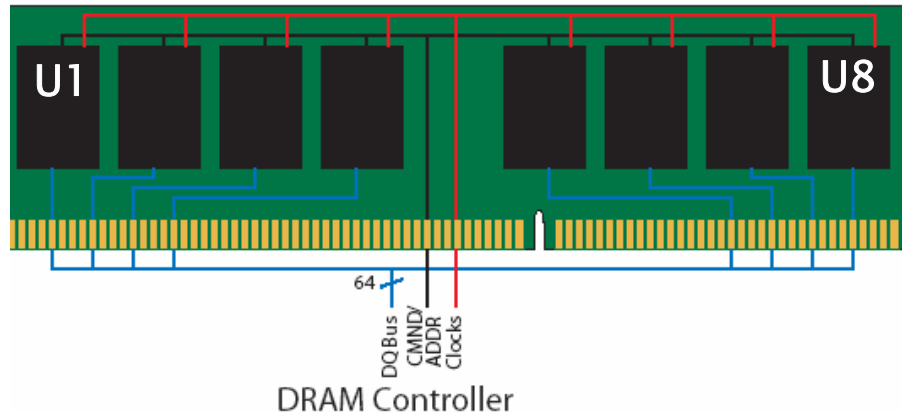
Outline

1. Comparing DDR2 and DDR3
 1. Tree Topology
 2. Fly-By Topology
 3. Data Channel
2. Using Allegro PCB SI
 1. Post-layout analysis using Bus Analysis in Allegro PCB SI
 2. Timing Budget for DDR2 and DDR3
 3. Comprehensive simulation in Allegro PCB SI
 4. S-Parameter Package Model in Allegro PCB SI
3. Correlation – Lab versus Simulation
4. Summary

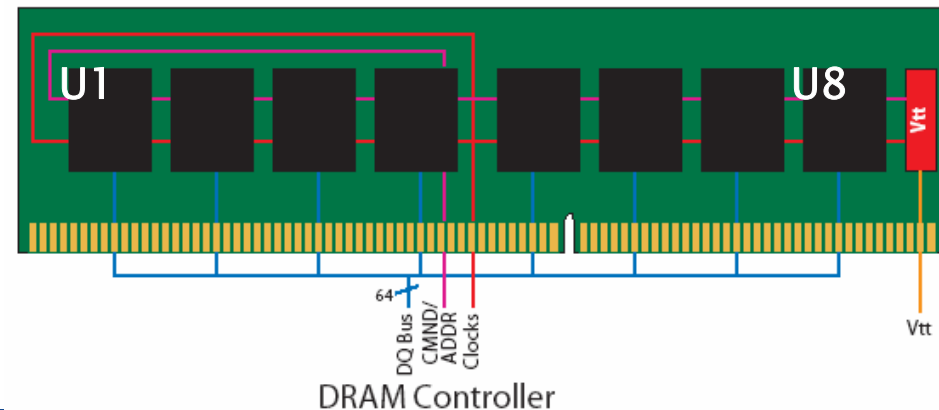
Topology

- **DDR2 memory modules uses tree topology which**
 - Increases number of stubs and stub length
 - Signal arrival time is same on each DRAM
 - Address/Command/Control has a VTT termination on the system board
 - Less data-eye margin
- **DDR3 memory modules uses fly-by topology which**
 - Reduces number of stubs and stub length
 - Causes interconnect delay skew between clock and strobe at every DRAM on DIMM
 - Address/Command/Control has a VTT termination at the far end of the bus on the module
 - More bandwidth

DDR2 'Tree' Structure

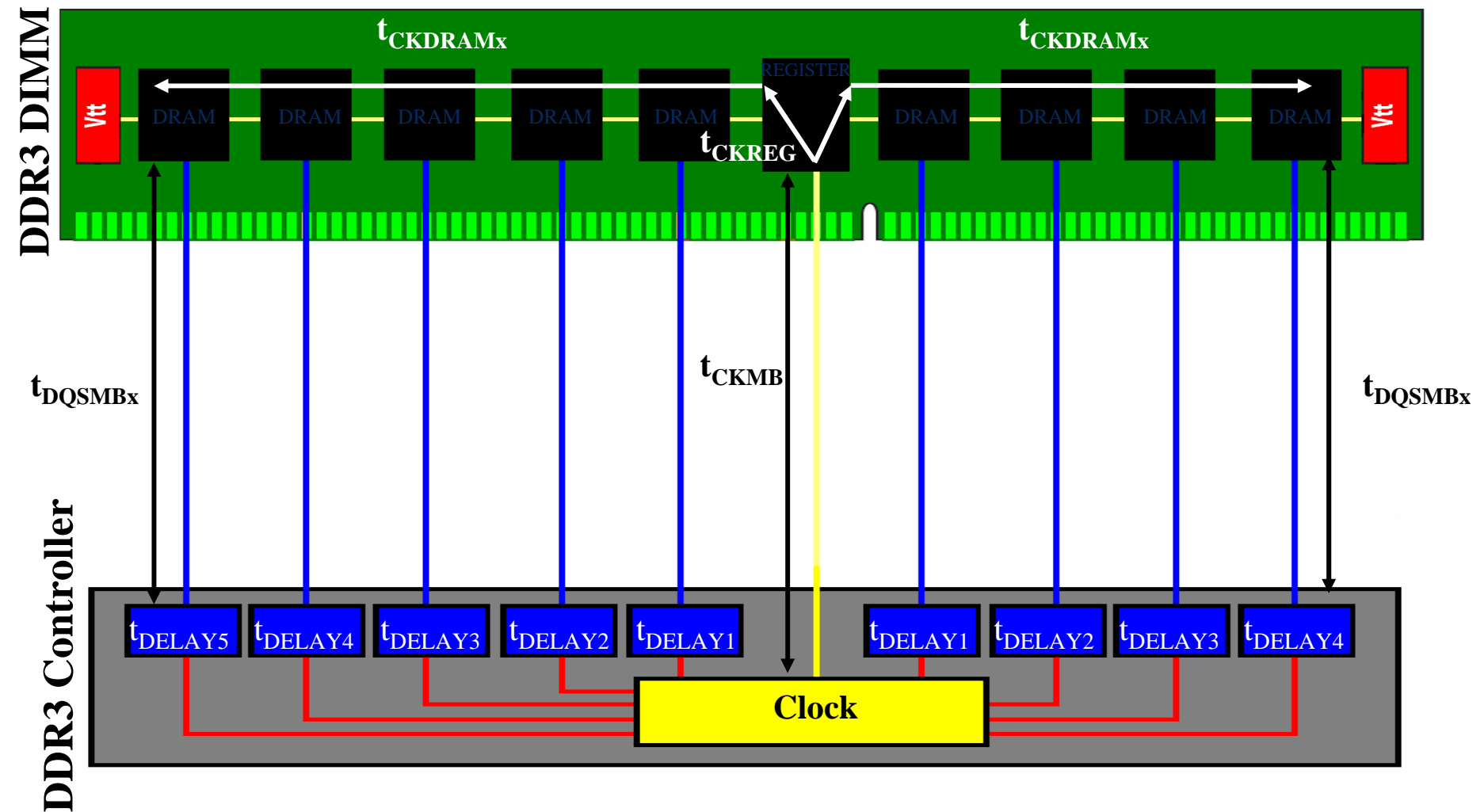


DDR3 'Fly-By' Structure

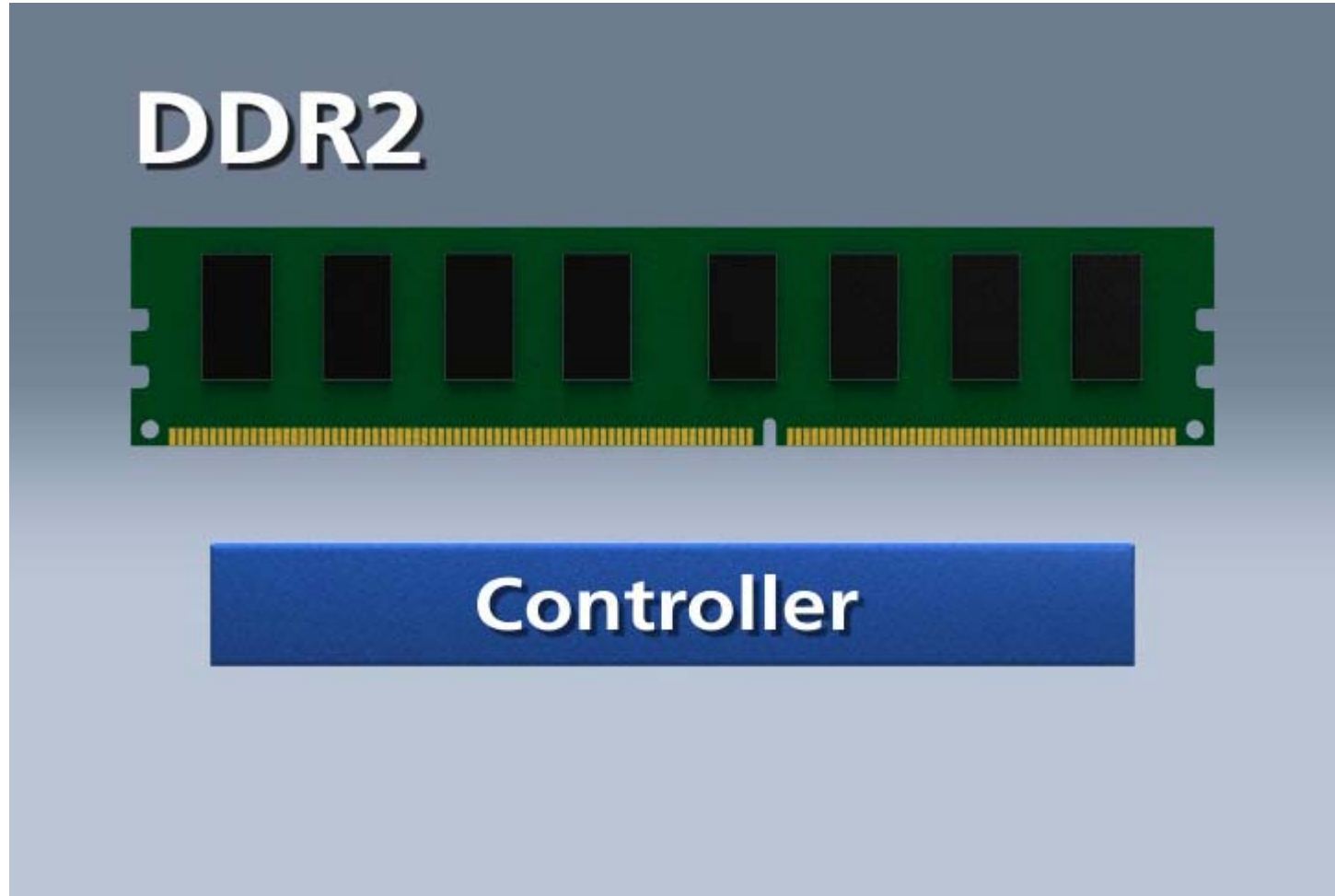


Write Levelization

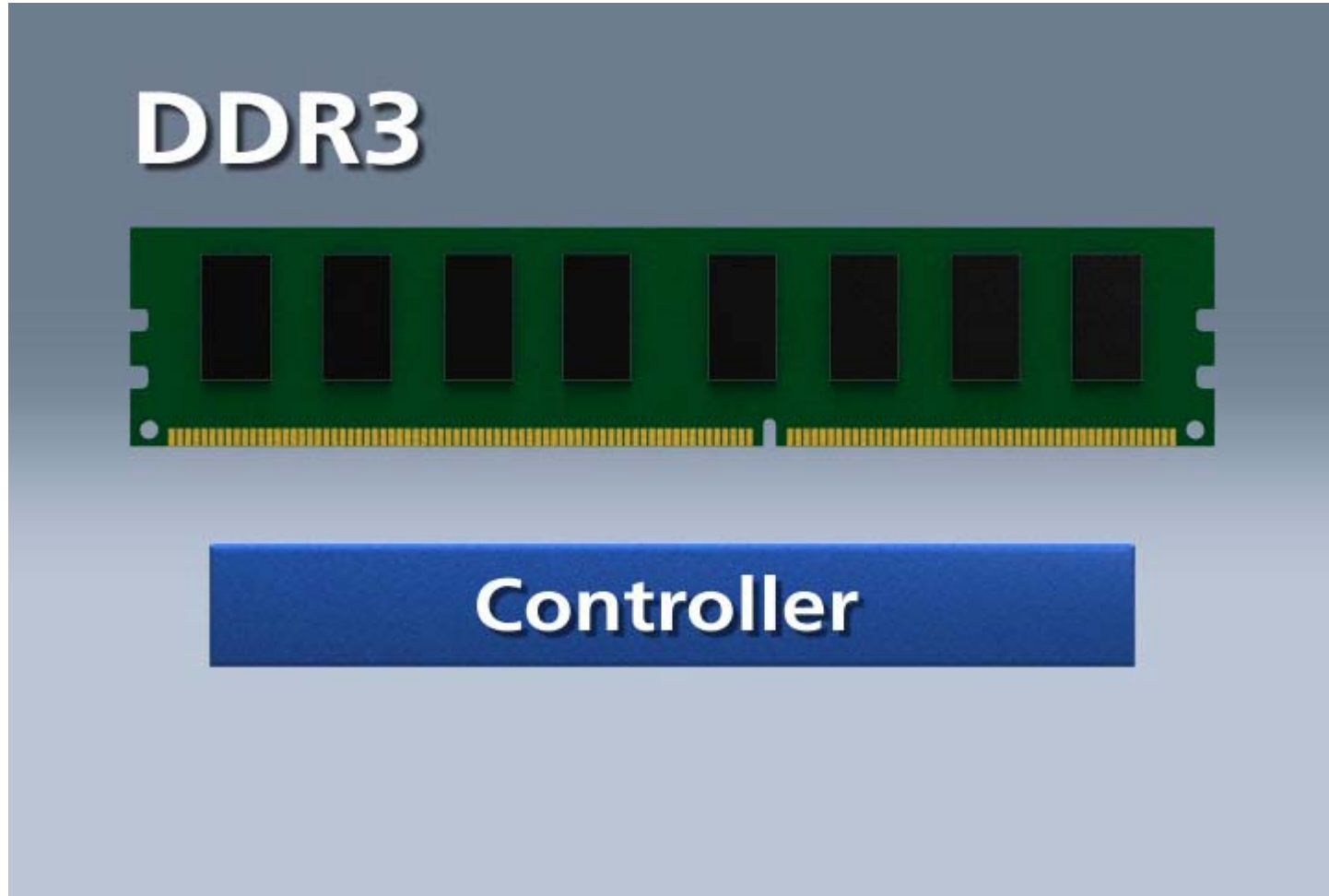
$$t_{\text{Delay}_x} + t_{\text{DQSMB}_x} = t_{\text{CKMB}} + t_{\text{CKREG}} + t_{\text{CKDRAM}_x}$$



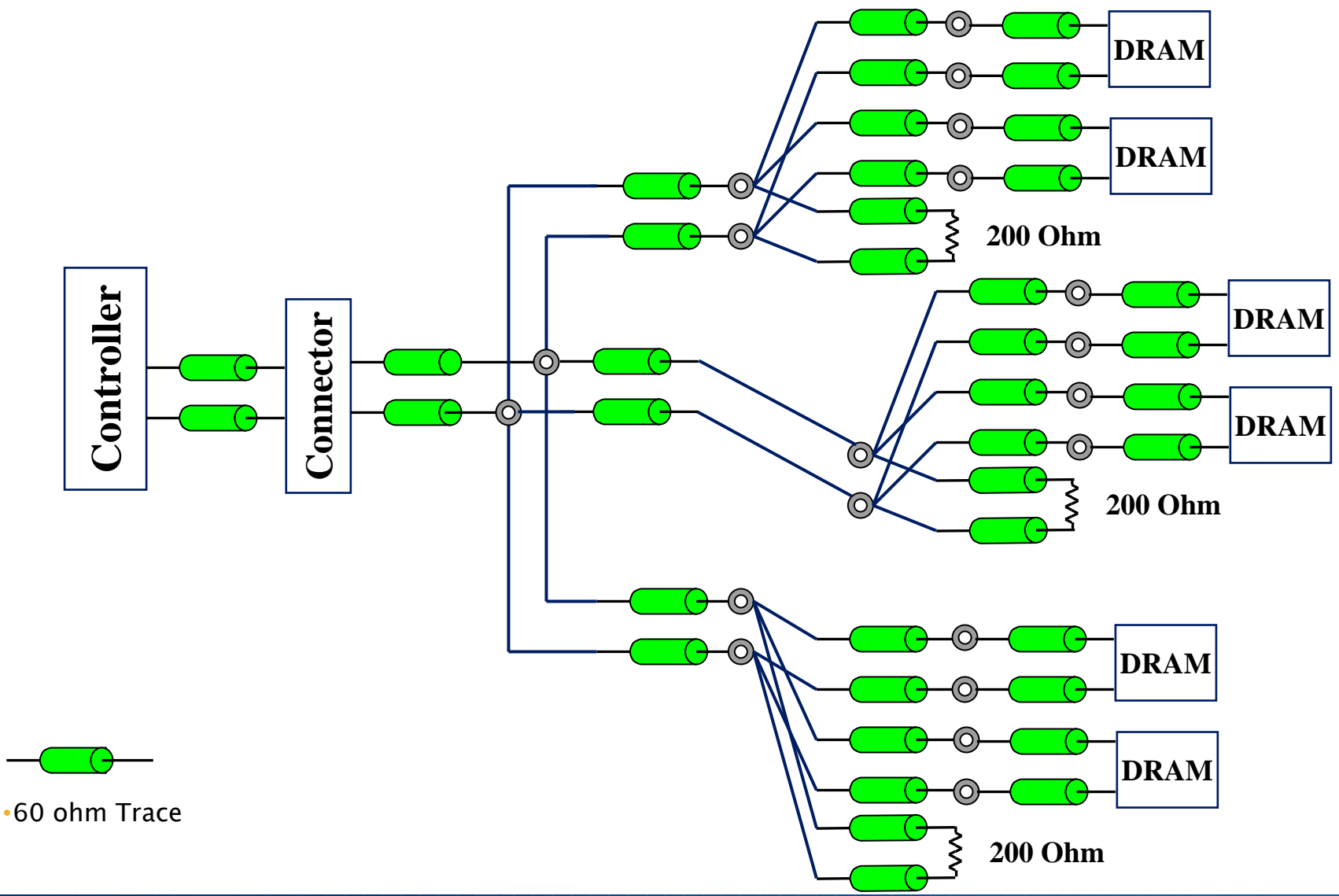
Tree Topology



Fly-by Topology

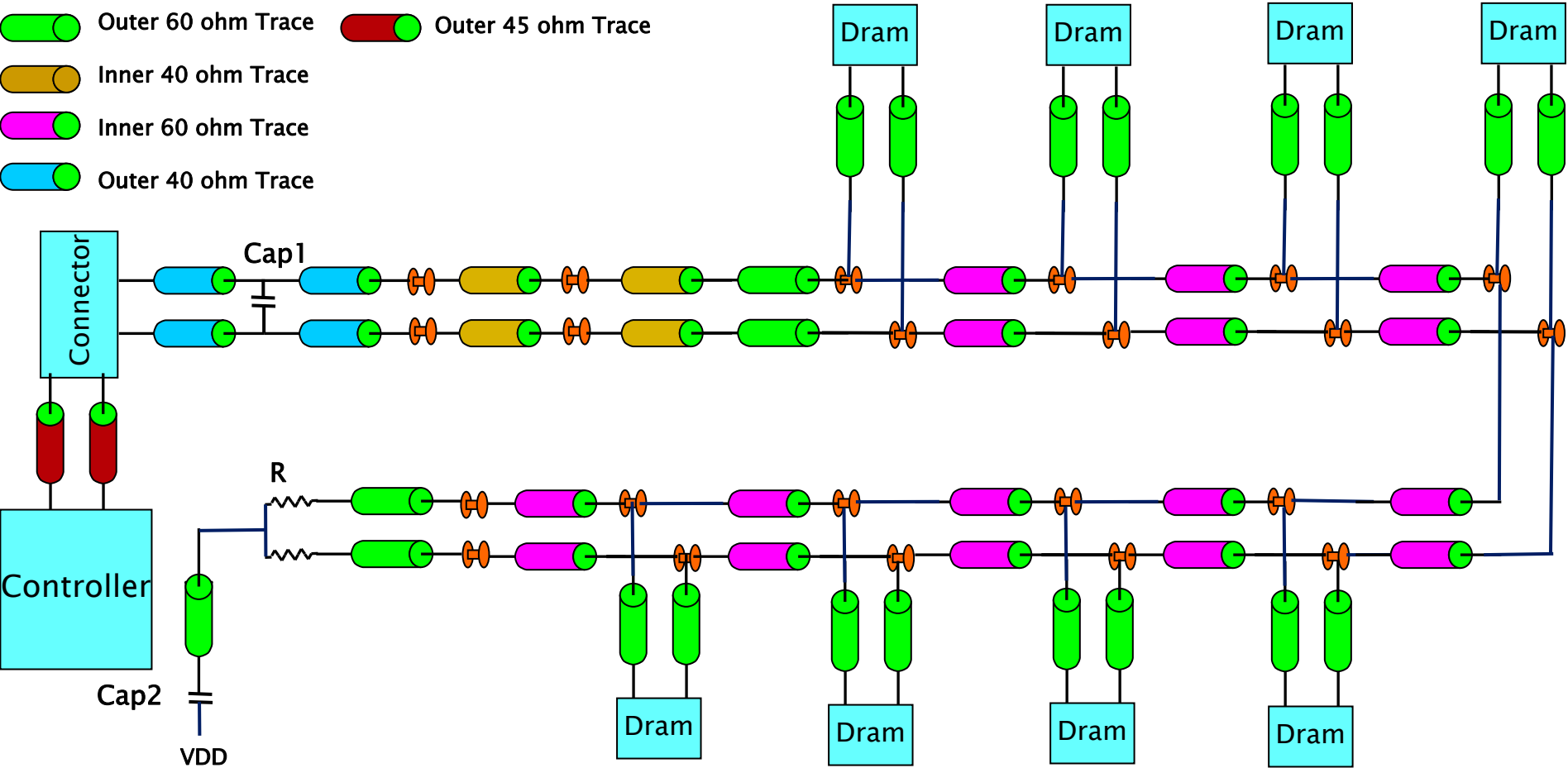


DDR2 UDIMM Clock Topology

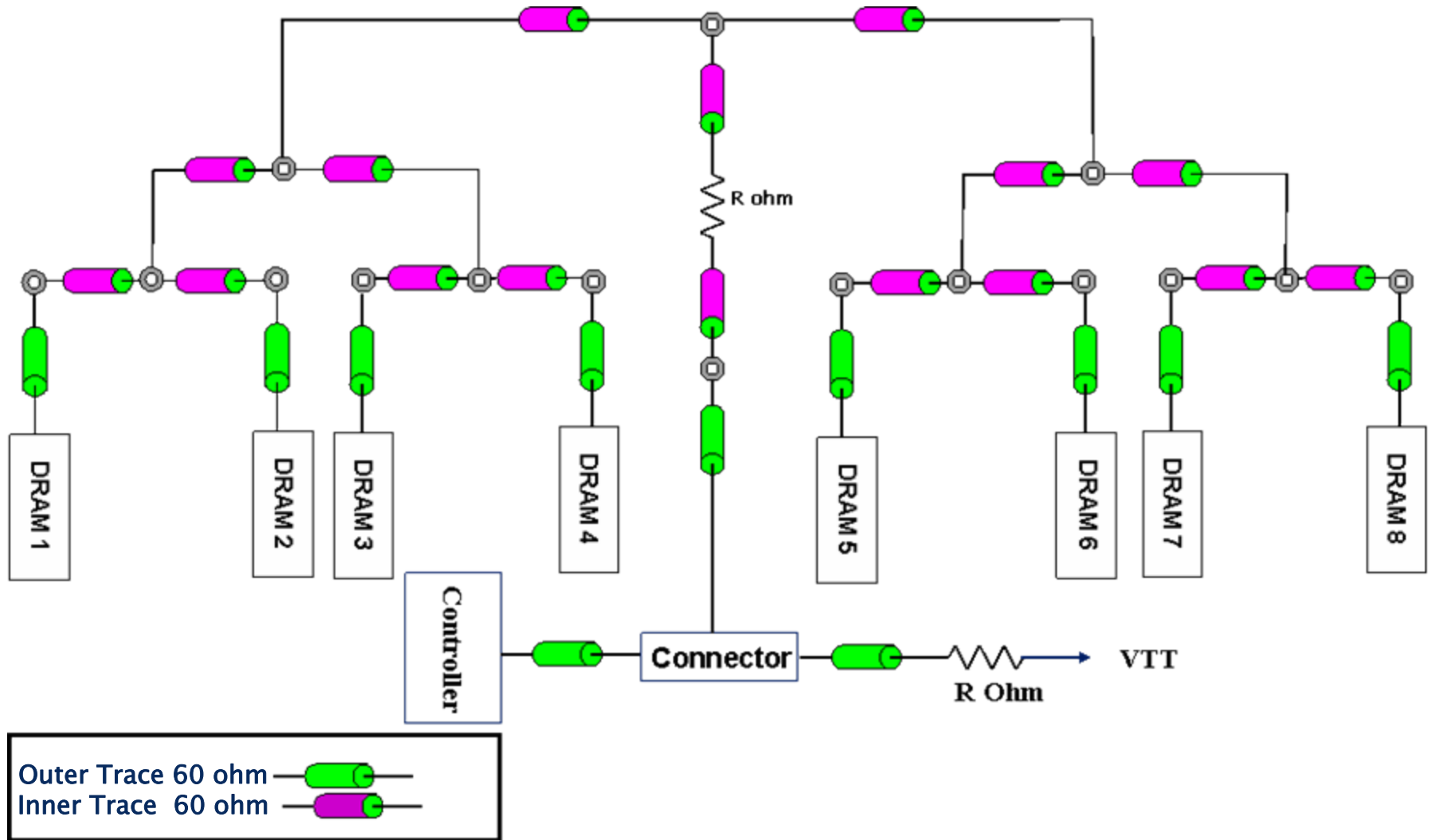


• 60 ohm Trace

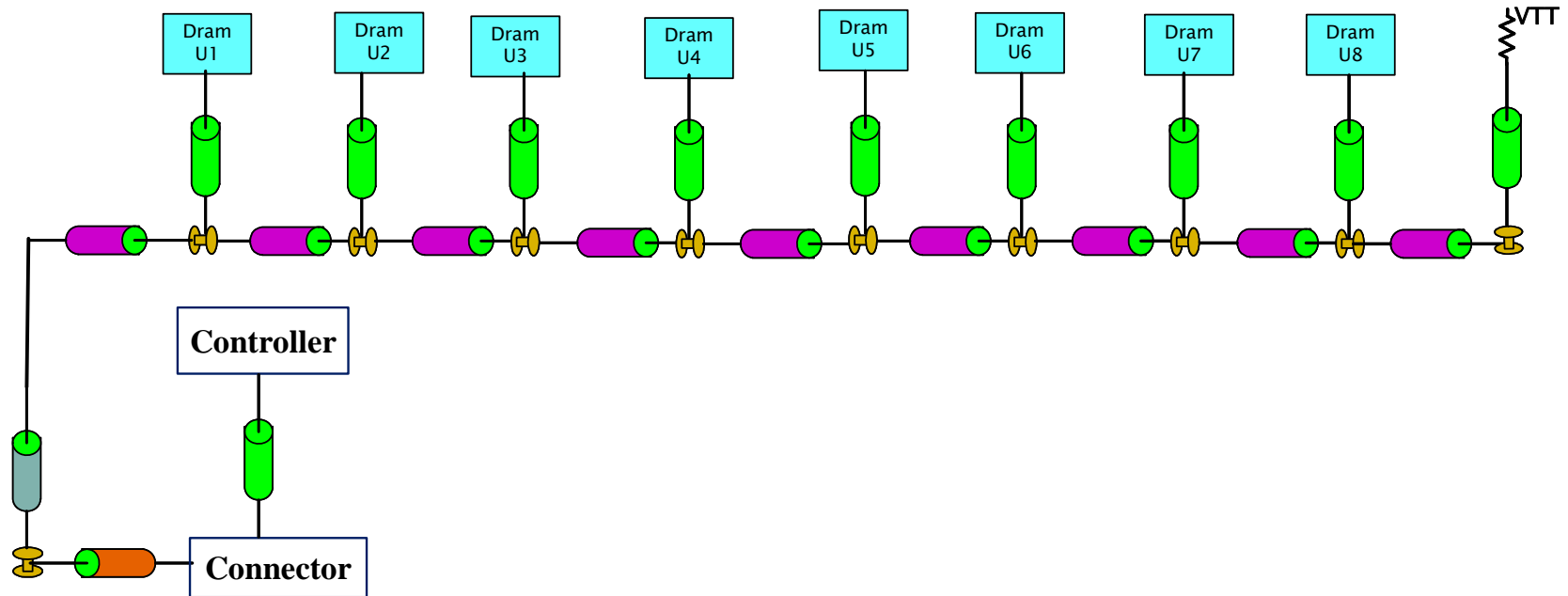
DDR3 UDIMM Fly-by Clock Topology



DDR2 UDIMM Address Topology



DDR3 UDIMM Fly-by Address Topology

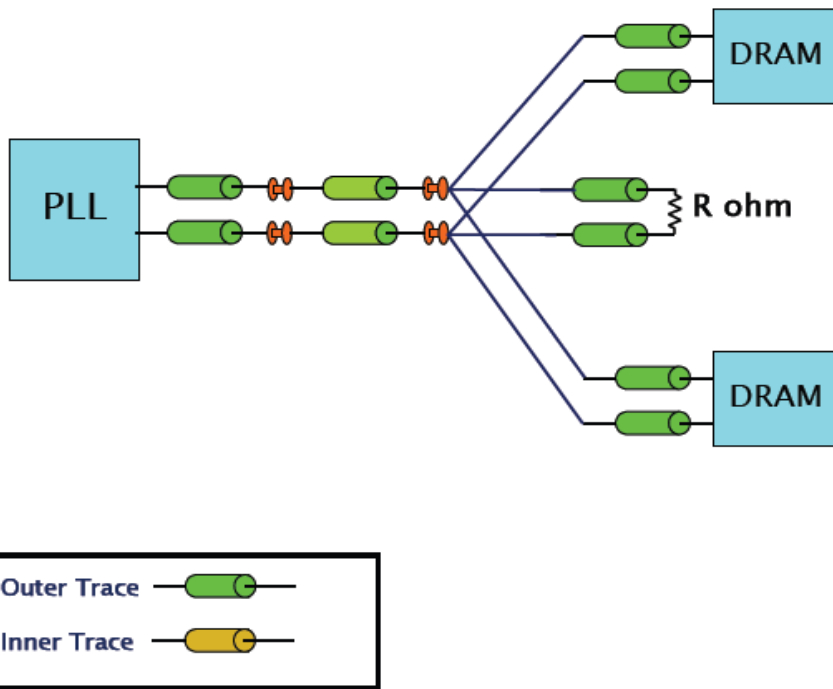


- DDR3 UDIMM nets have unloaded and loaded sections on Address/Command/Control topology
- This was required to obtain better impedance match in a system

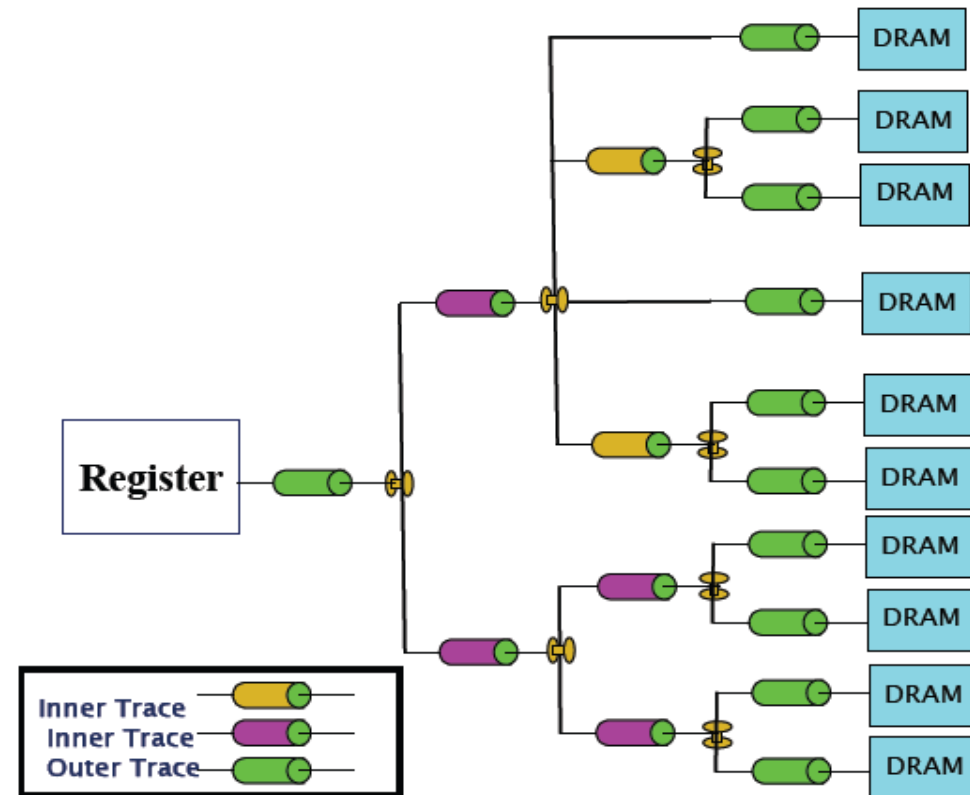


DDR2 RDIMM Post Register Nets

Clock Topology

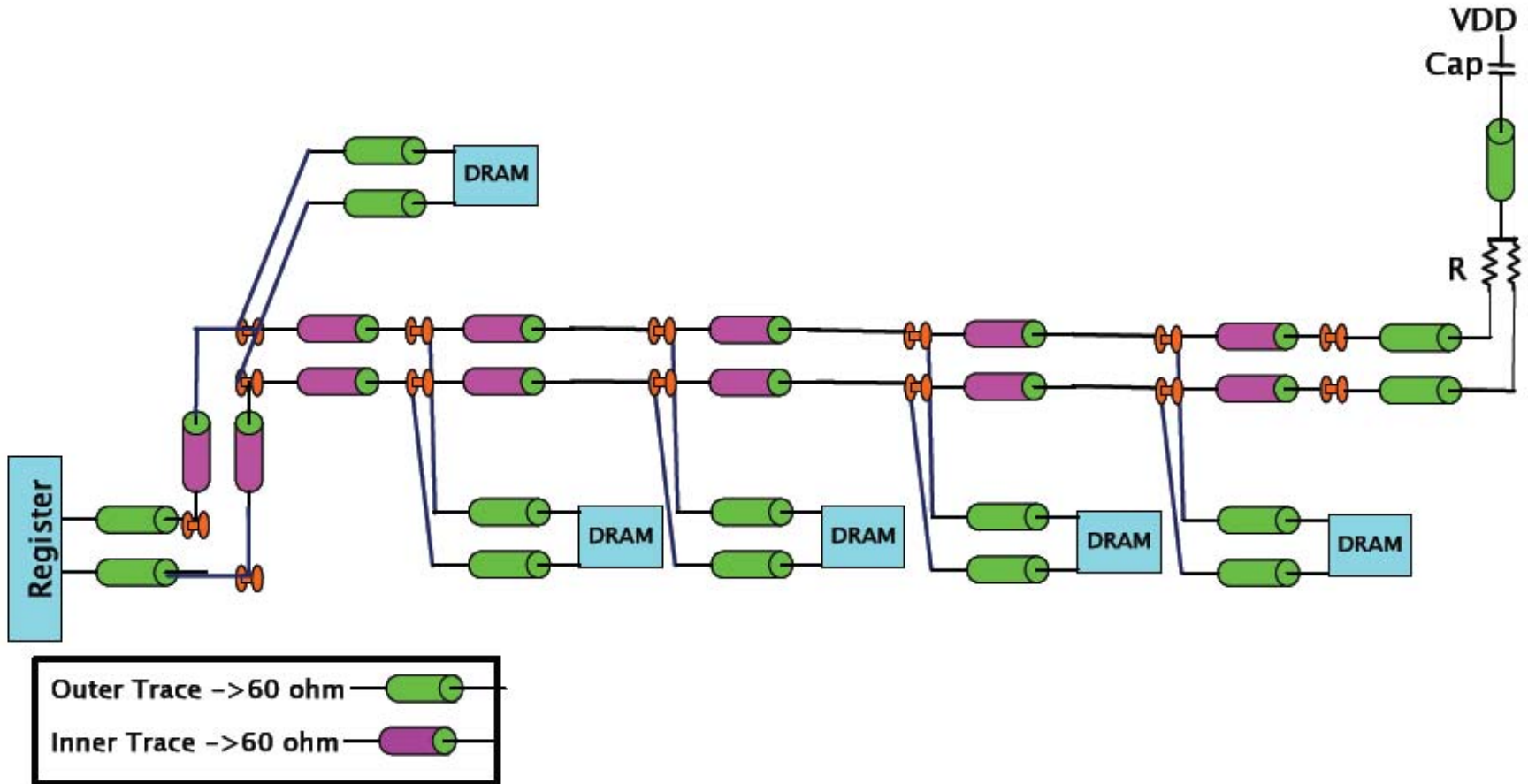


Address Topology

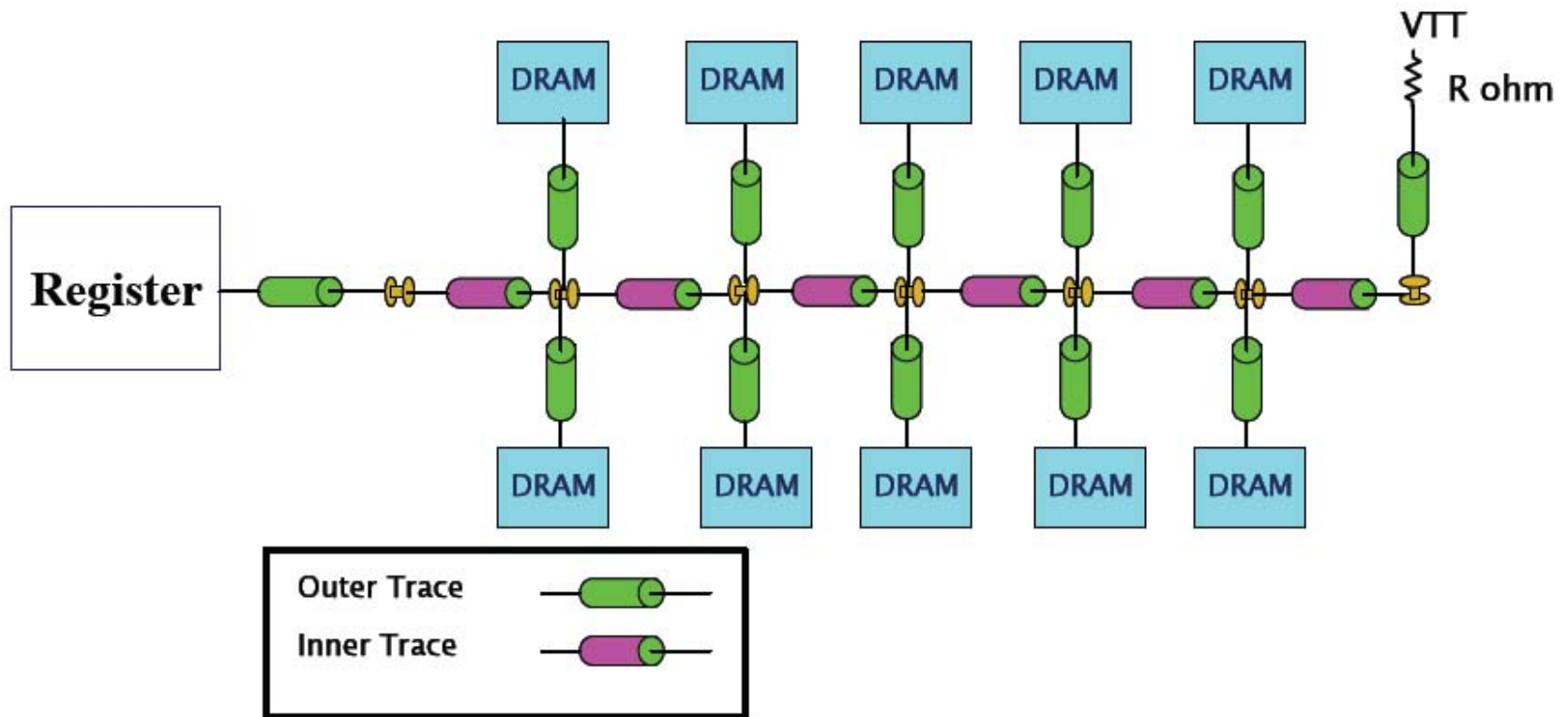


Note : All 60 ohm Trace

DDR3 RDIMM Fly-by Clock Topology



DDR3 RDIMM Fly-by Address Topology



Note : All 60 ohm Trace

Improvements to the Data Channel

- The DDR3 data channel can run faster due to enhancements in the DDR3 component
 - ▶ DDR2 ODT values reflect only: 50Ω, 75Ω, 150Ω
 - ▶ DDR3 ODT values include: 20Ω, 30Ω, 40Ω, 60Ω, 120Ω
 - ▶ DDR3 supports dynamic ODT

DR	SR	Slot 1	off	120Ω	ODT off	20Ω	na
		Slot 2	off	ODT off	20Ω	120Ω	na
SR	DR	Slot 1	off	120Ω	na	ODT off	20Ω
		Slot 2	off	20Ω	na	120Ω	ODT off
SR	SR	Slot 1	off	120Ω	na	30Ω	na
		Slot 2	off	30Ω	na	120Ω	na



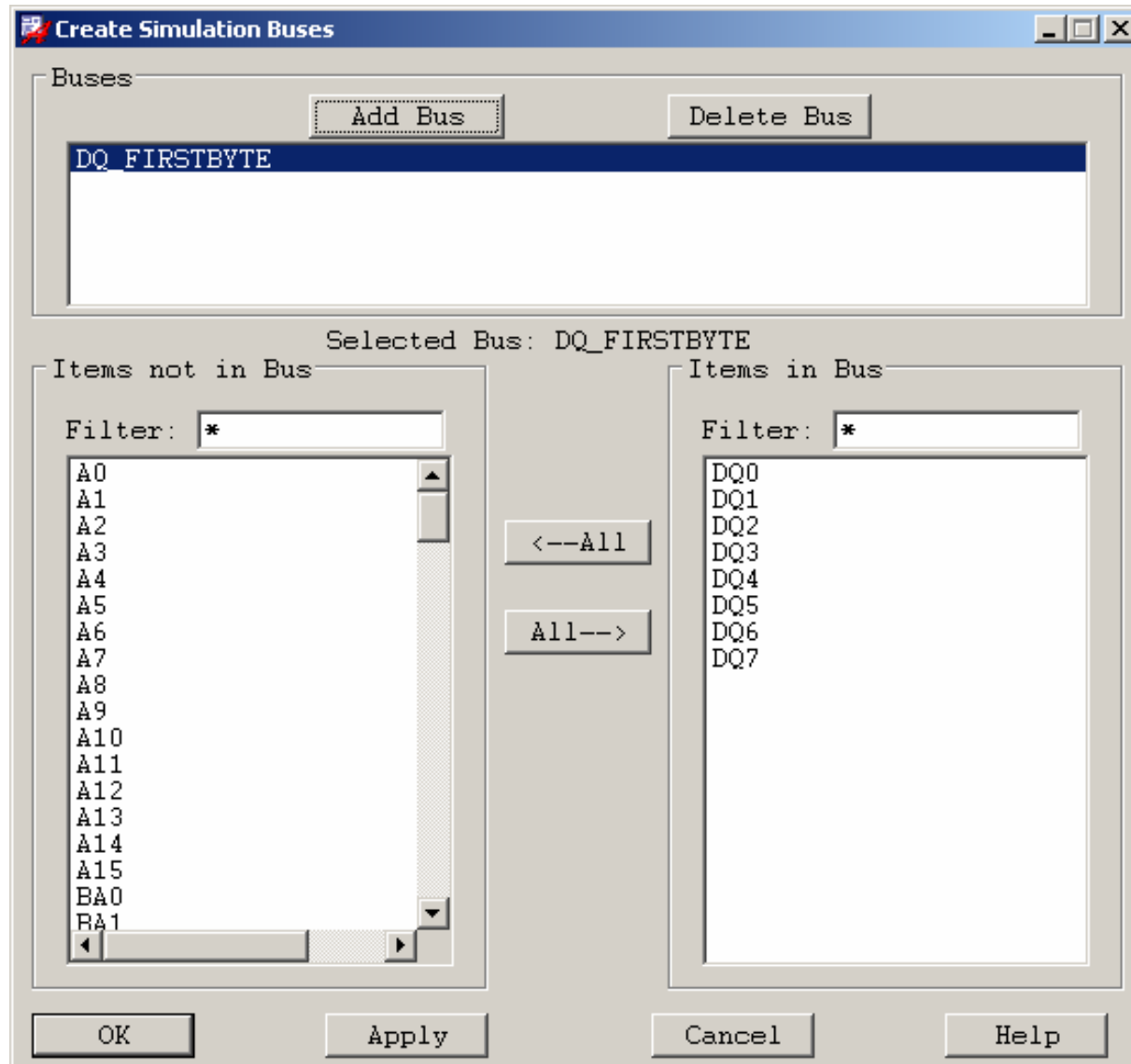
Bus Setup and Simulation

Allegro PCB SI

9/17/2007



Bus Setup and Simulation



Bus Setup and Simulation

- PCB SI V16.0 allows you to assign models in two different ways
 1. Assign by : Model Selector

Signal Bus Setup

Select Bus to Setup

Bus Name: MBRD_DQ_FIRSTBYTE

Bus Direction: UniDirectional BiDirectional

Controller Refdes: MBRD_U1

Switch On: Both Edges

Derating Table File: ddr3_dq_derating.dat

Assign Bus Component Buffer Models | Select Clocks or Strobes | Assign Bus Xnets to Clocks or Strobes

Assign By: Model Selector Component

Component Model	Model Selector	Driver	Active Receiver	Standby Receivers
MT41J128M8HX	V48C_DQ	V48C_DQ_34	V48C_DQ_34_ODT120	V48C_DQ_34
DDR3_Driver	DDR3_DRIVER_DDR3_DATA	_DRIVER_Data_IO_1p5X_OD	DDR3_DRIVER_Data_IO_1X	DDR3_DRIVER_Data_1p5X

Buffer Model To Be Assigned: DDR3_DRIVER_Data_1X DDR3_DRIVER_Data_IO_1X DDR3_DRIVER_Data_1X

Export... Import... Assign Assign Assign

OK Apply Cancel Help

Bus Setup and Simulation

2. Assign by: Component

Signal Bus Setup

Select Bus to Setup

Bus Name: MBRD_DQ_FIRSTBYTE Create Simulation Bus...

Bus Direction: UniDirectional BiDirectional

Controller Refdes: MBRD_U1 Assign Bus Stimulus...

Switch On: Both Edges

Derating Table File: ddr3_dq_derating.dat

Assign Bus Component Buffer Models | Select Clocks or Strobes | Assign Bus Xnets to Clocks or Strobes

Assign By: Model Selector Component

* Component *	* Model Selector *	* Driver *	* Active Receiver *	* Standby Receivers *
MODULE2 U1	V48C_DQ	V48C_DQ_34	V48C_DQ_34_ODT120	V48C_DQ_34
MODULE2 U21	V48C_DQ	V48C_DQ_34	V48C_DQ_34	V48C_DQ_34_ODT30
MODULE1 U1	V48C_DQ	V48C_DQ_34	V48C_DQ_34_ODT120	V48C_DQ_34
MODULE1 U21	V48C_DQ	V48C_DQ_34	V48C_DQ_34	V48C_DQ_34_ODT30
MBRD U1	DDR3_DRIVER_DDR3_DATA	3_DRIVER_Data_IO_1p5X_OD	DDR3_DRIVER_Data_IO_1X	DDR3_DRIVER_Data_1p5X

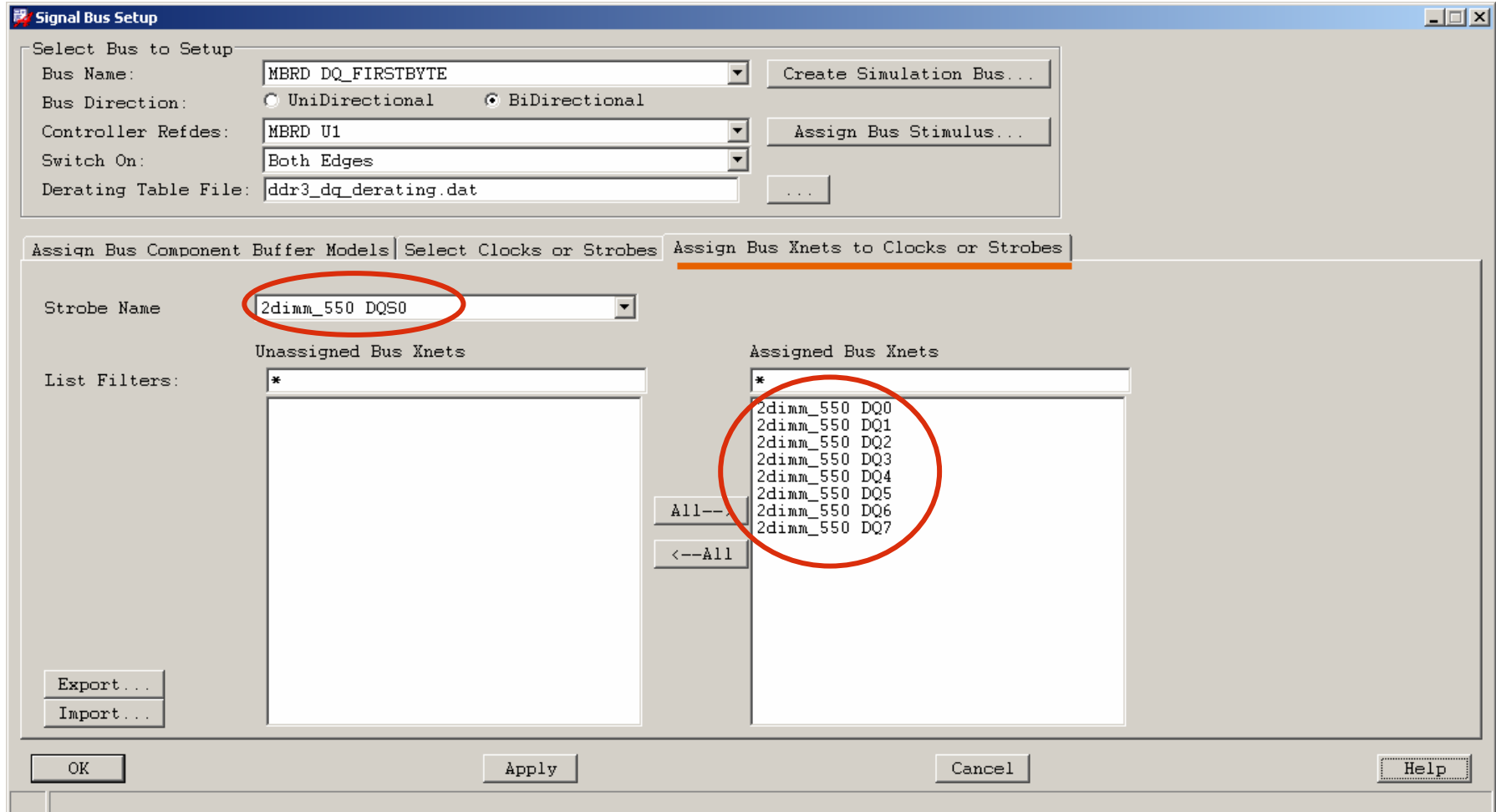
Buffer Model To Be Assigned: DDR3_DRIVER_Data_1X DDR3_DRIVER_Data_IO_1X DDR3_DRIVER_Data_1X

Export... Import... Assign Assign Assign

OK Apply Cancel Help

Bus Setup and Simulation

- Bus is assigned to the selected Clock or Strobe



Bus Setup and Simulation

• Derating:

The image shows a 'Signal Bus Setup' dialog box. The 'Derating Table File' field is highlighted with a red circle and contains the text 'ddr3_dq_derating.dat'. Below this, there are tabs for 'Assign Bus Component Buffer Models', 'Select Clocks or Strobes', and 'Assign Bus Xnets to Clocks or Strobes'. The 'Assign By' section has 'Model Selector' selected. A table below shows the assignment of buffer models to components.

Component Model	Model Selector	Driver	Active Receiver	Standby Receivers
MT41J128M8HX	V48C_DQ	V48C_DQ_40_ODT60	V48C_DQ_40_ODT60	V48C_DQ_40_ODT60

At the bottom, the 'Buffer Model To Be Assigned' section shows 'V48C_DQ_34' selected in three dropdown menus, with 'Assign' buttons below each. Other buttons include 'Export...', 'Import...', 'OK', 'Apply', 'Cancel', and 'Help'.

Bus Setup and Simulation

- DDR2 Derating table from Micron Data sheet



1Gt

Table 33: DDR2-667/DDR2-800/DDR2-1066 t_{DS} , t_{DH} Derating Values v
All units are shown in picoseconds

DQ Slew Rate (V/ns)	DQS, DQS# Differential Slew Rate											
	2.8 V/ns		2.4 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns	
	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}
2.0	100	63	100	63	100	63	112	75	124	87	136	99
1.5	67	42	67	42	67	42	79	54	91	66	103	78
1.0	0	0	0	0	0	0	12	12	24	24	36	36
0.9	-5	-14	-5	-14	-5	-14	7	-2	19	10	31	22

- CSV format to read into Allegro PCB SI

```
# Derating table for DDR2 DQ 667/800
DQS_SLEW,0.8,1.0,1.2,1.4,1.6,1.8,2.0,2.4,2.8
DATA_SLEW,0.4,0.5,0.6,0.7,0.8,0.9,1.0,1.5,2.0
SETUP_DERATING_TABLE
-28,12,38,50,59,67,72,139,172
-40,0,26,38,47,55,60,127,160
-52,12,14,26,35,43,48,115,148
-64,-24,2,14,23,31,36,103,136
HOLD_DERATING_TABLE
-116,-53,-11,18,41,58,72,114,135
-128,-65,-23,6,29,46,60,102,123
-140,-77,-35,-6,17,34,48,90,111
-152,-89,-47,-18,5,22,36,78,99
```





DDR2 RDIMM

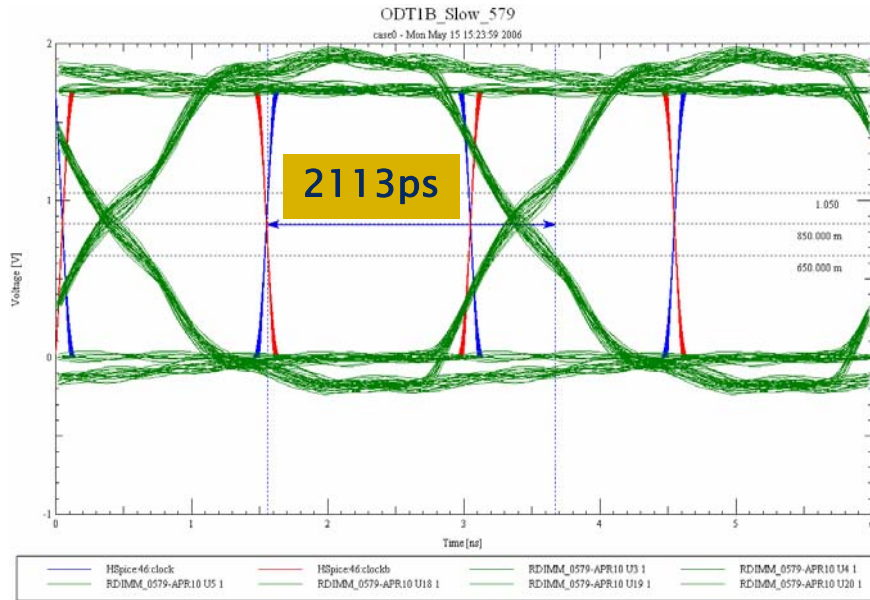
Post Register Timing Budget

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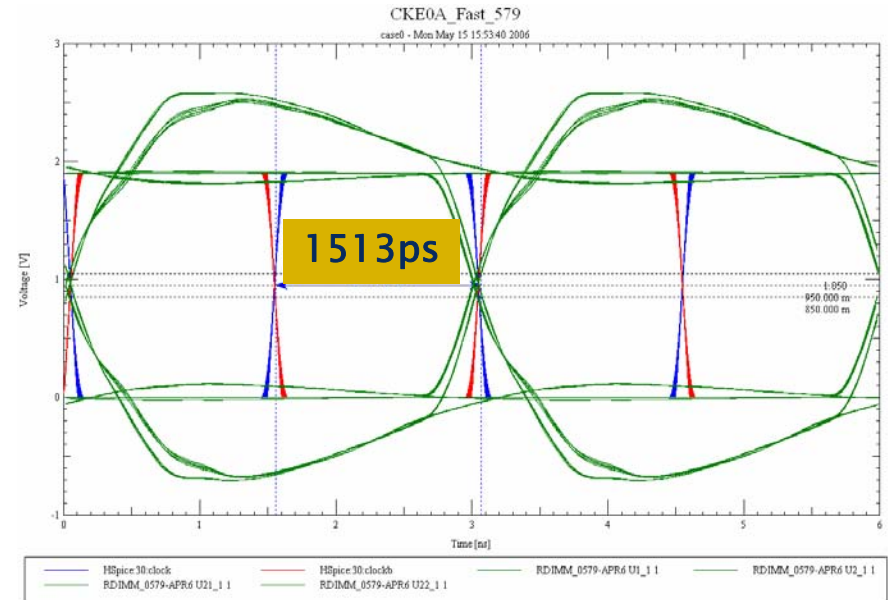


DDR2 Post Register Simulation Hspice Simulation

Slow Corner



Fast Corner



Timing Budget for DDR2 RDIMM

- Register clock to output is determined from the Simulation
- Helps in getting more accurate timing budget
- Tlsim can also be used to come up with the Timing Budget

Timing Budget				
Description	Symbol	Setup(ps)	Hold(ps)	
Clock Period	tCLK	3000	N/A	
Measured Delay: Clock to Actual Load	tPD	-2113	1513	Reg_Clk at Vref to Receiver at AC / DC
Simultaneous Switching Adder	tSS	-200	N/A	Register Spec
*Cross Talk Adder	tXTALK	-50	-50	Estimated for non-XTALK SIMM
Intersymbol Interference	tISI	N/A	N/A	Included in tPD
Clock Skew	tSKEW	-150	-130	PLL jitter/skew + PCB clk skew
Register Clock Shift	tREG	-100	-100	Register clock input skew
DRAM Setup/Hold (derating values)	tISb/tIHb	-200	-275	DRAM Spec @ ac/dc thresholds
Derating		-100	-94	
* Register Clock Offset		0	0	As needed to help setup or hold
Margin (worst case corners)	tM	87	864	Unit: ps



DDR3 RDIMM

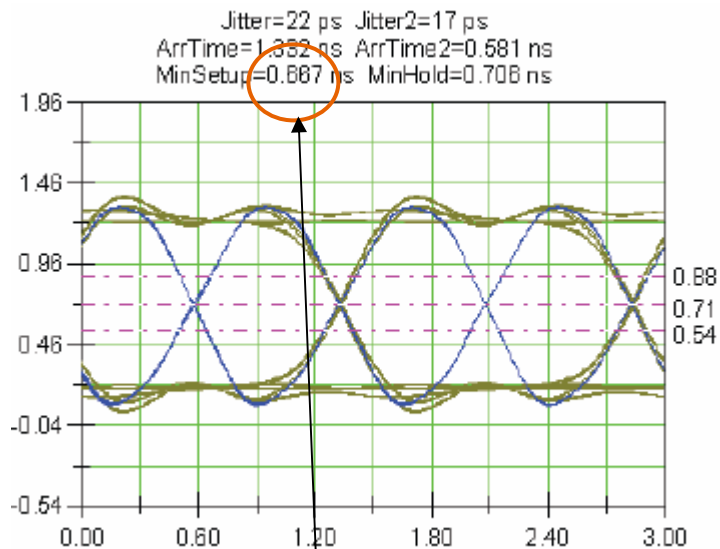
Post Register Timing Budget

9/17/2007



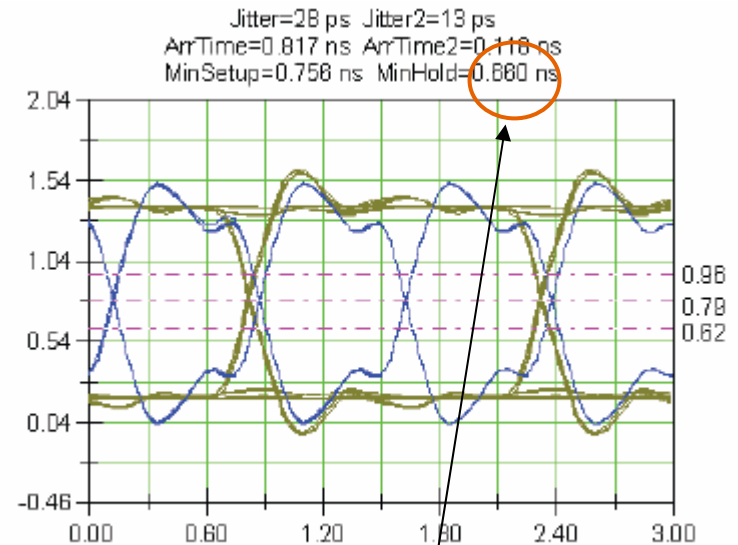
DDR3 Post Register Simulation

Address Net in Slow Corner



Minimum Setup Region

Control Net in Fast Corner



Minimum Hold Region

Note: Used proprietary Micron tools to plot the data from Allegro PCB SI

Timing Budget for DDR3 RDIMM

Timing Budget at 667MHz - Clock at 50%		
	Setup(ps)	Hold(ps)
Measurement	667	660
DRAM setup/hold @ 667MHz Clock	50	125
Timing offset for VREF error (30 mV) based on min. slew rate (30mv / 2.40 v/ns)	13	
Timing offset for VREF error (30 mV) based on min. slew rate (30mv / 3.36 v/ns)		9
DRAM derating	88	50
tjit(hper) half period jitter from register	50	50
tQSK1 for Register (includes SSO for inverted outputs)	200	100
xtalk	16	16
Margin available for Clock placement error (at 50% point)	250	310



Comprehensive Simulation

In Allegro PCB SI

9/17/2007



Crosstalk Report in Allegro PCB SI

Analysis Report Generator (case3)

Standard Report | Custom Report

Case Selection
Current Case : case3 : case2 + unknown change in 'C:\Cadence\SPB_...

Report Types

Reflection Summary Parasitics Segment Crosstalk
 Delay SSN Crosstalk Summary
 Ringing SDF Wire Delay Crosstalk Detailed
 Single Net EMI

Fast/Typical/Slow Mode
 Fast Typical Slow Fast/Slow Slow/Fast

Primary Net
 Net Selection: All Selected Nets
 Driver Selection: Fastest Driver

Aggressor
 Switch Mode: Odd
 Net Selection: All/Group Neighbors
 Driver Selection: All/Group Neighbors
 Each Neighbor

Reflection Data Simulation
 Type: Reflection Measurement: Pulse
 Comprehensive Odd Rise/Fall
 Comprehensive Even Custom Stimulus
 Comprehensive Static Custom Stimulus
 Use Timing Windows Save Circuit Files Save Waveforms

Create Report

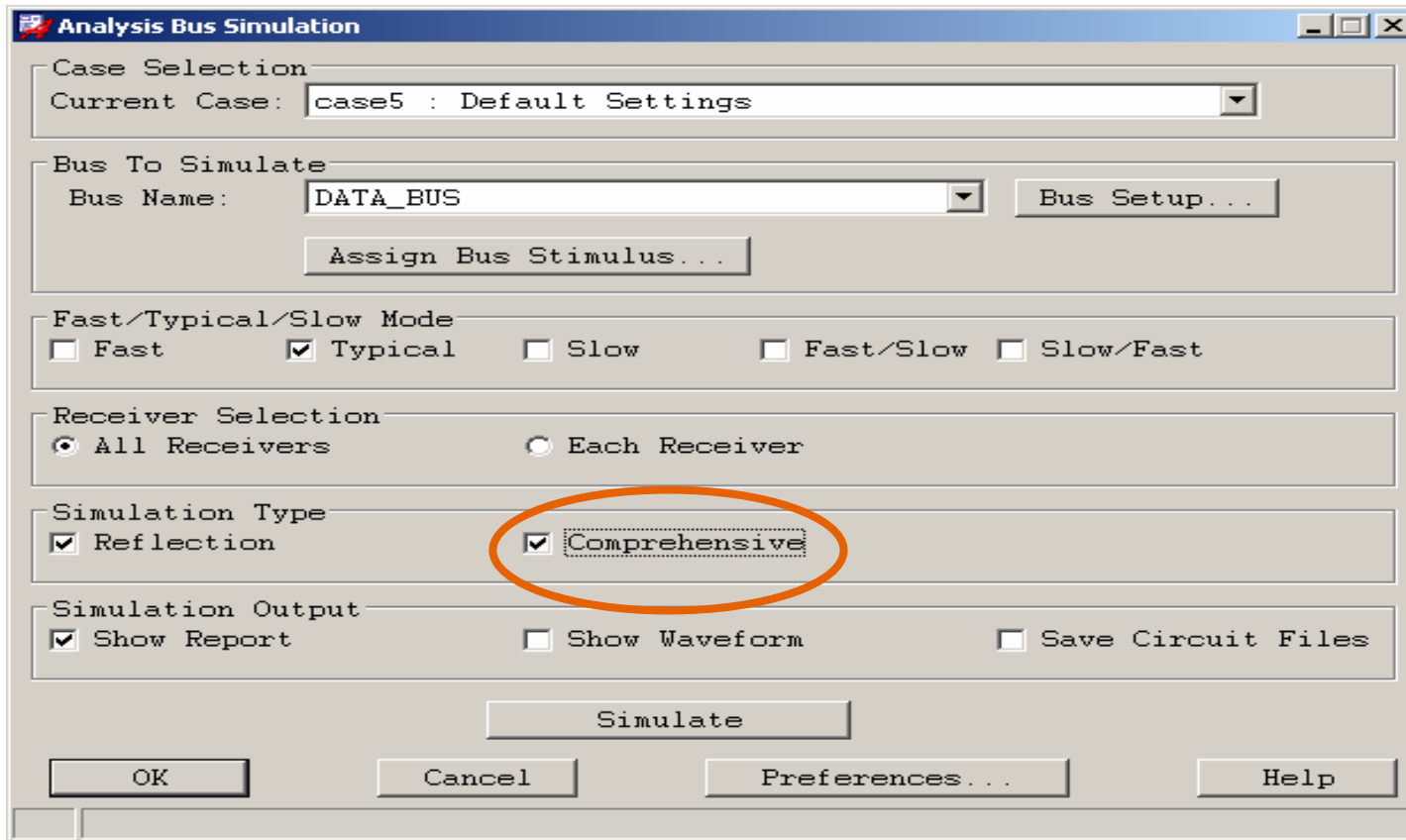
OK Cancel Preferences... Help

```
#####
# Allegro PCB SI XL
# 15.7 s039 (v15-7-42B[1/5/2007])
#
# (c) Copyright 1998-2004 Cadence Design Systems Inc.
#
# Report: Standard Crosstalk Summary Report Sorted By Worst Case Crosstalk
# Tue Apr 17 22:59:07 2007
#####
```

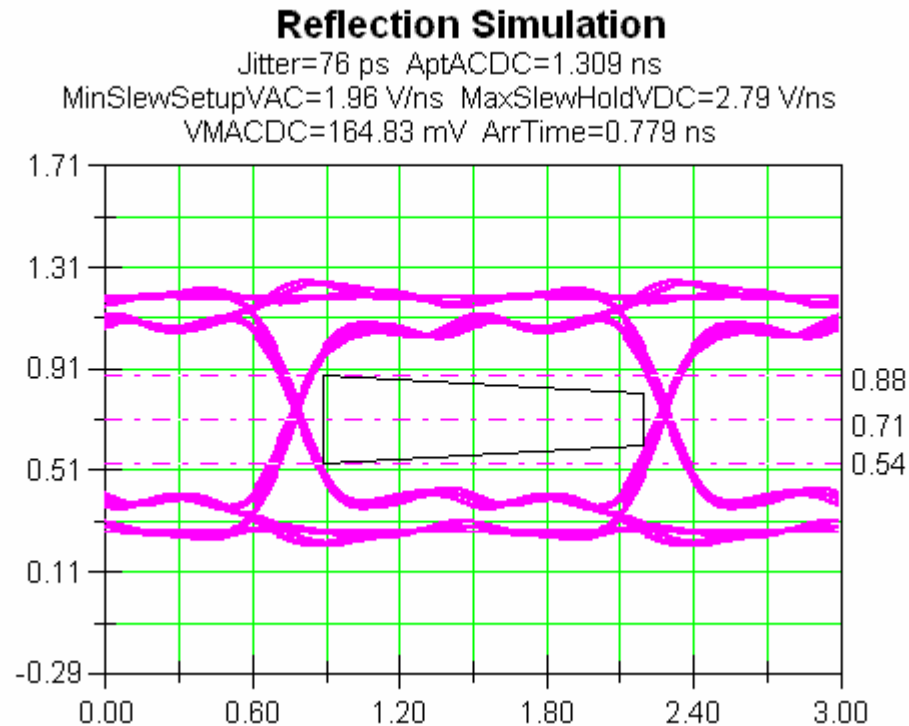
All	Neighbors	Crosstalk	(mV)	(Typ	FTSMODE)	*****			
Victim	XNet	Victim	Drvr			HSOddXta	HSEvenXtr	LSOddXtal	LSEvenXtalk
2	0550AA_1	A10B	0550AA_1	U7	M11	80.82	NA	79.57	NA
2	0550AA_1	A15B	0550AA_1	U7	K11	72.43	NA	69.93	NA
2	0550AA_1	A3A	0550AA_1	U7	F2	65.76	NA	62.56	NA
2	0550AA_1	BA1A	0550AA_1	U7	G2	65.14	NA	62.23	NA
2	0550AA_1	A10A	0550AA_1	U7	M1	57.26	NA	53.51	NA
2	0550AA_1	A6A	0550AA_1	U7	C2	51.38	NA	49.29	NA
2	0550AA_1	CKE1B	0550AA_1	U7	M10	50.14	NA	48.21	NA
2	0550AA_1	BA2B	0550AA_1	U7	J11	48.79	NA	47.9	NA
2	0550AA_1	WEA	0550AA_1	U7	L1	48.45	NA	45.77	NA
2	0550AA_1	A6B	0550AA_1	U7	C10	47.6	NA	45.28	NA
2	0550AA_1	CASA	0550AA_1	U7	N1	46.96	NA	44.98	NA
2	0550AA_1	A5A	0550AA_1	U7	D2	42.43	NA	40.44	NA
2	0550AA_1	A1A	0550AA_1	U7	F1	39.07	NA	37.54	NA

Crosstalk in PCB SI V. 16.0

• Comprehensive Bus Simulation



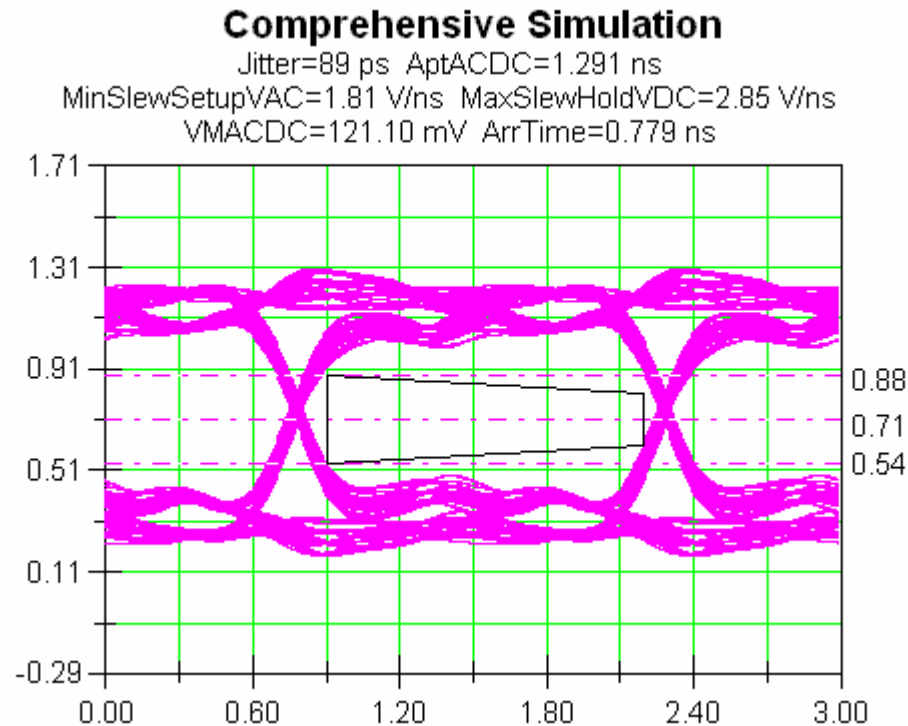
Reflection Simulation in DDR3



Note: Used proprietary Micron tools to plot the data from Allegro PCB SI

Comprehensive Simulation in DDR3

- As an Example following settings were used to run Comprehensive Simulation:
 - Geometry Window = 40 mil
 - Min. Coupled Length = 50 mil
 - Neighbor Capacitance = 0.01 pF



Note: Used proprietary Micron tools to plot the data from Allegro PCB SI



S-Parameter Package Model

In Allegro PCB SI

9/17/2007

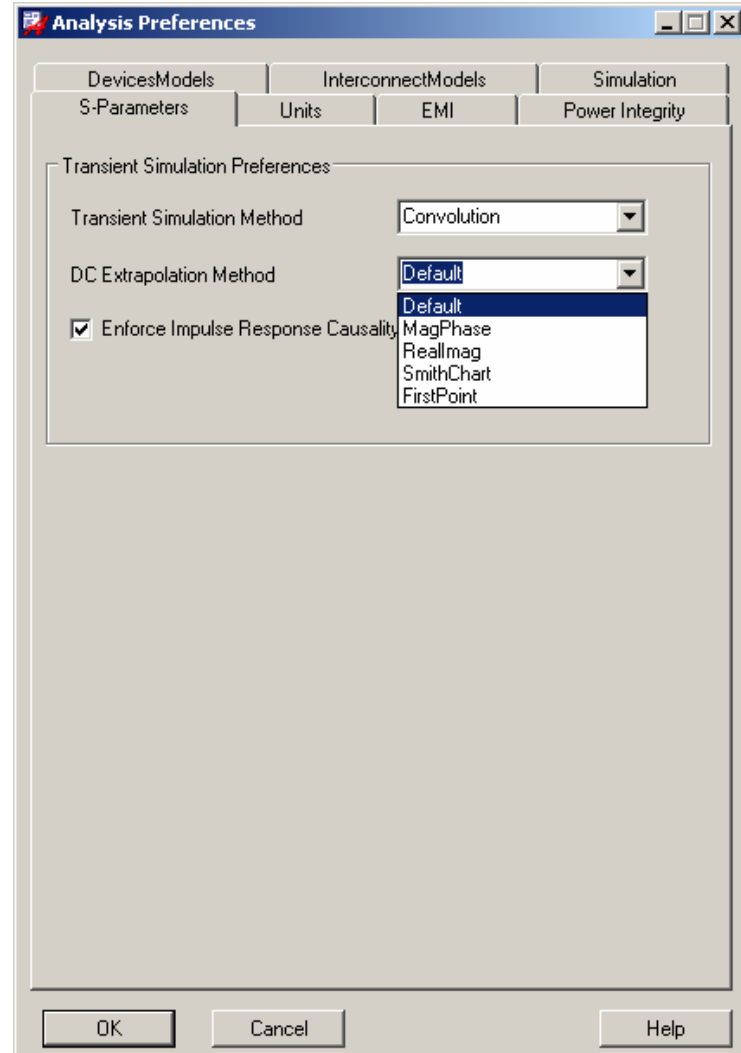


S-Parameter

- Scattering Parameters are normally referred as S-Parameters.
- Relates to a traveling waves that are scattered or reflected when an n-port network is inserted into a transmission line.
- S-Parameter models are frequency domain and they describe the behavior of a set of ports at different frequencies.

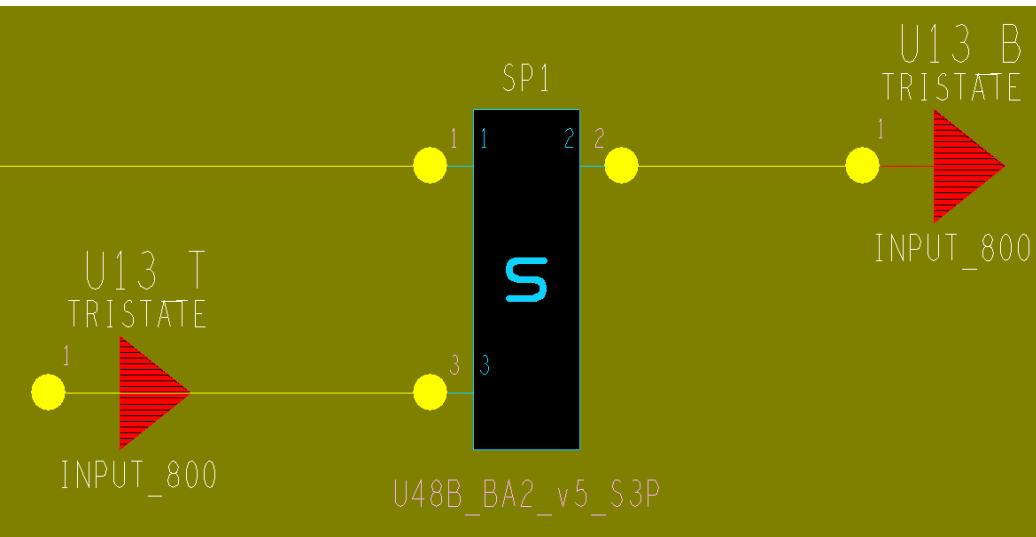
S-parameter in Allegro PCB SI

- PCB SI V. 16.0 has:
 - DC Extrapolation Options
 - Causality
 - Passivity Check



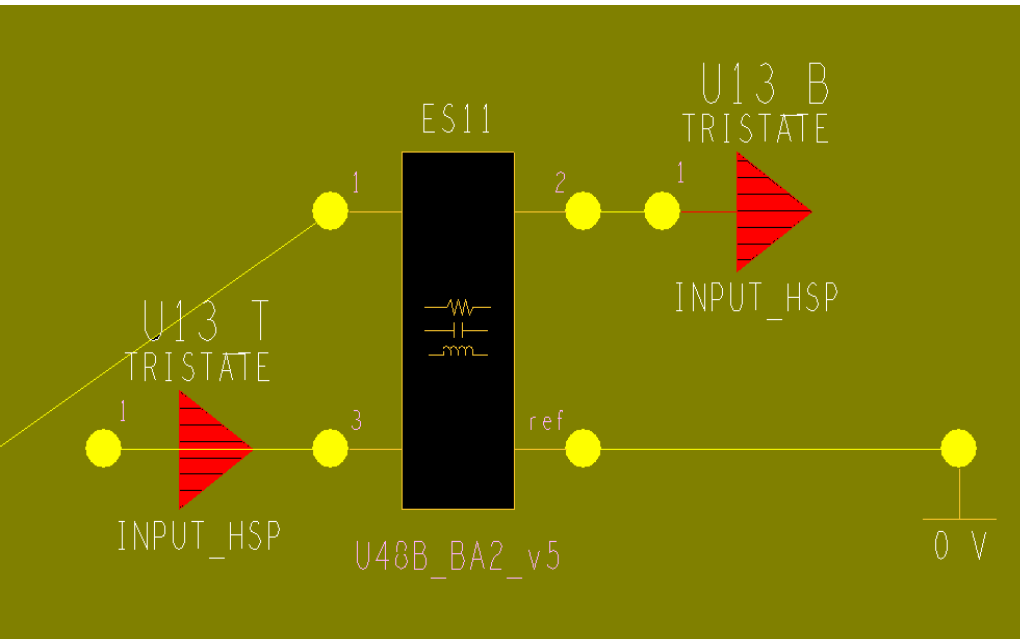
Using Allegro PCB SI GXL

- Tlsim Engine is used for simulation.
- The converted .dml file from a touchstone file is shown here as black box with letter "S" in Sigxp .



Using Allegro PCB SI XL

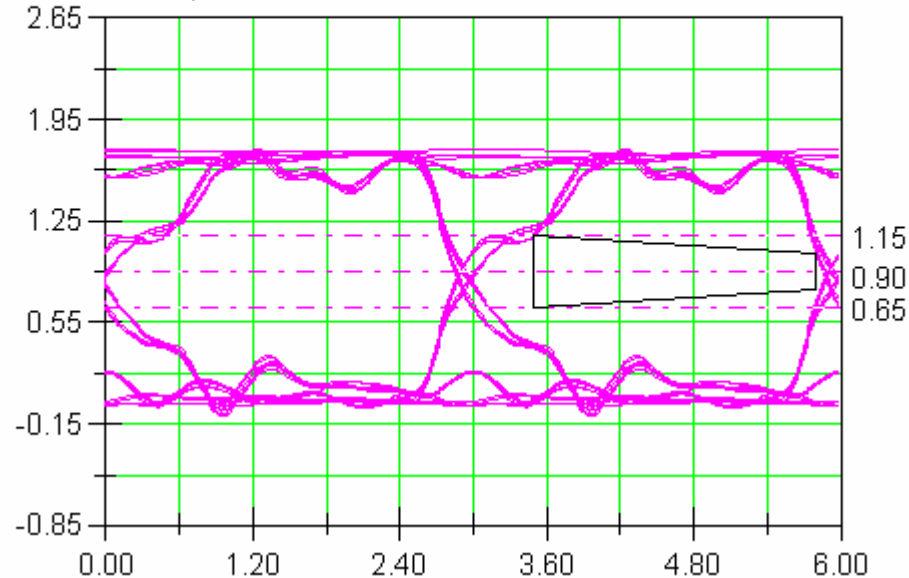
- Hspice Engine is used for Simulation
- The converted .dml file from a touchstone file is shown here as black box in Sigxp



Simulation With Lumped Package Model

Lumped Package Model

Jitter=194 ps MaxSlewSetupVAC=1.74 V/ns
MaxSlewHoldVDC=2.47 V/ns AptACDC=2.304 ns
AptAC/DCCtr=4.637 ns ArrTime=2.940 ns

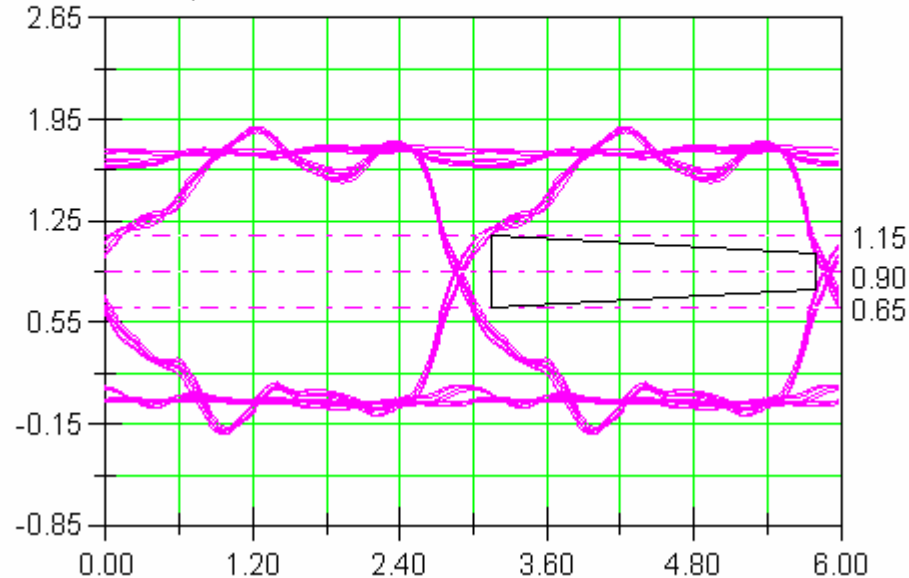


Note: Used proprietary Micron tools to plot the data from Allegro PCB SI

Simulation With S-Parameter Package Model

S-Parameter Package Model

Jitter=99 ps MaxSlewSetupVAC=1.90 V/ns
MaxSlewHoldVDC=2.48 V/ns AptACDC=2.625 ns
AptAC/DCctr=4.465 ns ArrTime=2.886 ns



Note: Used proprietary Micron tools to plot the data from Allegro PCB SI



Correlation

Lab versus Simulation

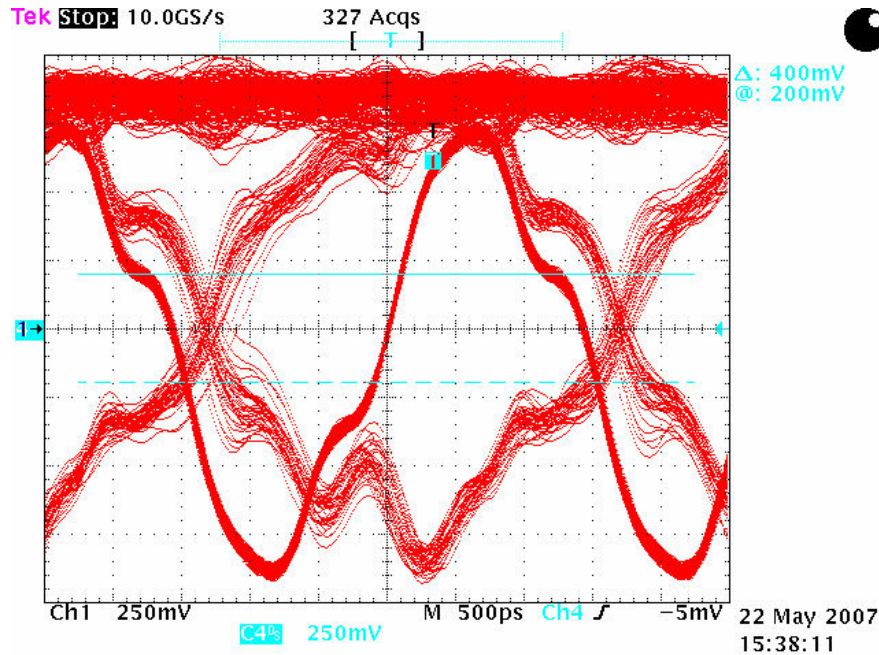
9/17/2007



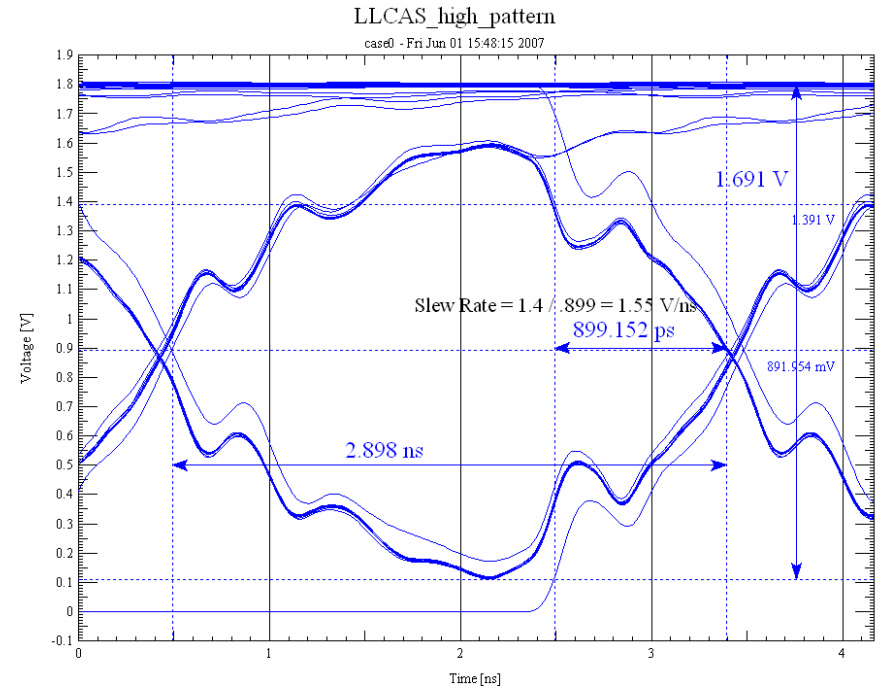
DDR2 RDIMM System Verification

Lab Measurements versus Simulation Correlation on Address Net in a RDIMM DDR2 Card .

Lab Measurements



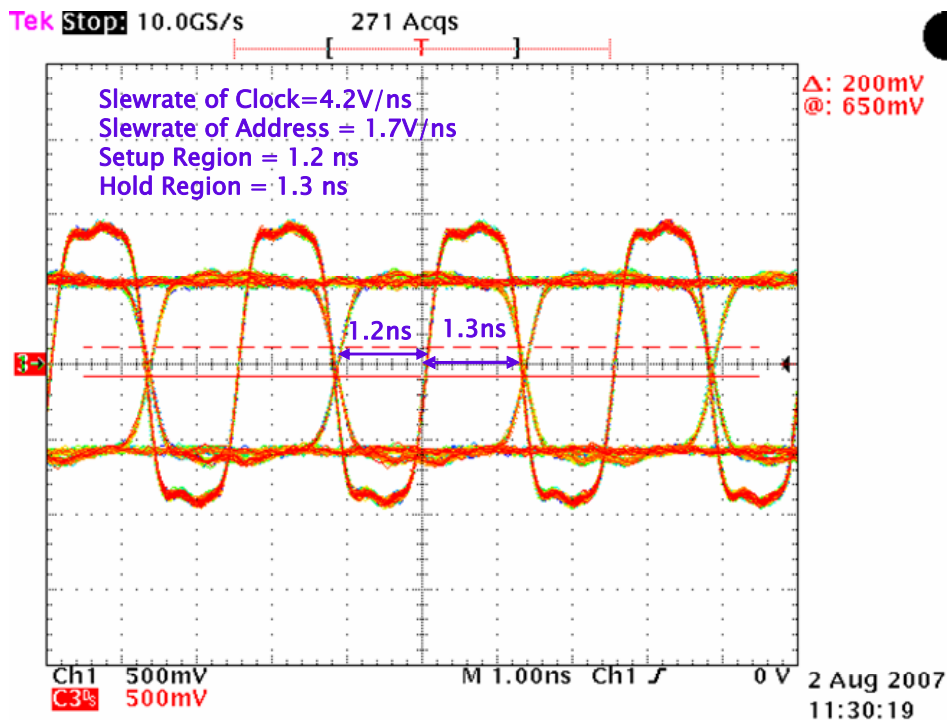
Simulation (Uncoupled)



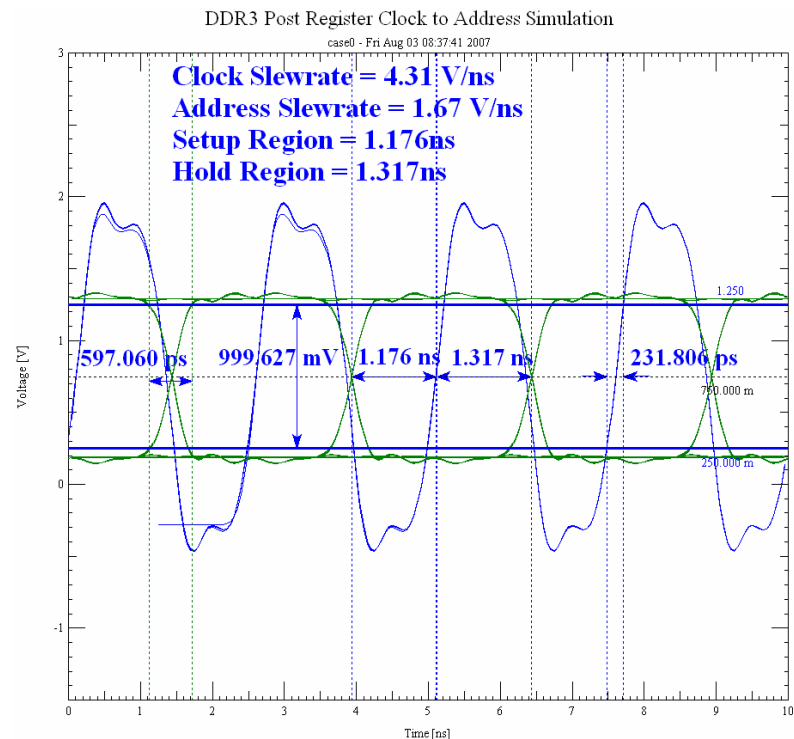
DDR3 RDIMM System Verification

Lab Measurements versus simulation correlation on Address Net in a RDIMM DDR3 Card.

Lab Measurements



Simulation (Uncoupled)



Summary

- The challenges in designing with
 - ▶ DDR2 reside in signal integrity
 - ▶ DDR3 reside in timing
- Due to Tree Topology DDR2 signals arrive at the same time in every DRAM even though it has less bandwidth
- Due to DDR3 fly-by topology, timing skews exist from DRAM-to-DRAM
 - ▶ therefore it is more challenging for the DDR3 controller to match timing even though it has a larger bandwidth
- Allegro PCB SI
 - ▶ Can be used to design DDR3 with timing issues
 - ▶ Following enhancements in 16.0 make it easy to get silicon-accurate timing data
 - Comprehensive Simulation
 - Slewrate derating
 - Ease of use improvements with Bus Setup



CONNECT: IDEAS

CDNLive! 2007 Silicon Valley