

CDNLive 2007: Session #: 8.8

3D S-parameter Simulation with Allegro SI

Presented By:

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www.sedonaii.com

In this session attendees will discover several places where simulation accuracy can be improved by incorporating S-Parameter models of 3D structures such a Connectors and Ball Grid Array (BGA) pin fields. Attendees will also see how 3D modeling and S-Parameter generation and simulation is greatly simplified by the combination of Allegro SI and CST Microwave Studio.

The session will include comparisons of real DDR2 and SERDES cases with and without 3D models. Attendees will learn that improved accuracy will affect some of the engineering tradeoffs made during the design and layout process.

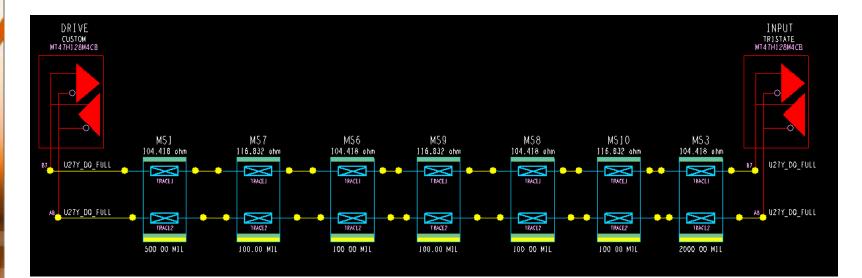
2D - 2 ½ D - 3D

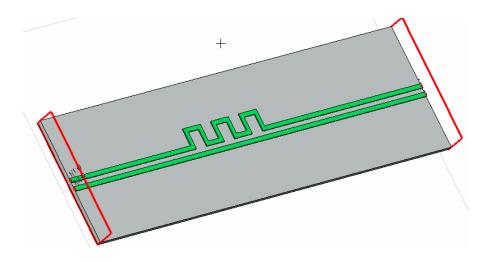
- Much of engineering is about tradeoffs
- SI simulation tradeoff is speed for fidelity
 - Large size = slow speed
 - Large detail = slow speed
- Hard to setup = VERY slow speed
 - Is a one week setup worth it?



- Optimized simulators add tremendous value
 - Allegro SI
 - CST Microwave Studio

Serpentine Example DDR2 DQS

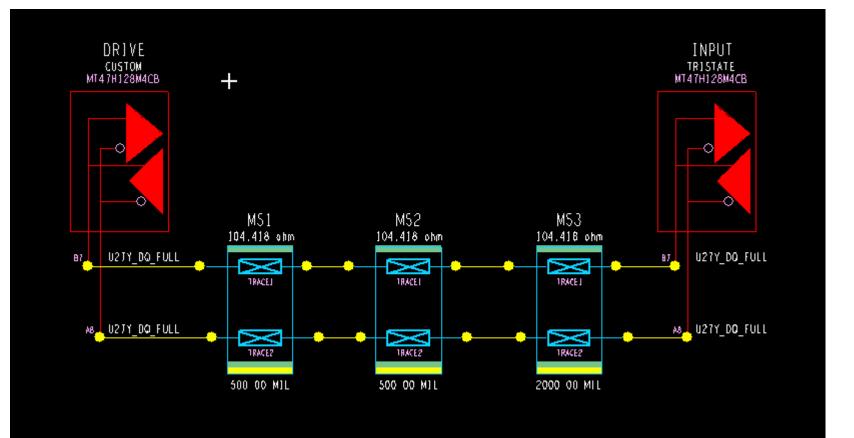




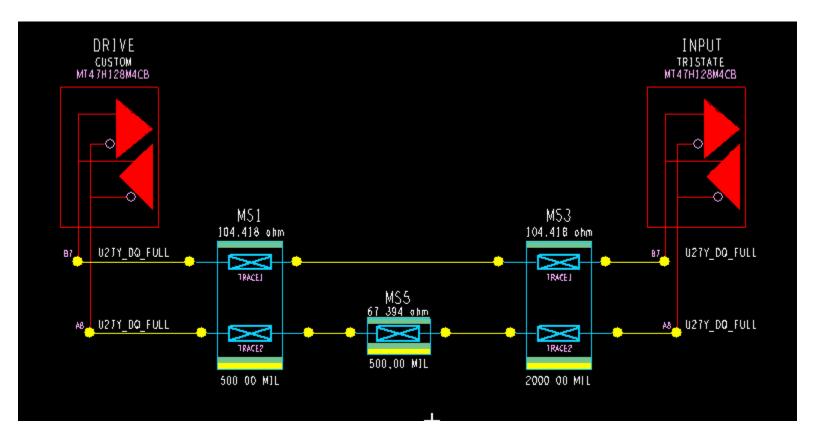
Verify Allegro SI in Combination with CST

- Verify with a simple example
- Build an understanding of how to blend two environments
- Verification allows for extrapolation to unknown cases

Simulation Setup: Decompose into 3 Lengths

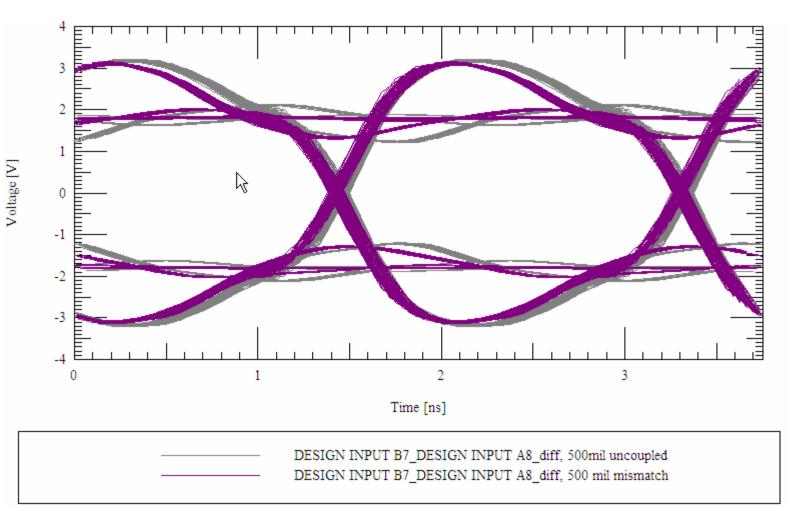


Length Mismatch



500 mil trace removed from Diff pair

Mismatch Results

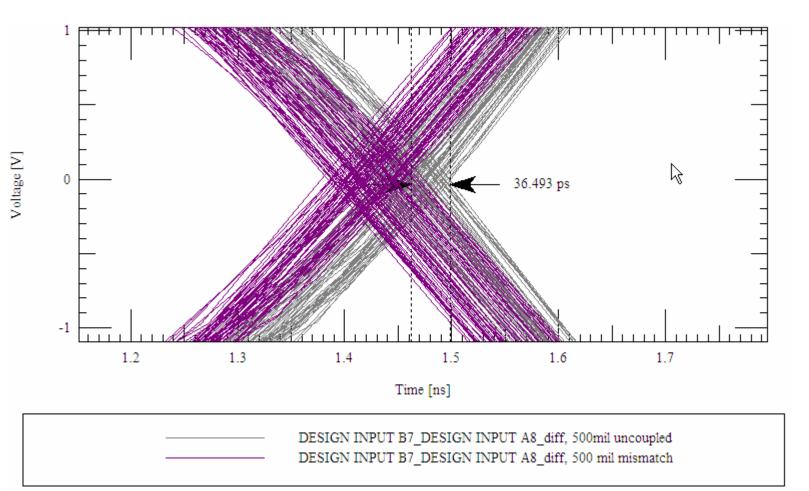


Very small impact on wave shape

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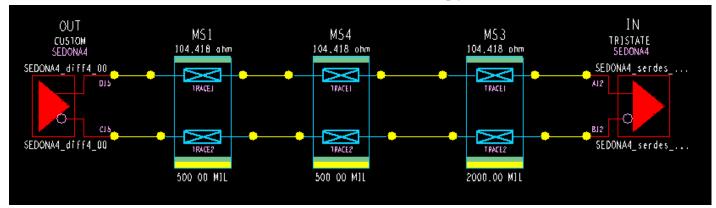
500mil Time Delay



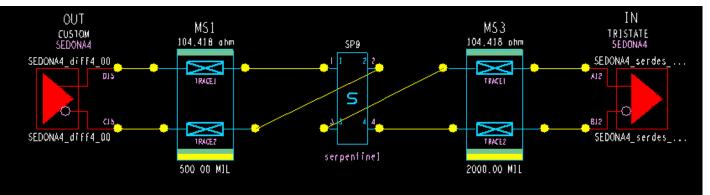
Allegro SI Diff Normalizes the data 36.5 x 2 = 73ps or 500mils

Simulation Topologies

Reference topology

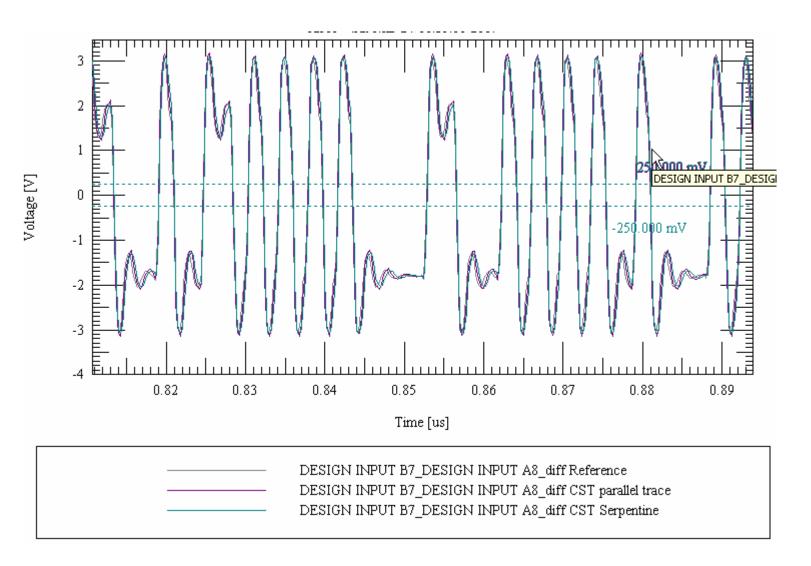


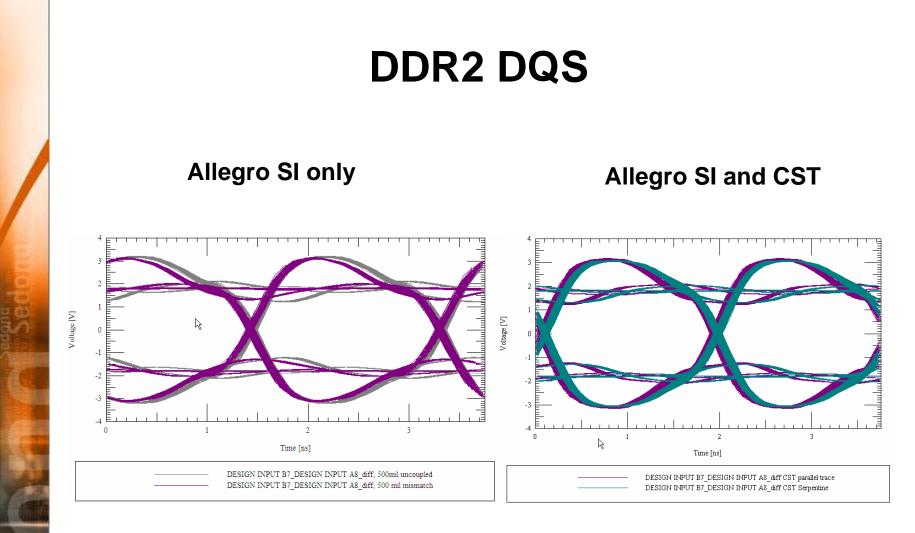
S-Parameter simulation model from 3D extraction



S-Parameter models are touchstone files

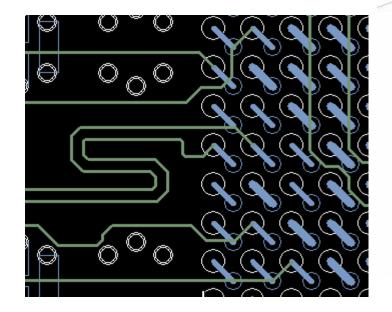
Time vs Voltage



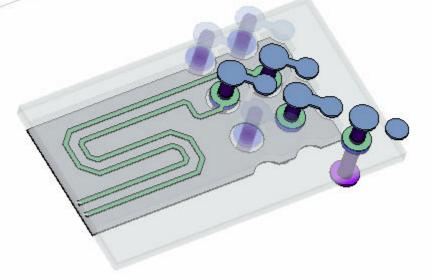


Almost no difference at DDR2 speeds What about Gigabit speeds?

Gigabit Example; PCB in 3D, End Match

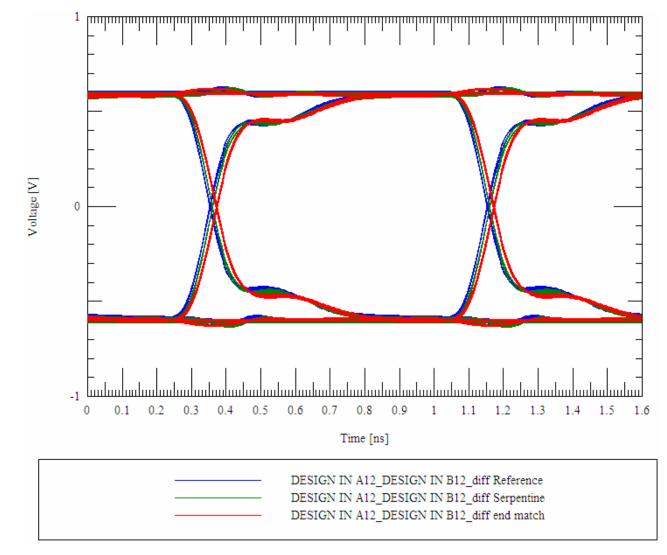




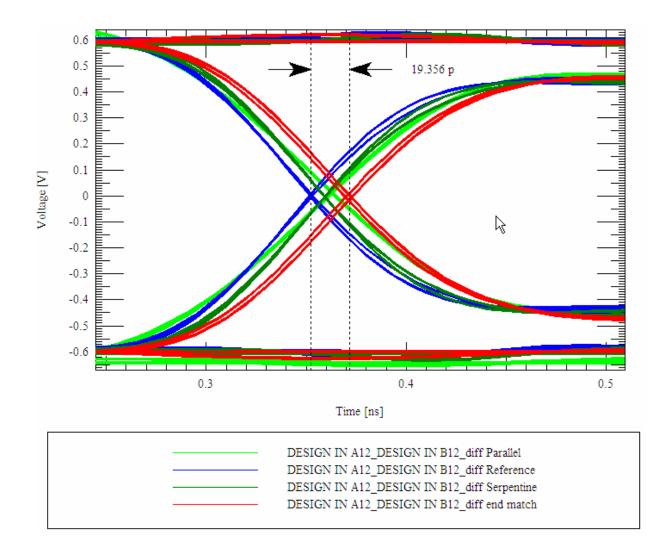


3D extraction in CST Microwave Studio

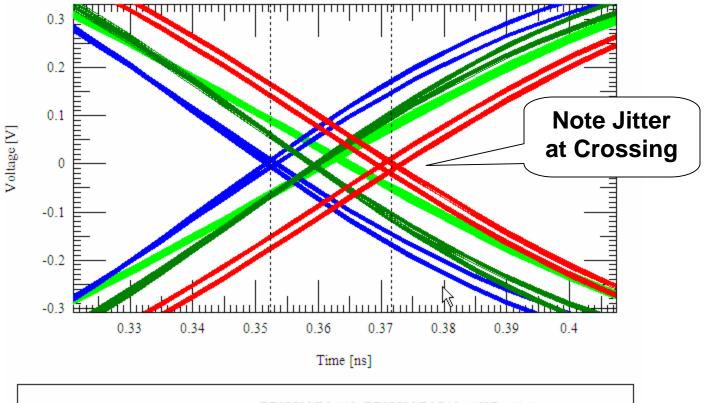
Random 256 Bit Eye



Random 256 Bit Eye Zoom Overlay

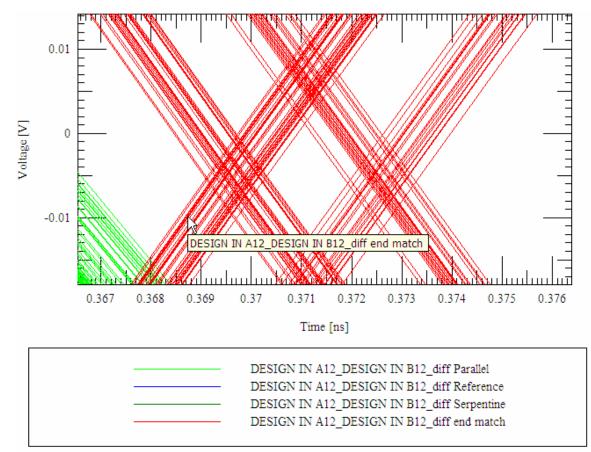


Random 256 Bit Eye Zoom



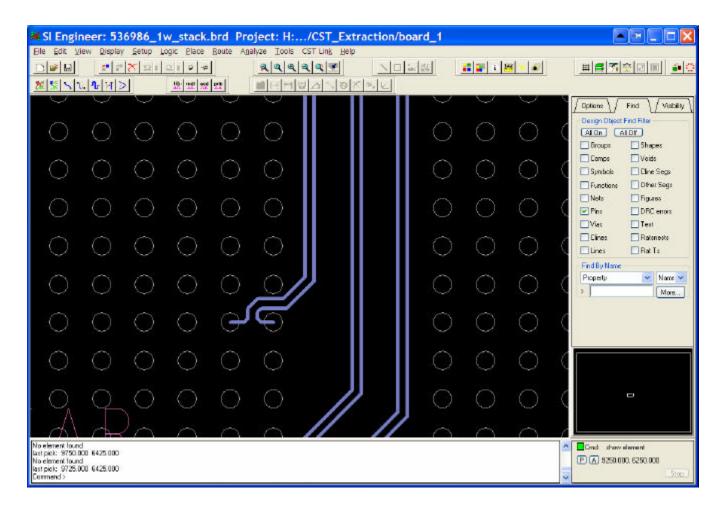
 DESIGN IN A12_DESIGN IN B12_diff Parallel
 DESIGN IN A12_DESIGN IN B12_diff Reference
 DESIGN IN A12_DESIGN IN B12_diff Serpentine
 DESIGN IN A12_DESIGN IN B12_diff end match

Jitter Close-up: Data Dependency?



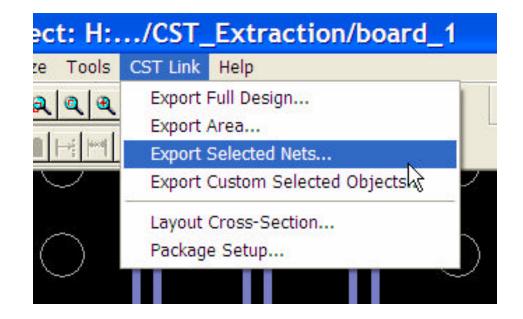
Conclusion: DDR2 speeds minimal effect Gigabit speeds noticeable differences in signal performance

Extracting Data from Allegro



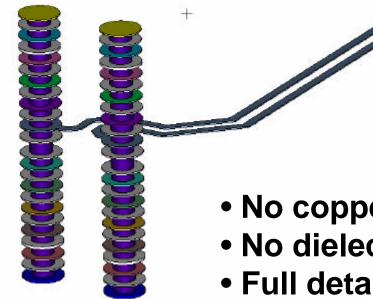
A single Diff pair is of interest on the board

Export Options

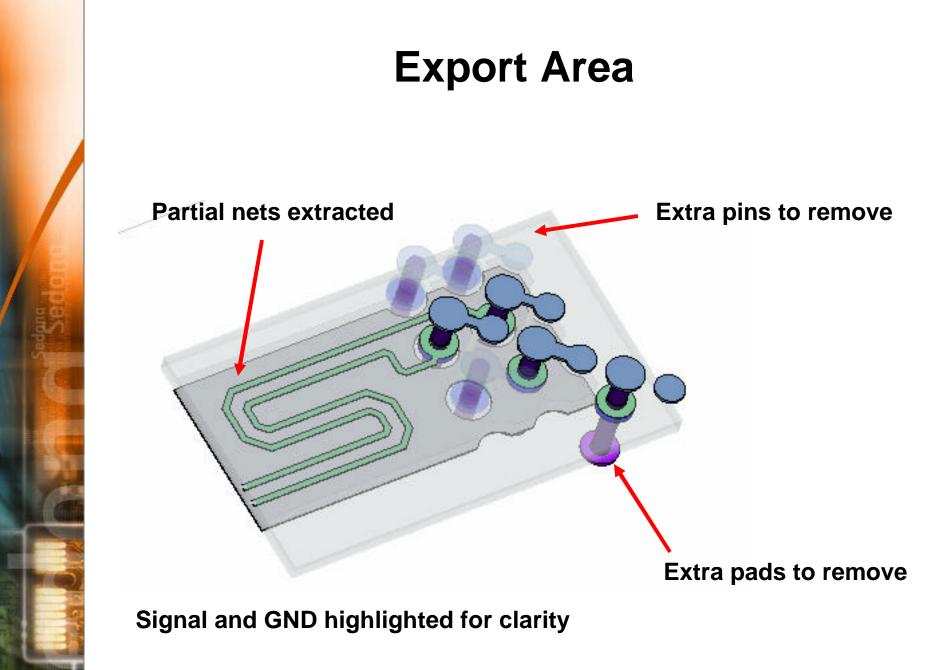


Selecting the correction extraction is important

Export Net



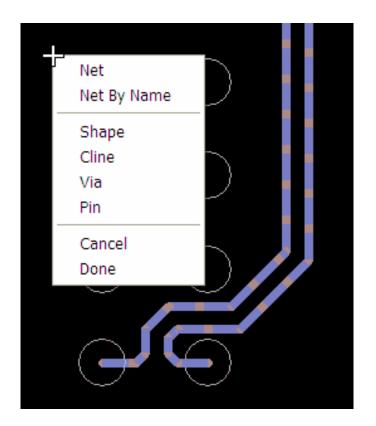
- No copper planes extracted
- No dielectric planes extracted
- Full detail on VIAs



Export Custom Select

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Selected Objects



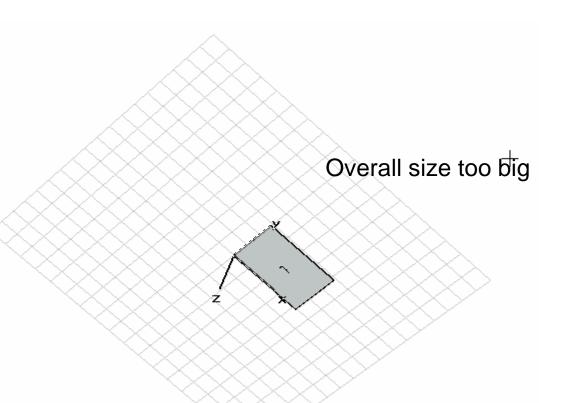
Diff Pair selected by Net Planes selected by Net Name

ETCH_L11_SIG5 Lossy metal 1 5.959e+007 [S/m] 8920 [kg/m^3]

z

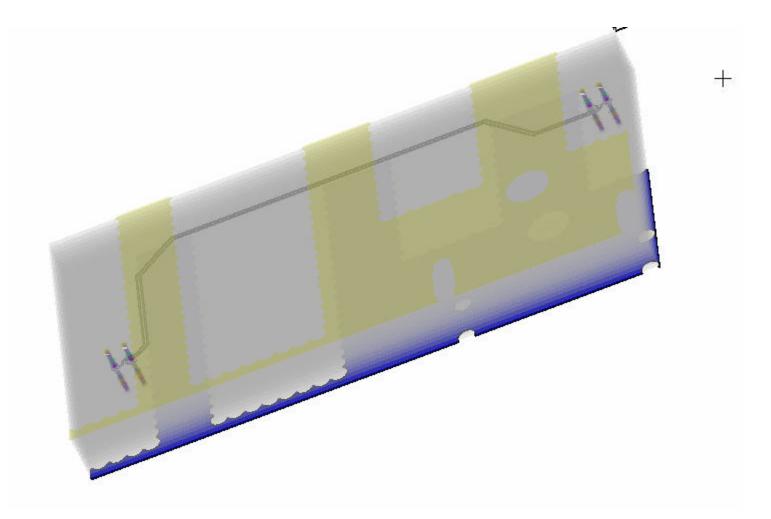
Zoom on Diff Pair

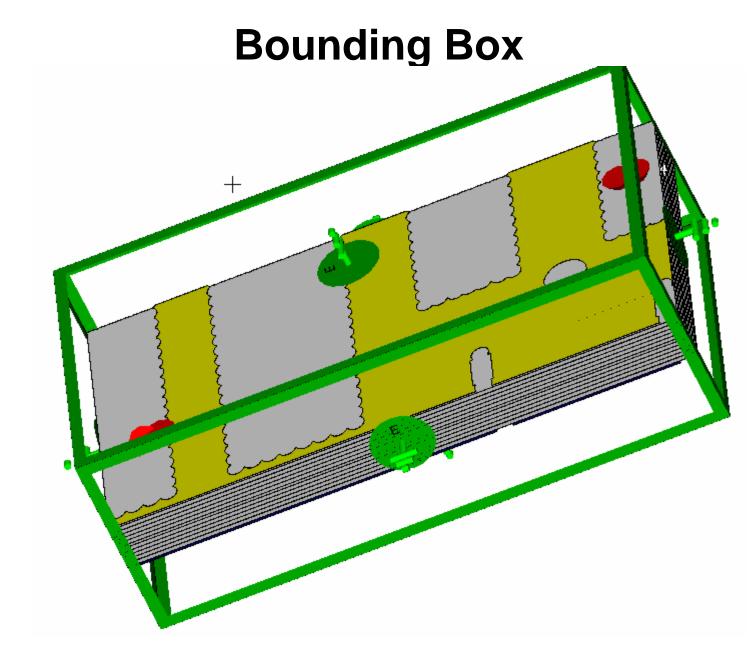




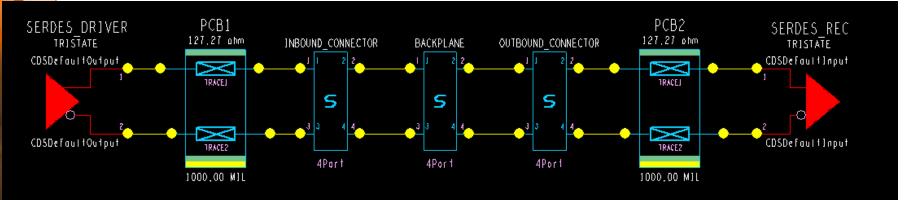
Solution: Add new shapes that overlap with unwanted areas. New shapes are vacuum and merged with 'Insert'

Final Shape



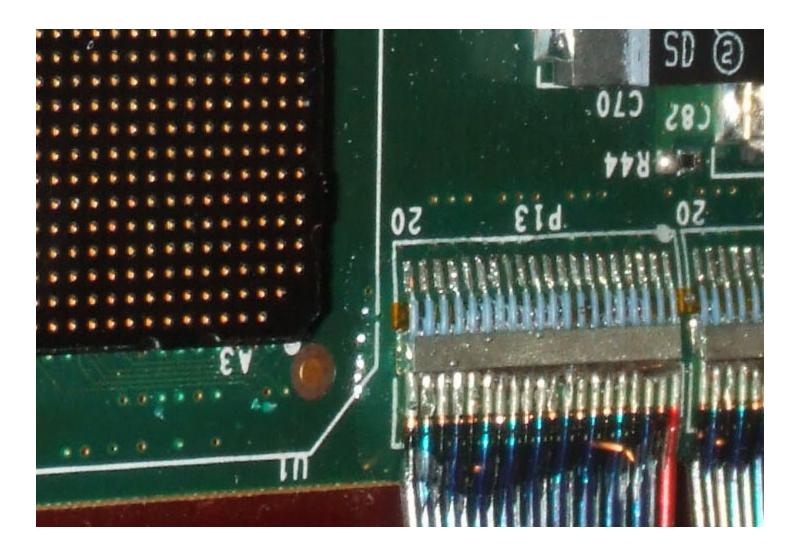


System Level Simulation Example

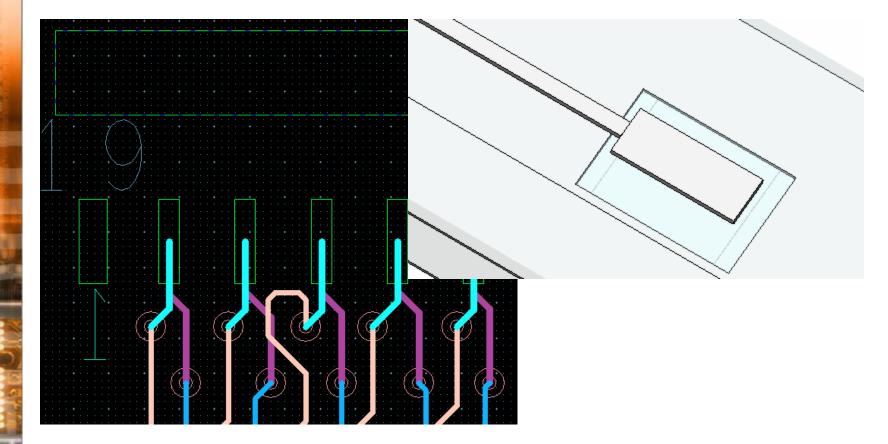




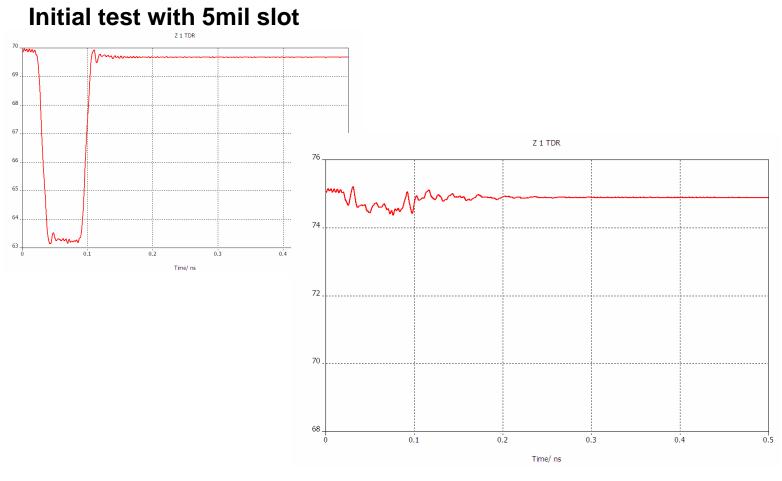
Consider other 3D Connections



Impedance Matching Coax Landing to Etch Transition



TDR Plot from Slot Under Trace



Final optimized slot length and width

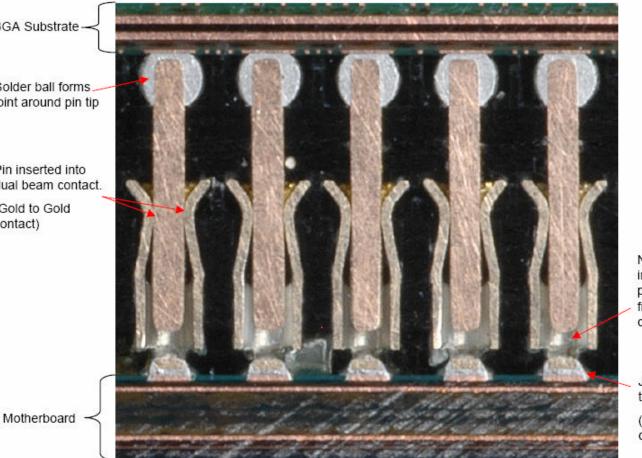
BGA Adapter

HiLo[™] Cross Section - BGA Socketing Application

BGA Substrate

Solder ball forms. joint around pin tip

Pin inserted into dual beam contact. (Gold to Gold contact)



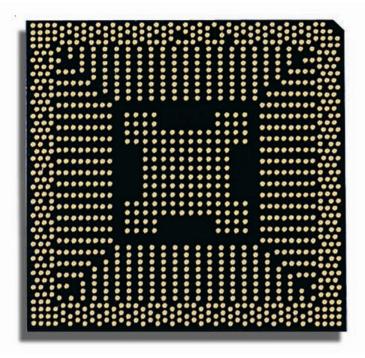
Nickel plating in inside of barrel prevents solder from wicking up contact

J-Lead soldered to motherboard

(J cut off in cross-section)

Low Cost Variable Pitch Custom Connectors

Center pitch is 1mm Inner ring is 1.5mm x 1mm pitch Outer ring is 0.8mm pitch

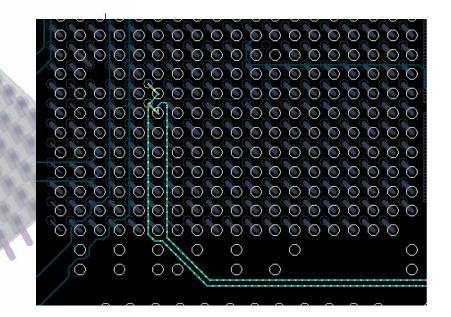


Conclusion:

As custom connectorization decreases in cost and system complexity increases the need for 3D analysis will also increase.

Future Work:

- Study Contribution of Pin Field vs Length Mismatch
- Build Test Structure



Tools Used

- CST Microwave Studio
 - 3D solver for S-Parameters
 - Good Allegro interface
- Cadence Allegro SI
 - Flexible layout tool
 - Good constraint management
- Cadence SigXp
 - Topology viewer
 - Simulation

Results viewer - SigWave ____

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References

- Cadence Design Systems
- CST
- ISI Interconnect Systems Incorporated

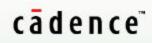
About Sedona International, Inc.

- Specialized Engineering services for complex electronics
 - Electrical, Mechanical and Embedded Software
- Core Strengths
 - Integrated PCB layout and SI Analysis:
 - Chip Board System
 - Subject Matter Experts: right people to the job
- Large company processes, small company feel
 - Wiki, RT, Automated systems
- Serving North America
 - Locations in Boston / Ottawa / Texas

Thank you

Questions

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