Presentation Title:

Next-Generation SoC Architectures Will Include Intrinsic Ability to See Inside Silicon

Description:

In order to dramatically accelerate the silicon validation of new SoC platforms, ST Microelectronics and DAFCA have partnered in the creation and deployment of recently commercialized on-chip instrumentation. ST has long recognized that increased reliance upon block-based IP severely limits the effectiveness of pre-silicon verification, since the "deep state" interactions between once-discrete components are now far too complex to reliably explore in simulation or emulation. Moreover, although the blocks themselves can be thoroughly examined pre-silicon, there are no standards or, until now, automated flows that enabled at-speed, in-system observability of internal signals and block interconnects.

ST and DAFCA have solved this problem by collaborating on an altogether new reference design that can be quickly adapted to a broad variety of consumer and professional applications. The particular video processor prototype is comprised of a standard microprocessor core with several application-specific logic cores, configurable logic subsytems, memory controllers, standard I/O interfaces, and special fault injection capabilities. It also included DAFCA's compact reconfigurable infrastructure fabric to facilitate bus monitoring and, in certain instances, logic control; the fabric requires no extra pins, no special libraries, and no change to the design methodology.

We employed a Cadence Palladium emulation environment to verify the functional logic, as well as to insure script portability between the design environment and at-speed silicon validation and eventual debug. We have created a detailed case study of the reference design including the on-chip, at-speed, in-system infrastructure, whose analysis capability has been previously shown to dramatically shorten silicon validation and subsystem integration. In qualitative terms, we expect to dramatically accelerate system validation and shake-out; more importantly, we can now, for the first time, approach functional misbehaviors methodically, and at bit-level detail, with a infrastructure fabric that is easily re-applied and scaled to other applications.