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Speeding-up HW/SW Co-Development Using HW Emulation

Session#: 1.11

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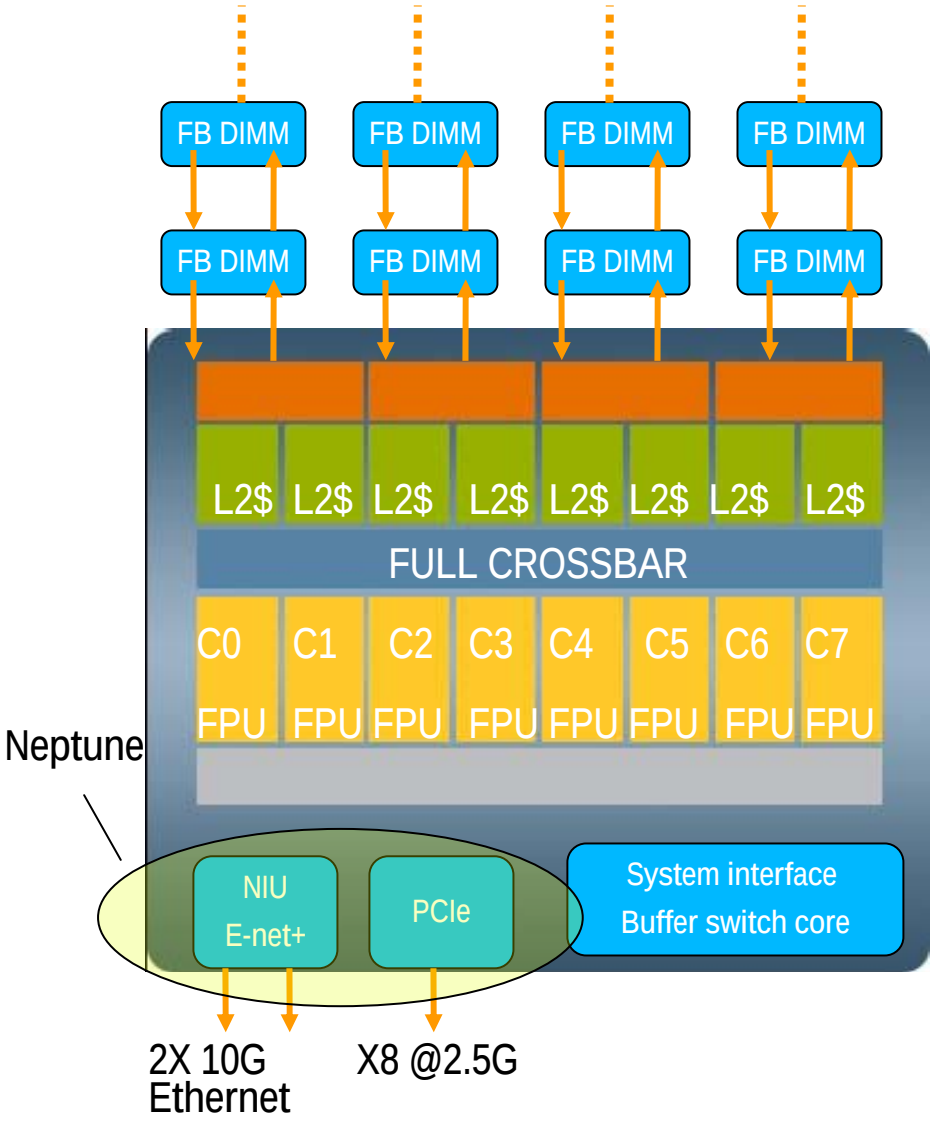
Presentation Outline

- Introduction
- Traditional System Development Methodology
- Verification Platforms
- System Development Methodology with Emulation
- Value Derived
- Summary

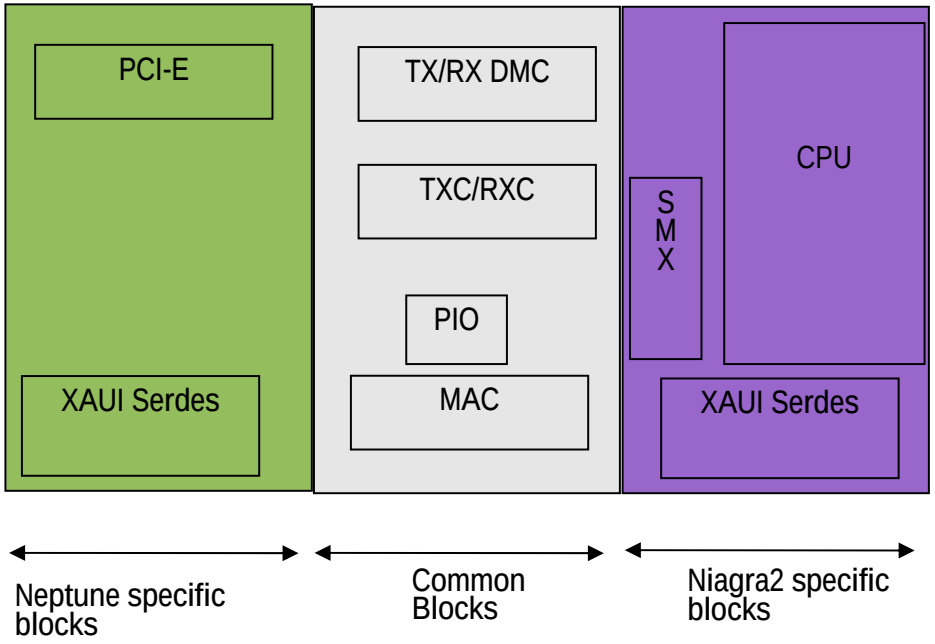
Niagara2: True SoC



- 2x+ performance over UltraSPARC T1, within the same power envelope
- Up to 8 cores @1.4GHz
- 2x the threads
  - > Up to 64 threads per CPU
- 2x the memory
  - > Up to 128GB memory
  - > Up to 16 full buffered Dimms
  - > 2.5x memory BW = 60+GB/S
- 8x FPUs, 1 fully pipelined floating point unit/core
- 4MB L2$ (8 banks) 16 way set
- Security co-processor per core

Neptune Overview

- Sun's unique 10 Gig Ethernet Networking & PCI-Express technology.
- Designed to accelerate multi-core, multi-threaded application performance (CMT CoolThreads)
- It's main features include:
  - Layer 2/3/4 Packet Classification, movement using multiple DMA engines, Virtualization and partitioning functionality
  - Upto 4 multi-speed (up-to 10 Gbps) Ethernet ports line rate.
  - PCIe interface
- Available as discrete ASIC, Atlas host adapter cards or integrated with Niagara2 SoC
- Everything new – HW ASIC, Firmware (device drivers)

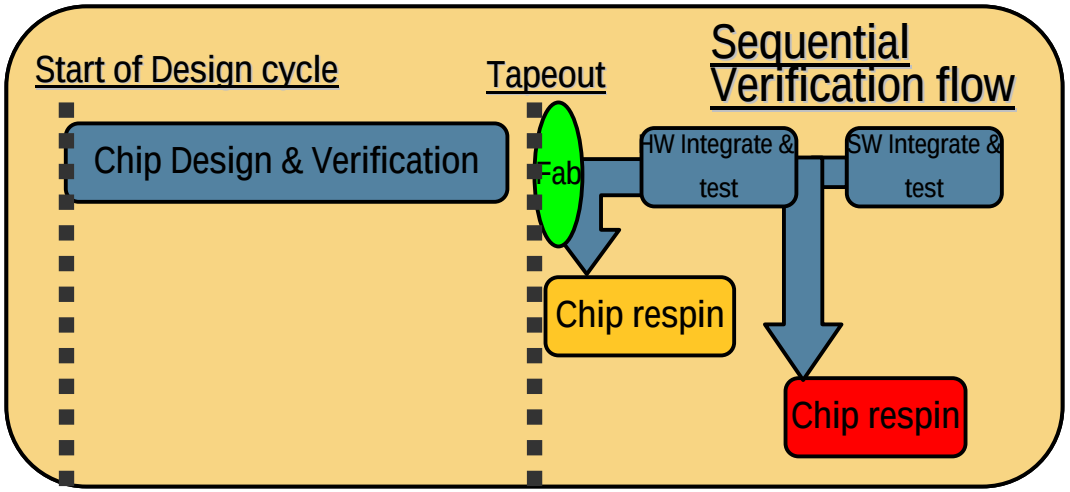


Problem Statement

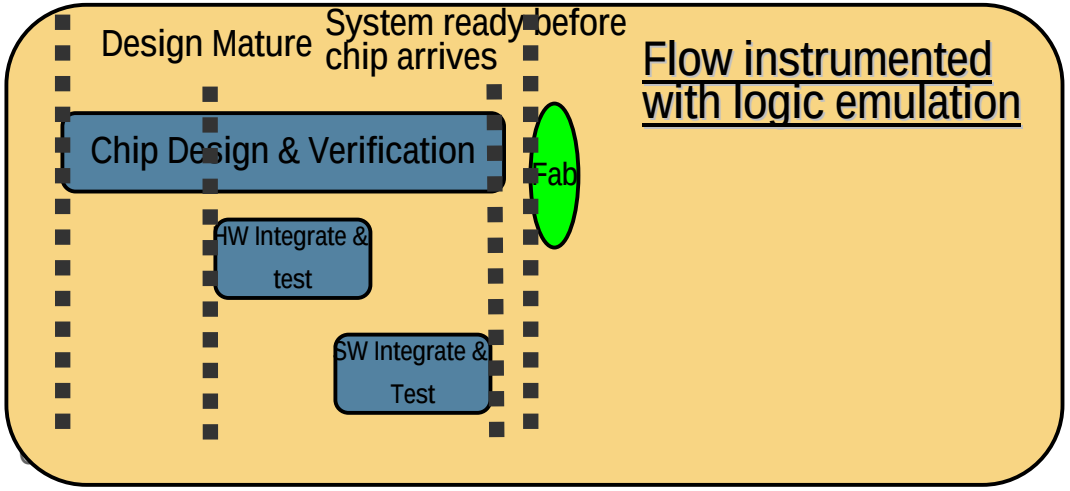
- Traditionally SW validation requires the manufactured design for System Integration & Test
  - > SW and HW validations are sequential tasks:

- Specific problems for Neptune:
  - Classic HW/SW co-simulation dilemma.
  - Everything New – design, host adapter board, firmware.
  - Testing RTL with real-world traffic.
  - Networking chip should be compatible to all the vendors in the industry.

Sequential Verification



Concurrent Verification



Generalised Cost of show-stopper bug analysis:

- Early in design phase: *Almost negligible.*
- Close to tapeout: *Schedule impact.*
- After tapeout: *Few silicon respins, schedule impact.*
- Close to RR: *Loss of revenue at $1+ Million per day.*
- After RR: *Cost of recall at $150 Million per day; Also damages reputation*

Source: N. Winkworth & B.Blohm

Simulation Options

SW Simulator

Simulation Accelerator

Accelerator/ Emulator- Xtreme

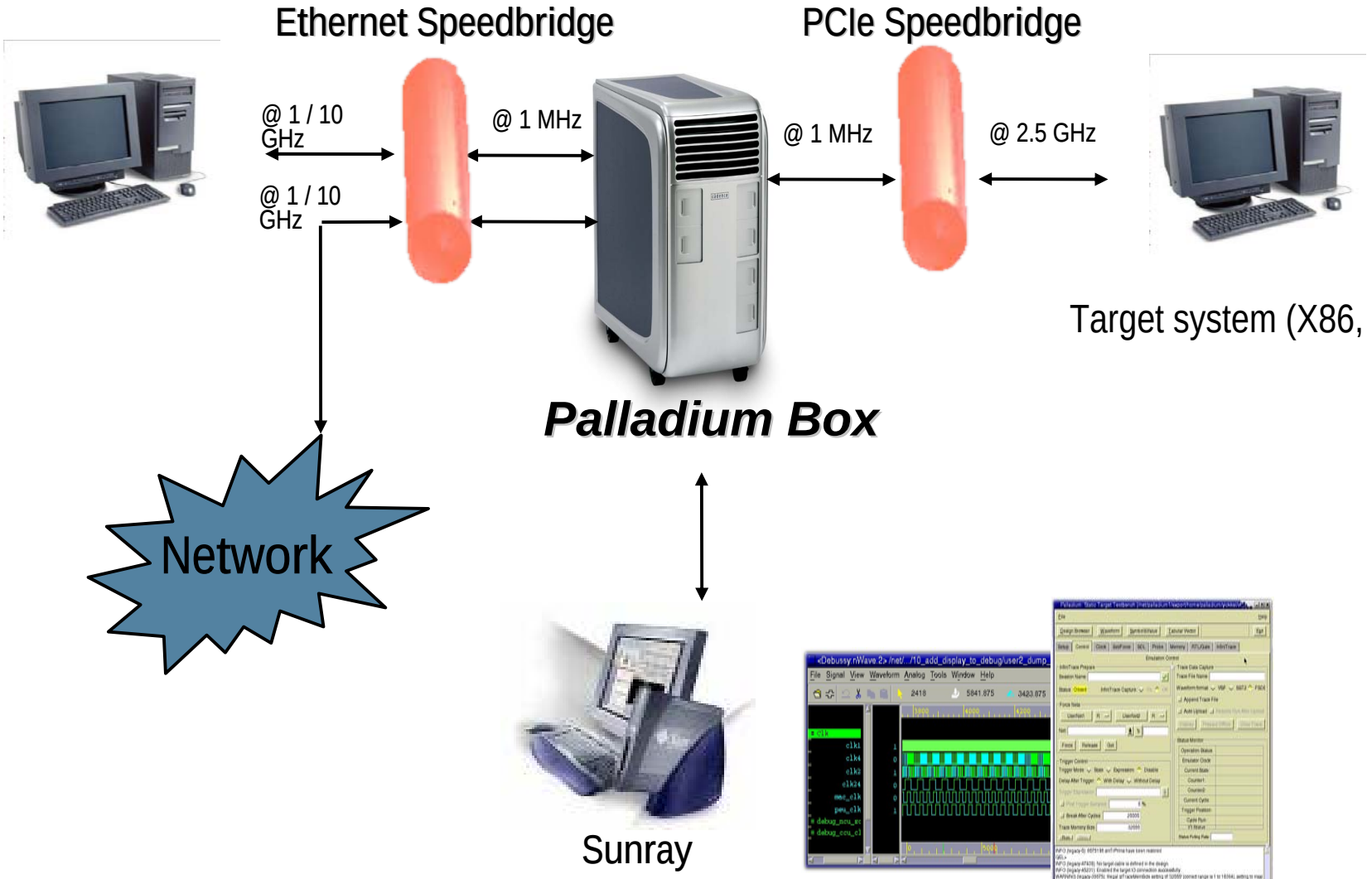
Accelerator/ Emulator- Palladium

Normalized speed:	1X	100X	10,000X	100,000X
			Ability to connect to a real target.	Ability to connect to a real target.

HW/SW Co-simulation Options

	Abstraction in C	FPGA Prototyping	HW Emulation
RTL Verification	No	Yes	Yes
Debugging features	Good	Limited	Good
Bringup effort	Days	Weeks	Days
Model turaround	Hours	Days	Hours
Timing concept	No	Yes	Yes
Modeling accuracy	Low	High	High
Runtime speed	High	High	Enough for SW verif
Capacity	Unlimited	Low	High
Real target system	No	Yes	Yes

Neptune In-circuit Emulation Setup



Classes of bugs found

- RTL bugs
  - Functional Verification had coverage holes
    - Vendor-defined type1 messages was wrongly decoded as configuration read packets.
    - PCIe bus device supported only 4 functions. BIOS trying to read all 8 functions in the emulation environment led to a hang.
  - Timing critical corner cases
    - After receiving thousands of vendor-specific message packets, PCIe device stopped updating the credits which led to a hang.
- Software bugs
  - 32-bit PCIe host, 64-bit device driver. Breaking 64-bit transactions incorrectly.
  - Initialization squence issues and Endianness issues.

System-level debugging

- Complicated bugs: Escaped from functional verification.
- Accurate emulation of final application is the key.
- Effective debug tools to root cause the issue.
- Our approach:
  - Print statements/$display messages from SW / RTL in real-time.
  - PCIE Monitors
  - Logic analyser for firmware debug.
  - Localize the issue and dump waveforms.
- Need experts from SW, Firmware and RTL team to come together.
- Debugging at System level is a time-consuming process.

Advantages of our solution

- System Development
  - Early System Integration
  - System bug finding
- ASIC HW Development
  - RTL Release Regressions
  - RTL bug finding
  - Ability to run compliance tests.
- Software Development
  - Firmware Development
  - SW bug finding.
- Simulation Acceleration.
- Easy debugging with waveforms and $display.
- Fast and inexpensive turnaround.
- Aid Silicon bring-up team.

Summary

- Neptune was a complex chip with tight development schedule
- Only emulation can give you the confidence that complete system (HW/SW) will start working at power on.
- Emulation cost and effort do pay-off!

Neptune was sending and receiving packets after 12 hours of power on!

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