

# Cadence Rapid Prototyping Platform

## FPGA-Based Prototyping Solution

Part of the Cadence® System Development Suite, the Cadence Rapid Prototyping Platform is an advanced FPGA-based prototyping solution for early software development and high-performance system validation. It combines high-capacity FPGA boards with a complete implementation and debug software flow, providing unprecedented design implementation speed and ease of use. Compatible with the Cadence Palladium® XP Verification Computing Platform and SpeedBridge® rate adapters, the Rapid Prototyping Platform allows for quick and smooth transition of an SoC design from an existing emulation environment into a high-performance rapid prototype.

### Early Software Development

Realizing today's SoCs—with their increasing software content—on-time and on-budget requires starting the software development process as early as possible. FPGA-based prototyping has long been a key technology to achieve just that. However, growing complexities and shrinking time-to-market windows are making the bring-up of such a prototyping system increasingly painful and time consuming.

The Cadence Rapid Prototyping Platform addresses these challenges. It provides a comprehensive and productive solution consisting of a family of FPGA boards and a fully integrated implementation and debug software flow, reducing prototype bring-up from months to weeks.

### Integrated Compile Engine

Taking an ASIC design (RTL) and mapping it into a set of FPGAs is the most challenging and time-consuming task when getting an FPGA-based prototype up and running. Unlike other solutions, the Rapid Prototyping Platform's Integrated Compile Engine provides everything needed to take an

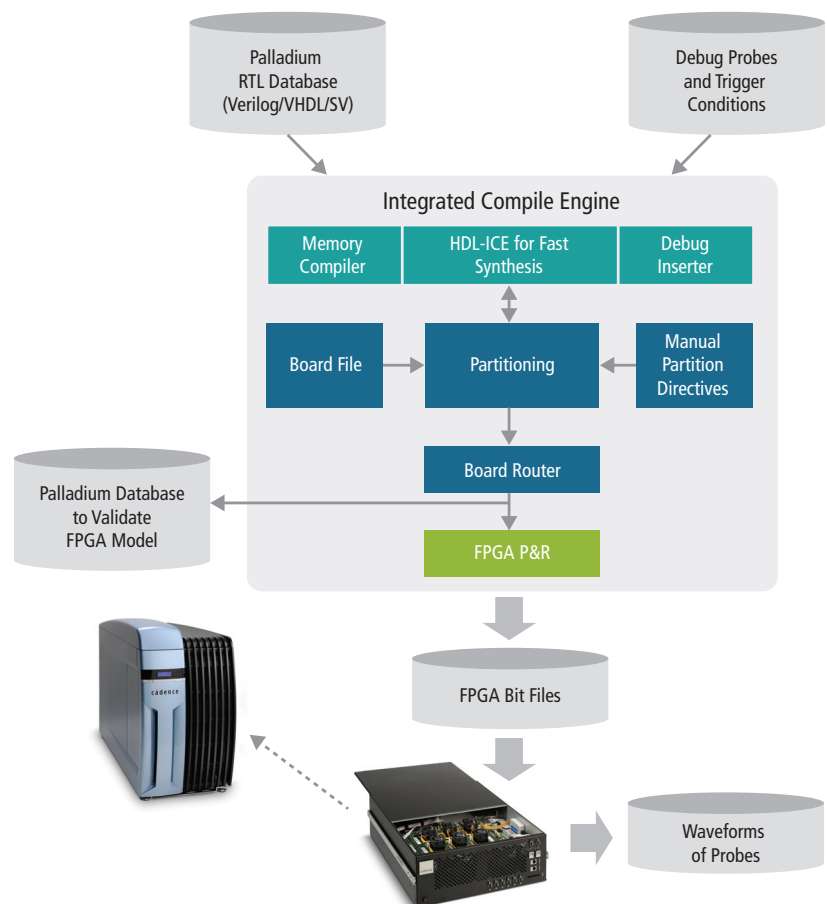


Figure 1: The Cadence Rapid Prototyping Platform delivers a comprehensive solution for early software development and high-performance system validation

existing RTL design, compile it, partition it into multiple FPGAs, and generate the individual bit files to configure each FPGA. This process can be fully automated or guided by the user at various levels of interaction—with minimal or no modifications to the original ASIC RTL code.

To gain visibility into the design during runtime, the user can select to-be-observed signals before compilation and define the trigger conditions to start a data capture. During runtime, the selected signals are captured and stored for offline viewing and analysis.

## Multiple Hardware Configurations

To cover a wide range of design sizes and different interface requirements, the Rapid Prototyping Platform offers multiple hardware configurations, ranging from 2–6 FPGAs per board. All FPGAs are Altera Stratix-4 8SE820-3 devices, providing up to 5M ASIC gates capacity (design dependent) and 33,294 Kbits of embedded memory per FPGA. The boards are mounted in a custom chassis with power supply, cooling, and all necessary interfaces and cabling included.

In addition to being equipped with a variety of on-board interfaces, Rapid Prototyping Platform systems are also fully compatible with the Cadence family of SpeedBridge interfaces, enabling a smooth transition from an emulation environment to a rapid prototyping environment.

## Benefits

### Fastest Prototype Bring-Up

- Reuse of the existing Palladium emulation environment
- Automatic multi-FPGA partitioning
- Automatic memory conversion and modeling

### Highest Model Accuracy

- Support for complex, ASIC-style clocking
- Palladium-compatible clocking definitions

- Automatic generation of a post-partitioning Palladium database for fast model validation

### Superior Debug

- Waveform capture and storage for offline debug and analysis
- Palladium compatibility for interactive debug and root cause analysis

### Unsurpassed Flexibility

- Most common interfaces standard on-board
- Expansion connectors for custom and off-the-shelf daughter cards
- Compatible with SpeedBridge emulation adapters

## Features

The Rapid Prototyping Platform is a complete, FPGA-based rapid prototyping system with all required hardware and software components:

### Design Input

- Synthesizable RTL (Verilog®, VHDL, SystemVerilog)
- Synthesizable gate-level netlist
- Full support and compatibility with the Palladium language set (synthesizable constructs only)

### Scripting and Set-Up

- Compatibility with Palladium script files
- Compatibility with Palladium clock definition files
- Automatic ASIC-to-FPGA memory conversion

### Probing and Debug

- User-defined probes at RTL
- Complex trigger definition in Verilog syntax
- VCD waveform file generation during runtime
- On-board MICTOR connectors for direct logic analyzer connection

## Multi-FPGA Partitioning

- Fully automatic with FPGA interconnect optimization and FPGA utilization balancing
- Optional user guidance through constraint file
- Automatic gated and generated clock conversion
- Automatic pin multi-plexing insertion
- Automatic board routing with trace delay optimization

## Post-Partitioning Palladium Model

- Generated automatically
- Fast FPGA model validation
- Accurate representation of the multi-FPGA implementation including clock re-mapping, memory conversion, pin multi-plexing, probing and triggering logic, etc.

## FPGA Place-and-Route

- Fully automatic set-up
- Support for parallel place-and-route
- Physical re-synthesis for implementation optimization
- Automatic timing closure, eliminating any set-up and hold time violations

## Requirements

### For Compile

- Linux workstation
- 64-bit Red Hat Enterprise or SUSE Enterprise
- 32GB of RAM

### For Control and Configuration

- Linux workstation (32-bit or 64-bit; Red Hat or SUSE)

### Or

- Windows PC (XP, Vista, Windows 7; 32-bit or 64-bit)
- 2GB of RAM
- 2 available USB 2.0 ports per Rapid Prototyping Platform system

- Multiple Rapid Prototyping Platform systems can be controlled from one workstation
- More than 25 Internet Learning Series (iLS) online courses allow you the flexibility of training at your own computer via the Internet

### Cadence Services and Support

- Cadence application engineers can answer your technical questions by telephone, email, or Internet—they can also provide technical assistance and custom training
- Cadence Online Support gives you 24x7 online access to a knowledgebase of the latest solutions, technical documentation, software downloads, and more
- Cadence certified instructors teach more than 70 courses and bring their real-world experience into the classroom

Rapid Prototyping Platform - Hardware Configurations				
	39RS401	39RS411	39RS412	39RS413
FPGAs	2 Stratix-4 EP4SE820-3	2 Stratix-4 EP4SE820-3	4 Stratix-4 EP4SE820-3	6 Stratix-4 EP4SE820-3
Approx. total capacity (design-dependent)	Up to 10M ASIC gates	Up to 10M ASIC gates	Up to 20M ASIC gates	Up to 30M ASIC gates
FPGA-internal memory	66,588 kbits	66,588 Kbits	133,176 Kbits	199,764 Kbits
On-board memory (optional)	Up to 8GB (2 DDR2 SODIMM)	Up to 8GB (2 DDR2 SODIMM)	Up to 8GB (2 DDR2 SODIMM)	Up to 16GB (4 DDR2 SODIMM)
On-board PCIe	N/A	8-lane gen-1 4-lane gen-2	8-lane gen-1 4-lane gen-2	8-lane gen-1 4-lane gen-2
On-board Ethernet	N/A	1 RJ45 socket 10/100/1000 Ethernet	1 RJ45 socket 10/100/1000 Ethernet	2 RJ45 sockets 10/100/1000 Ethernet
On-board serial interfaces	JTAG, RS232	JTAG, RS232	JTAG, RS232	JTAG, RS232
Clock generators	3 programmable synthesizers (20kHz – 600MHz)	3 programmable synthesizers (20kHz – 600MHz)	3 programmable synthesizers (20kHz – 600MHz)	3 programmable synthesizers (20kHz – 600MHz)
Low-skew, global clocks	16	16	16	16
Mictor connectors	N/A	N/A	1	2
Expansion connectors	6	1	2	3
User I/Os	1,110	190	380	570
Board configuration	CF card, JTAG, USB	CF card, JTAG, USB, PCIe	CF card, JTAG, USB, PCIe	CF card, JTAG, USB, PCIe
Dimensions	17.45" x 6.9" x 20.2" / 443mm x 175mm x 513mm (width x height x depth); rack mountable, 4U height			



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