Integrating Design IP and Verification IP

– To Ensure Quality and Predictability

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Agenda

- IP Challenges
- Rambus Design IP
- Verification IPs
  - Cadence VIP solution
  - Rambus VIP
- Cadence-Rambus collaboration
- Interoperability
- Summary

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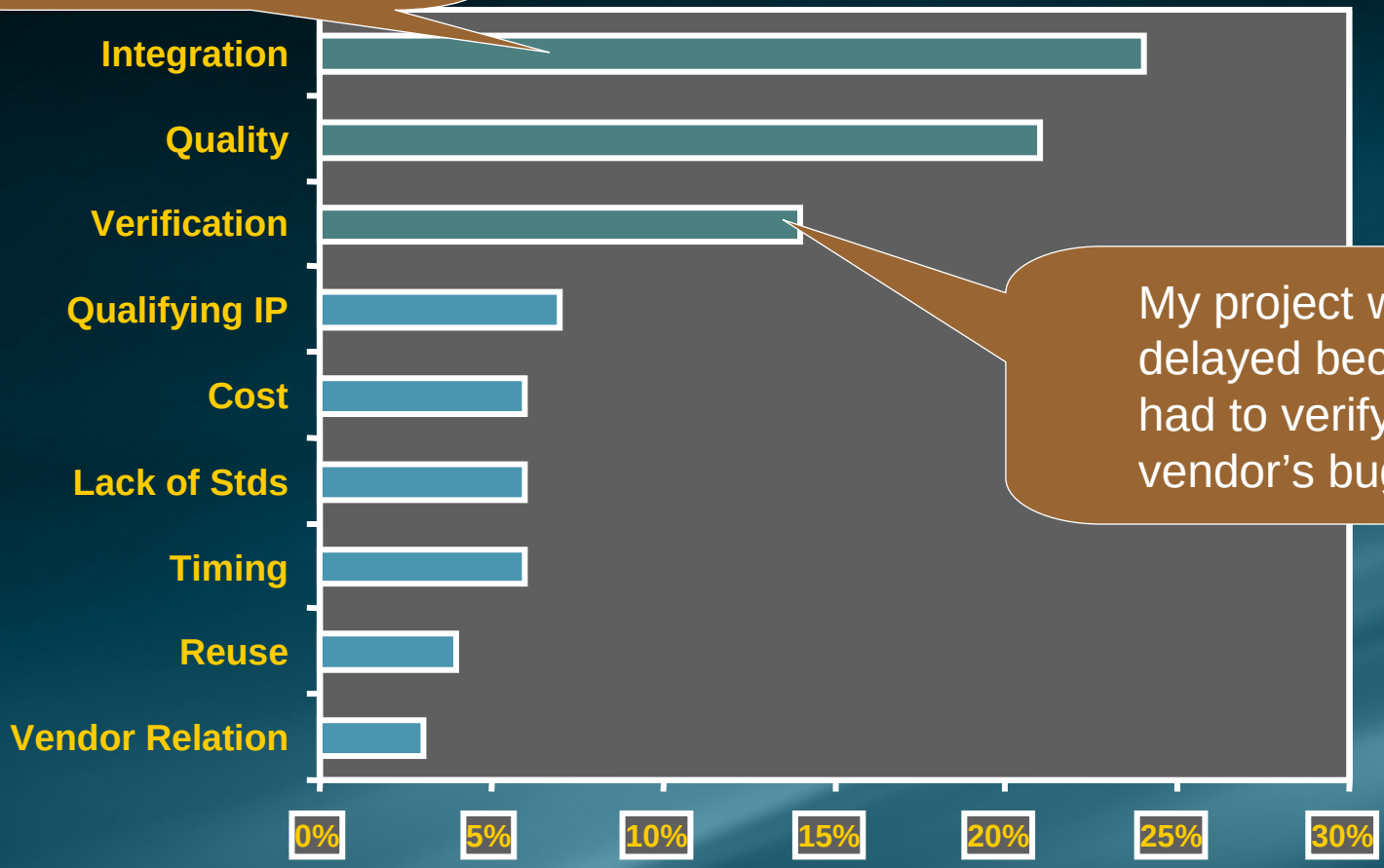
IP Challenges

"I had to spend time integrating the IP into SoC"



My project was delayed because I had to verify the vendor's bug fix"

Source: Gartner, DAC - 2006

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Challenges for IP providers

- Too much Variability → configuration explosion
  - Application: SOCs, bridges, switches, mobile, server..
  - Interfaces: proprietary, VCI, AHB, OCP-IP..
  - # of configurations >> 100
- Lack of standards in EDA space
  - Languages: Verilog, VHDL, SystemVerilog, e
  - Tools: Simulators, HVL engines, formal engines
  - Methodology: Cadence, Synopsys, Mentor
- Multiple vendors for Design and VIP

Challenges for IP consumer

- Correctness of integration
- Correctness of any changes to IP
- Correctness of selected configuration to meet the system goals performance, power..
- Verification after implementation stages
- System level aspects: reset, clock, intr, software access
- Verification of coverage: code, functional..
- Verification of rest of the design through the IP

Is the IP verification environment reusable for the above chip verification tasks?

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Rambus - Configurable IP Technology

- Easy IP configuration and integration
- Flexible verification env for all IP configs
- IP fully validated for all the configs
- Quality metrics for all the design modes
- Design aware customization service availability

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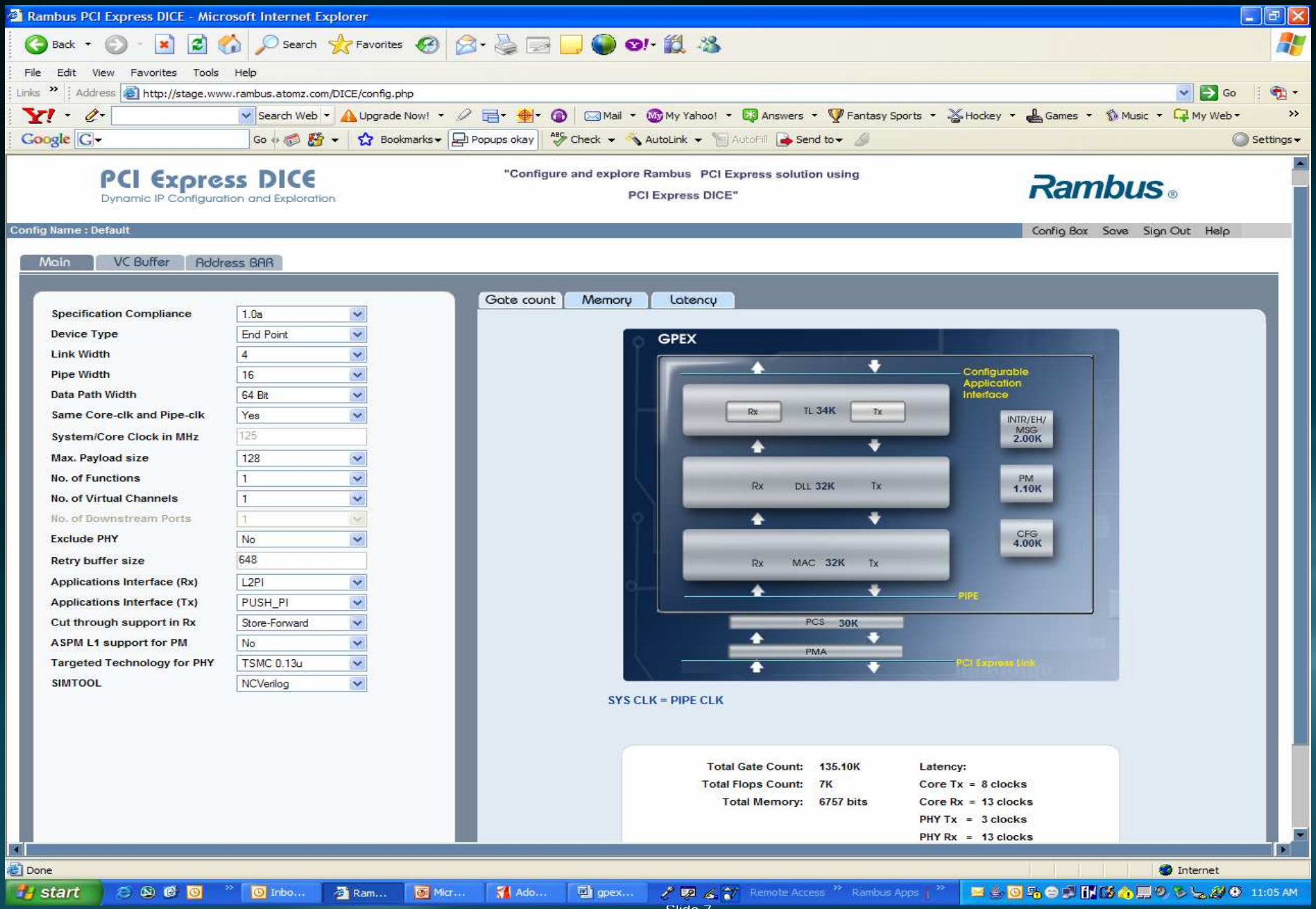
DICE


Rambus PCI Express DICE - Microsoft Internet Explorer
http://stage.www.rambus.atomz.com/DICE/config.php
PCI Express DICE
Dynamic IP Configuration and Exploration
"Configure and explore Rambus PCI Express solution using PCI Express DICE"
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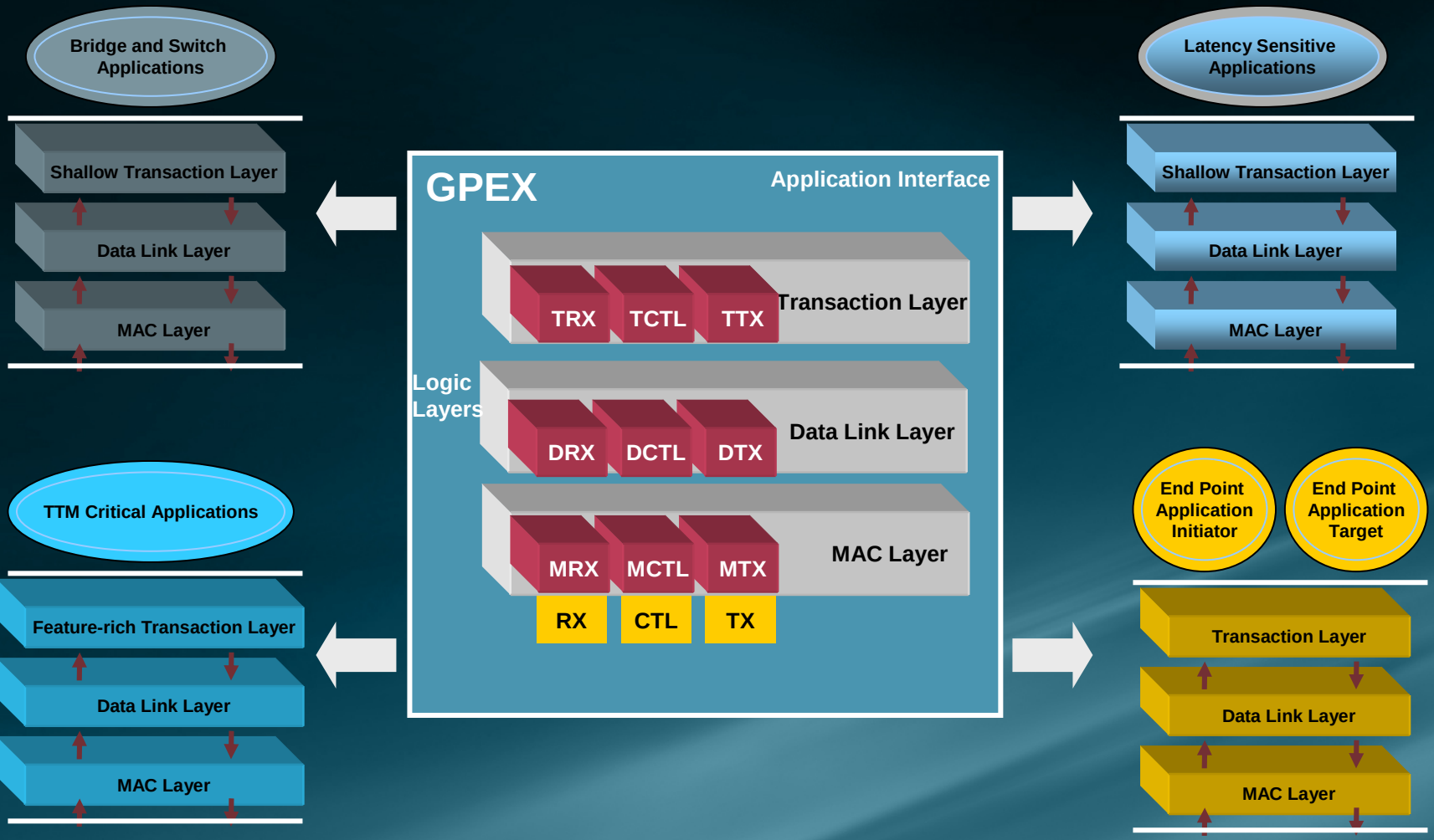
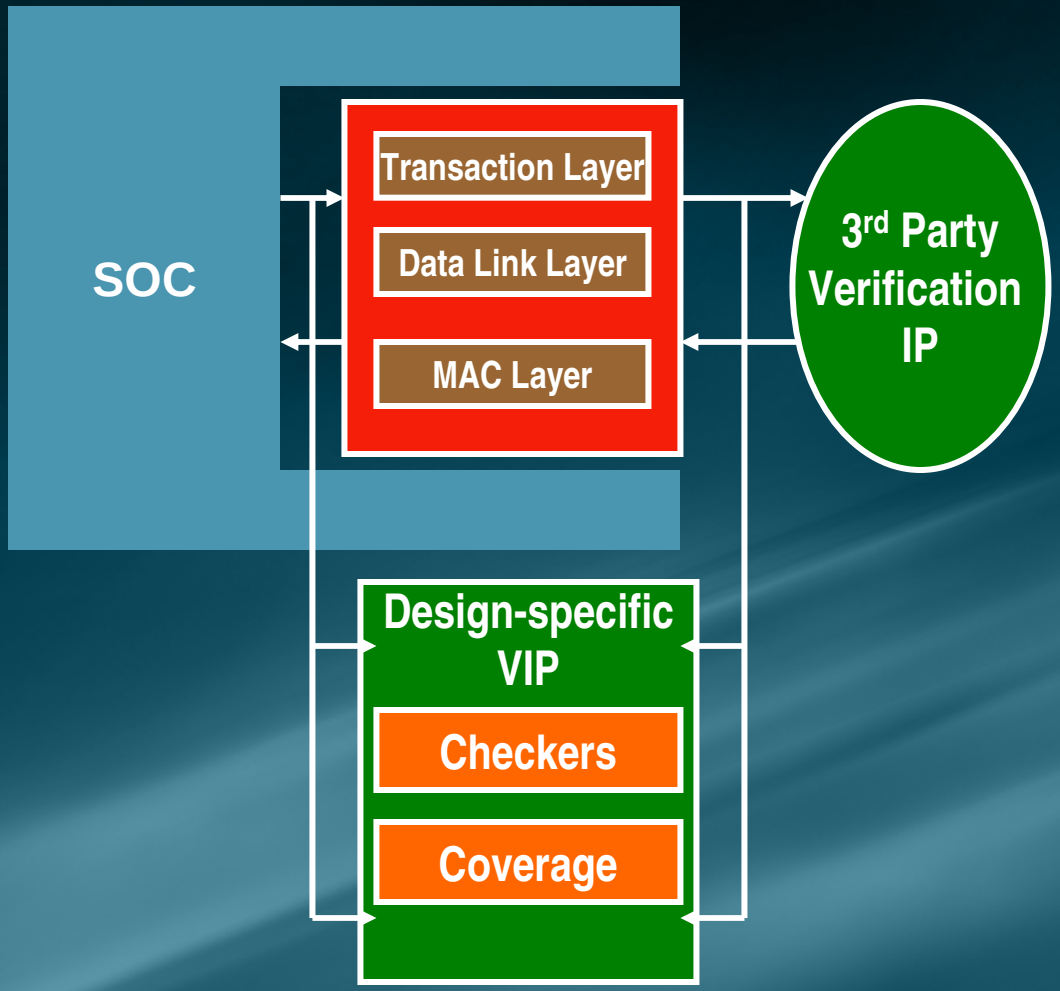
Config Name : Default
Config Box Save Sign Out Help
Main VC Buffer Address BAR
Specification Compliance 1.0a
Device Type End Point
Link Width 4
Pipe Width 16
Data Path Width 64 Bit
Same Core-clk and Pipe-clk Yes
System/Core Clock in MHz 125
Max. Payload size 128
No. of Functions 1
No. of Virtual Channels 1
No. of Downstream Ports 1
Exclude PHY No
Retry buffer size 648
Applications Interface (Rx) L2PI
Applications Interface (Tx) PUSH_PI
Cut through support in Rx Store-Forward
ASPM L1 support for PM No
Targeted Technology for PHY TSMC 0.13u
SIMTOOL NCVerilog
Gate count Memory Latency
GPEX
Configurable Application Interface
Rx TL 34K Tx
INTR/EH/MSG 2.00K
Rx DLL 32K Tx
PM 1.10K
Rx MAC 32K Tx
CFG 4.00K
PIPE
PCS 30K
PMA
PCI Express Link
SYS CLK = PIPE CLK
Total Gate Count: 135.10K
Total Flops Count: 7K
Total Memory: 6757 bits
Latency:
Core Tx = 8 clocks
Core Rx = 13 clocks
PHY Tx = 3 clocks
PHY Rx = 13 clocks
Done
Internet
start
11:05 AM

Configurable Design IP Solutions



IP Verification requirement

- Environment needs to be configuration agnostic
- Consider both protocol features and design-specific implementation
- Must be re-usable in SoC environment



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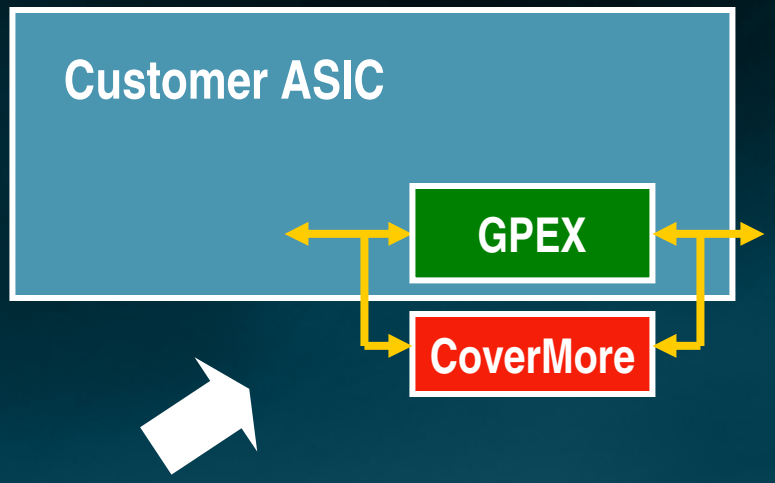
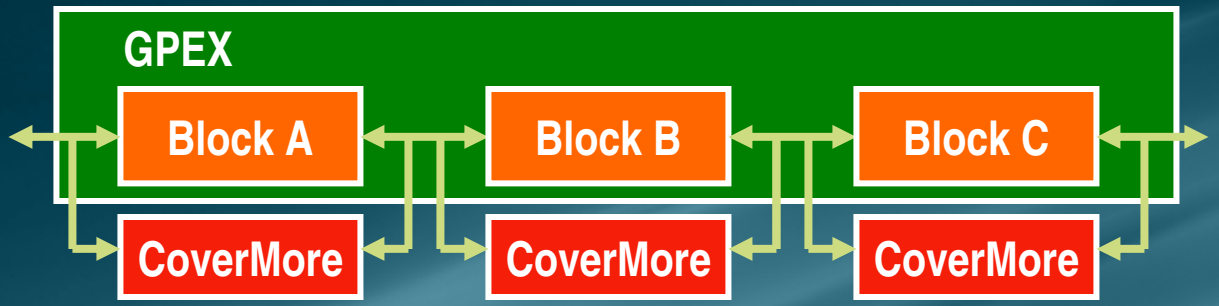
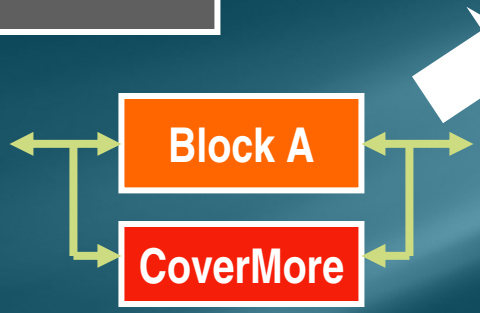
Rambus VIP - CoverMore

- CoverMore
  - Design-specific VIP
  - Highly modular approach
- Reusable across block, IP and chip level
- “Self-checking” Design IP



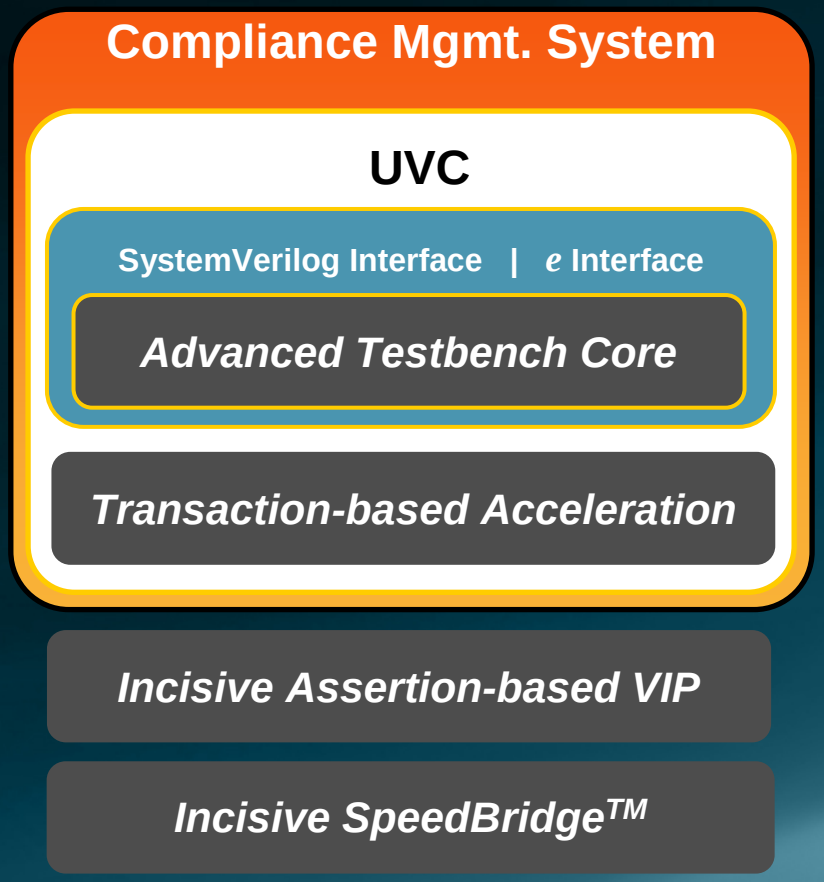


Coverage and verification based on Modular and reusable IPs



First CoverMore implementation based on Cadence Specman/e

Cadence VIP Strategy



- Provide *Plan-to-Closure* VIP spanning full verification process
- Support most complex, demanding protocols
- Unique Compliance Management System
- Enable customers & partners to deploy CDNS's VIP development *process*
- Provide tailored Verification IP for Cadence Vertical Kits

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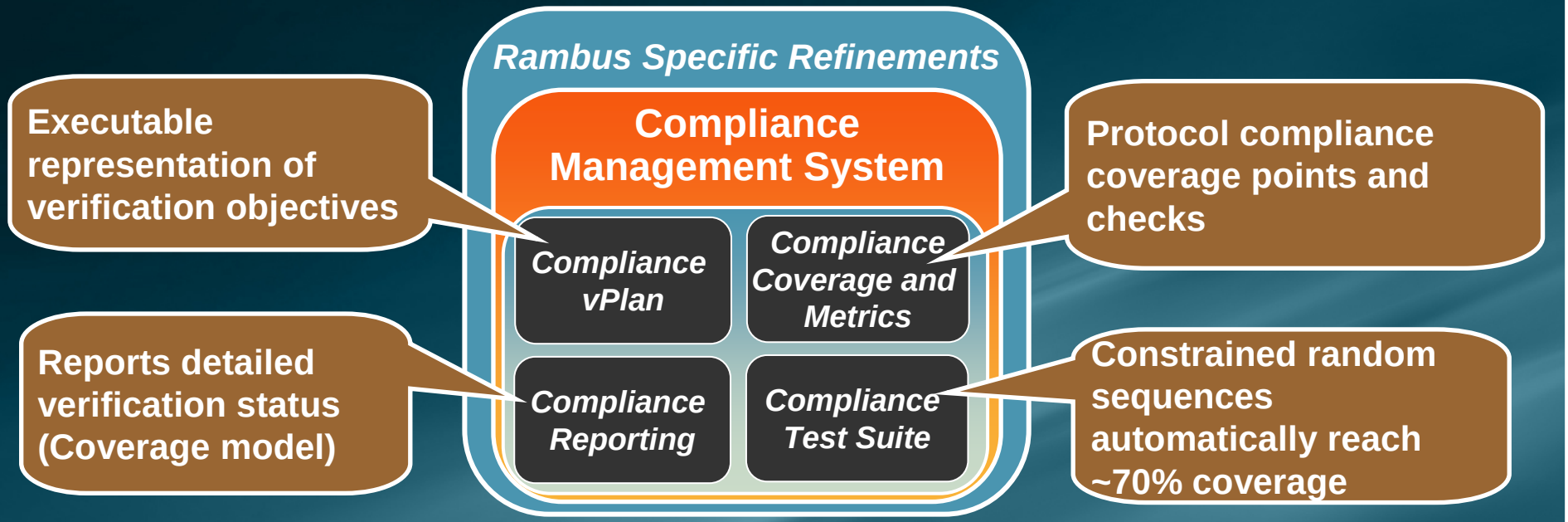
Compliance Management System (CMS)

Automates compliance verification and reporting

- Leverage Cadence uVC Functional Coverage
- Key differentiator
- Optimized for Rambus IP with Rambus refinements



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DIP-VIP Interoperability Challenges

- Ensuring the VIP and Design IP have the same configuration
  - In depth design knowledge availability
  - Verification IP expertise
- Achieving targeted coverage of Application Interface
- Debugging
  - Time consuming Root-cause analysis

Cadence-Rambus Collaboration

- **Fully Integrated and Independently verified PCIe solution**
- **Highly adaptable, silicon-proven PCIe digital core and Phy IP from Rambus**
- **Automated and metric-driven VIP from Cadence**
- **Leverages several years of expertise**

Combine configurable, proven design IP with best of class VIP

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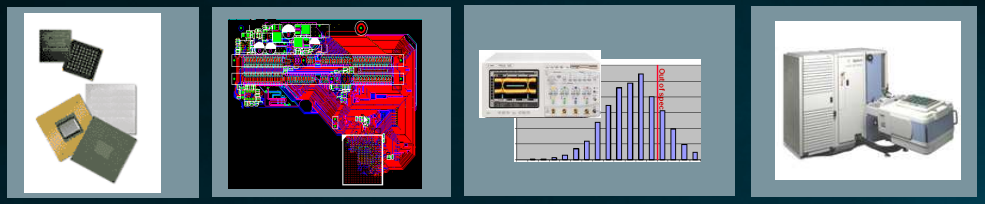
Combining Best of Breed Design and Verification IP



- Cadence & Rambus value proposition
  - Highest quality
  - Fastest time to revenue
  - Lowest risk

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Best of Breed PCI Express Solution

- Design IP and VIP independently cross checked
  - Cadence and Rambus models built independently

- Design IP and VIP most tightly integrated
  - Executable verification plan specific to your IP
  - Customized test suite specific to your IP
  - Automated protocol Compliance Management System

cadence™ + Rambus®

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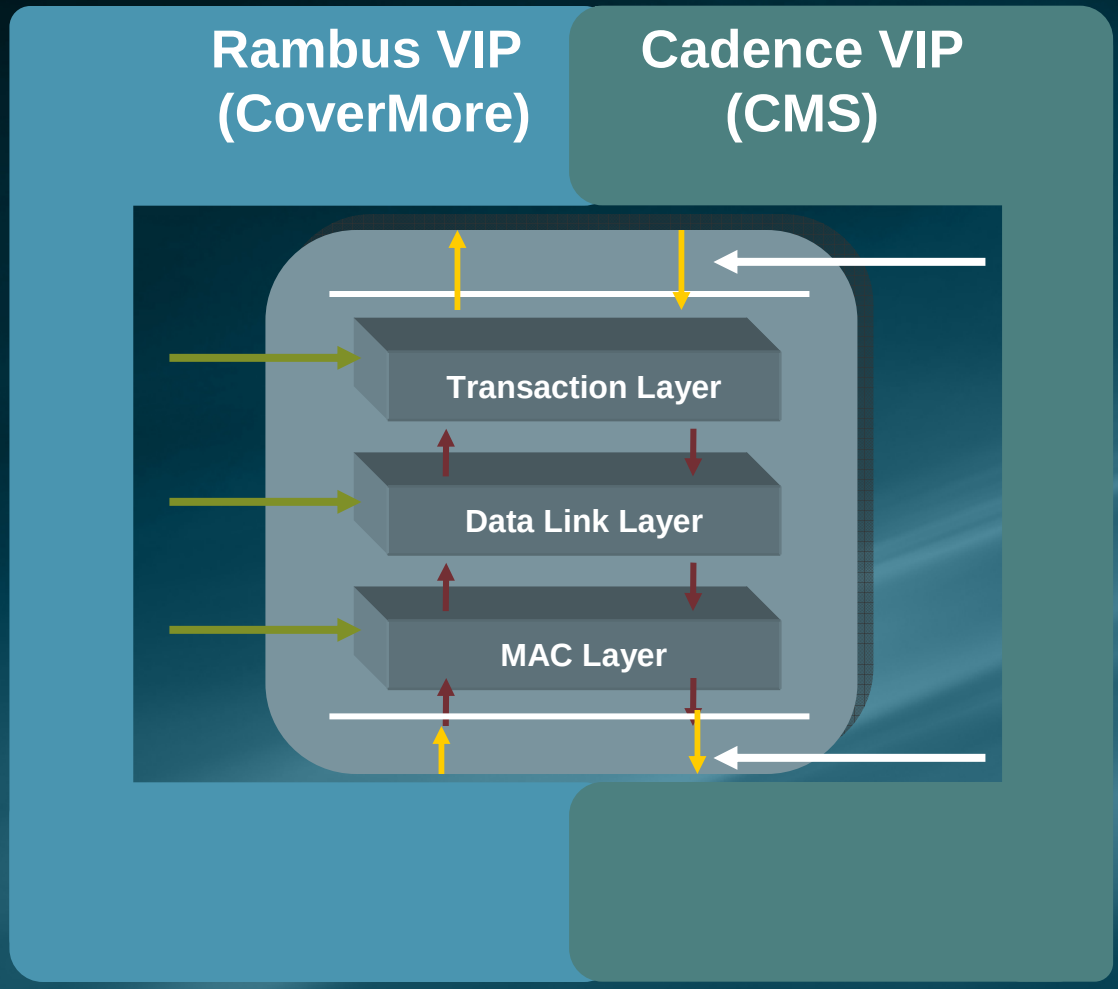
Integrated Environment

Targets Design IP-specific Functionality

Targets Design IP Protocol Compliance and Integration of Design IP and Customer Logic



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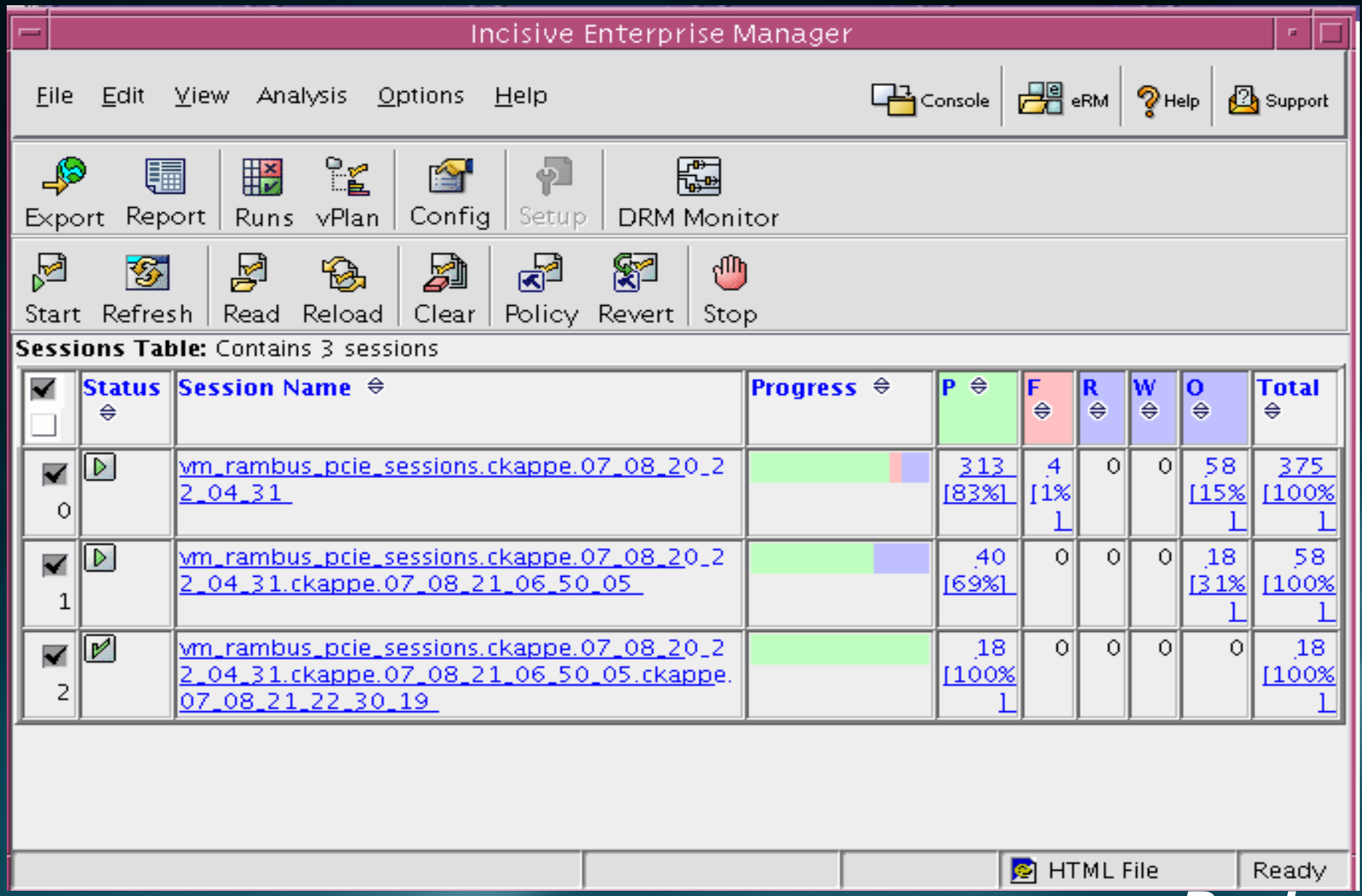
Methodology

- Re-create customer environment
- Maintain Verification independence
- Tool aspects
  - Follow release QA for eVC and Design IP
- Debugging
  - Run regressions at CDN and Rambus
    - Regressions include Cadence + Rambus tests
  - Root-cause analysis
    - VIP/tool anomaly fixes by CDN
    - Design IP anomaly fixes by Rambus

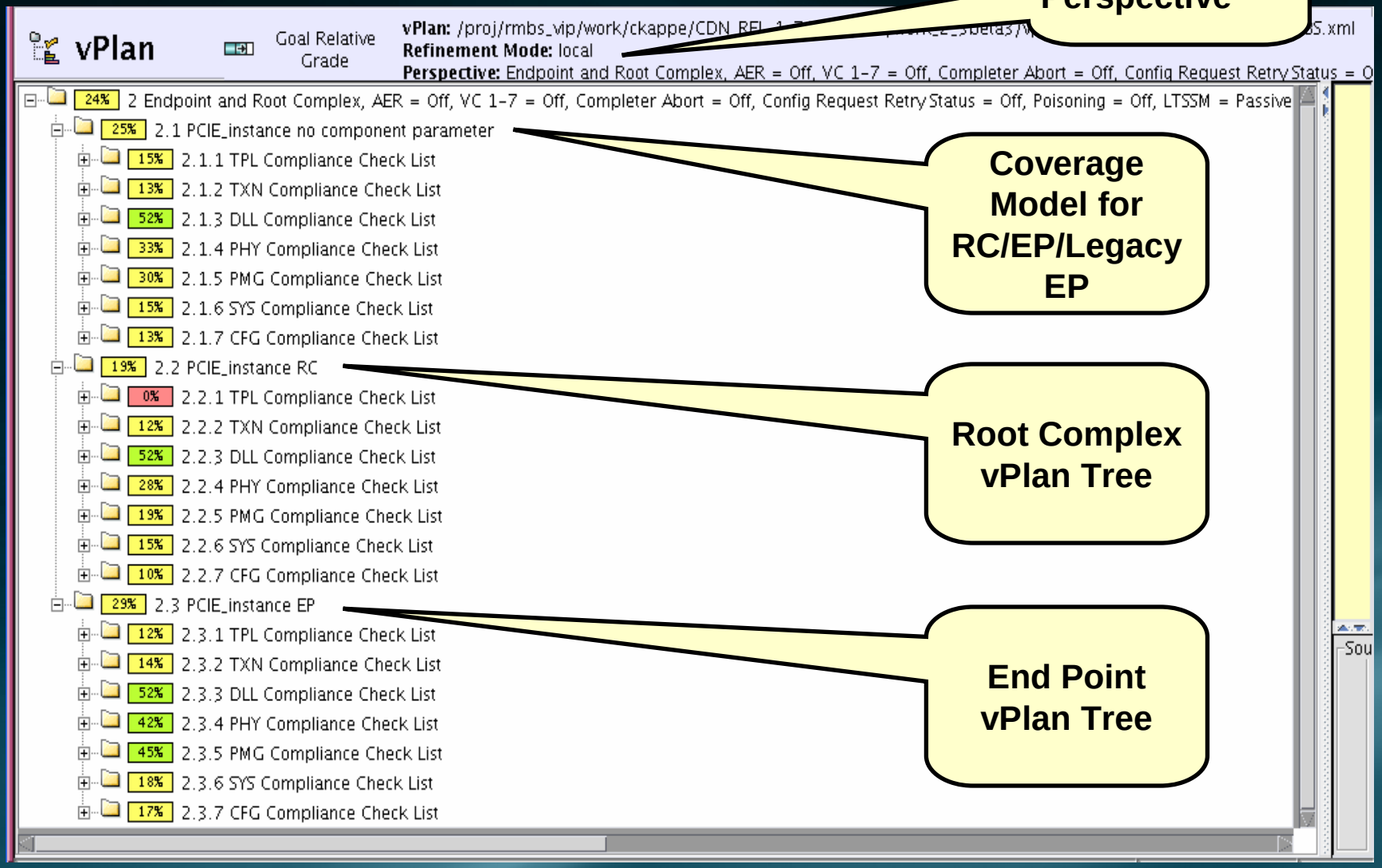
Refinement

- CDN PCIe compliance vPlan has all features of PCIe
- Example - DUT configuration specific features
  - DUT acts as End point
  - RC related coverage points are disabled
- Unsupported PCIe compliance points in the design
- Refined vPlan and created required perspective which will load on CDN compliance vPlan

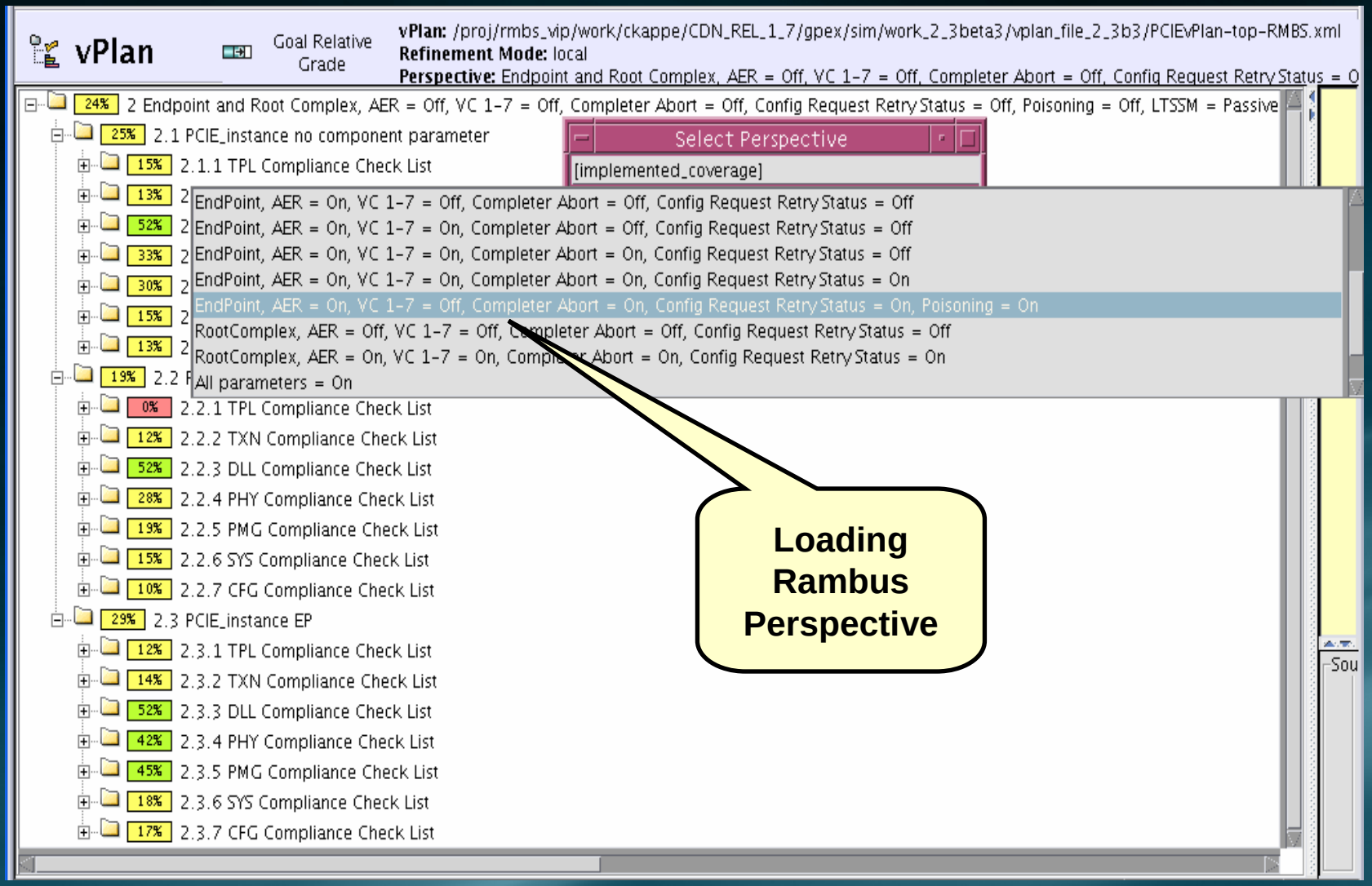
vManager Regression Session



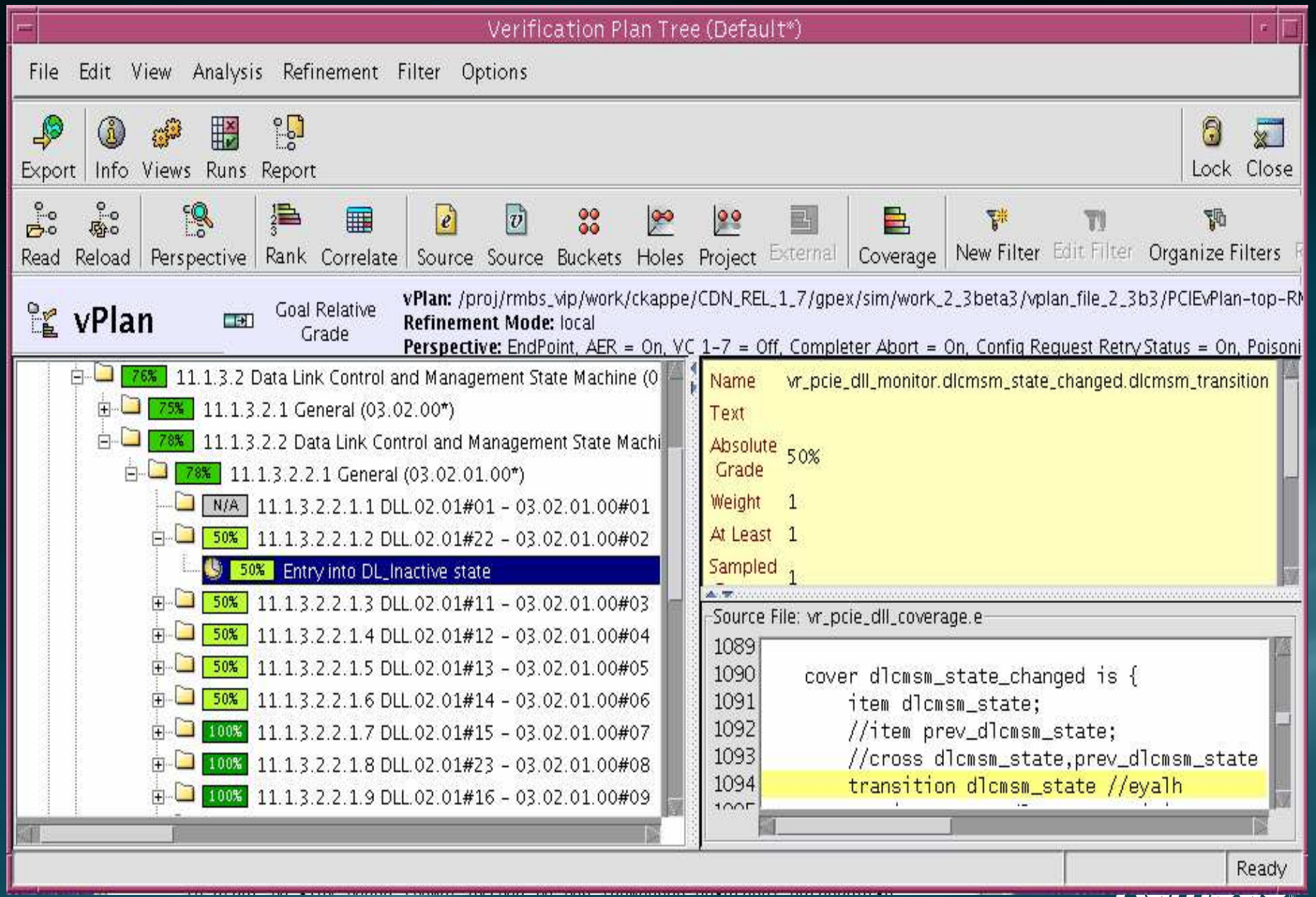
vPlan Default Perspective



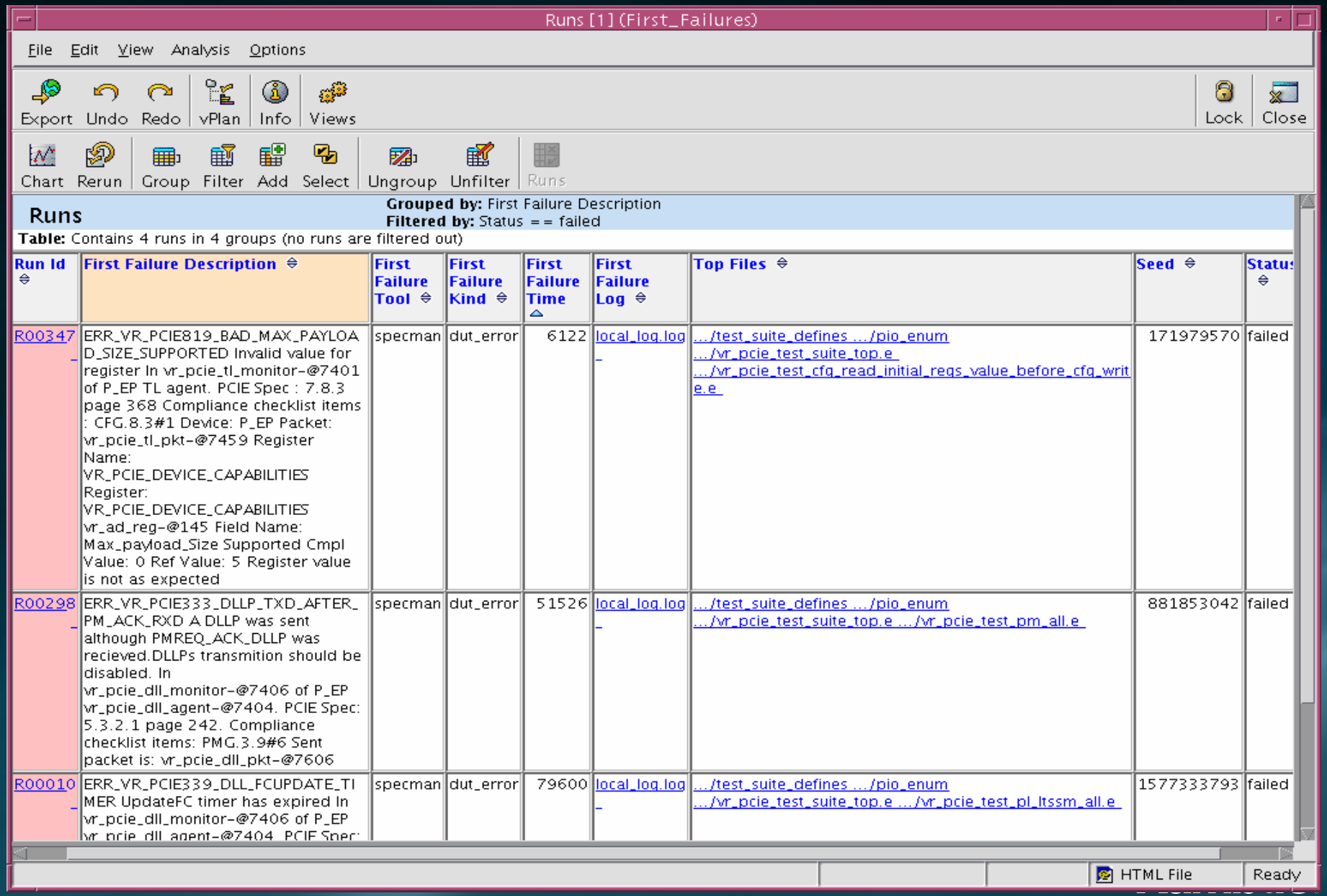
vPlan – Loading Rambus Perspective



vPlan Window – Selected Item

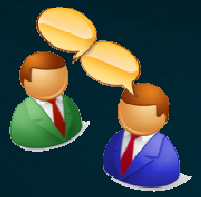


Failure Report - First Failure Description



Run Id	First Failure Description	First Failure Tool	First Failure Kind	First Failure Time	First Failure Log	Top Files	Seed	Status
R00347	ERR_VR_PCIE819_BAD_MAX_PAYLOAD_SIZE_SUPPORTED Invalid value for register In vr_pcie_tl_monitor-@7401 of P_EP TL agent. PCIE Spec : 7.8.3 page 368 Compliance checklist items : CFG.8.3#1 Device: P_EP Packet: vr_pcie_tl_pkt-@7459 Register Name: VR_PCIE_DEVICE_CAPABILITIES Register: VR_PCIE_DEVICE_CAPABILITIES vr_ad_reg-@145 Field Name: Max_payload_Size Supported Cmpl Value: 0 Ref Value: 5 Register value is not as expected	specman	dut_error	6122	local_log.log	.../test_suite_defines .../pio_enum .../vr_pcie_test_suite_top.e .../vr_pcie_test_cfg_read_initial_regs_value_before_cfg_write.e	171979570	failed
R00298	ERR_VR_PCIE333_DLLP_TXD_AFTER_PM_ACK_RXD A DLLP was sent although PMREQ_ACK_DLLP was recieved.DLLPs transmition should be disabled. In vr_pcie_dll_monitor-@7406 of P_EP vr_pcie_dll_agent-@7404. PCIE Spec: 5.3.2.1 page 242. Compliance checklist items: PMG.3.9#6 Sent packet is: vr_pcie_dll_pkt-@7606	specman	dut_error	51526	local_log.log	.../test_suite_defines .../pio_enum .../vr_pcie_test_suite_top.e .../vr_pcie_test_pm_all.e	881853042	failed
R00010	ERR_VR_PCIE339_DLL_FCUPDATE_TIMER UpdateFC timer has expired In vr_pcie_dll_monitor-@7406 of P_EP vr_pcie_dll_agent-@7404. PCIE Spec:	specman	dut_error	79600	local_log.log	.../test_suite_defines .../pio_enum .../vr_pcie_test_suite_top.e .../vr_pcie_test_pl_ltssm_all.e	1577333793	failed

Interoperability Efforts



Strategy Managers

TL Engineer

Team Lead

Project Manager

Tool R&D Engineer

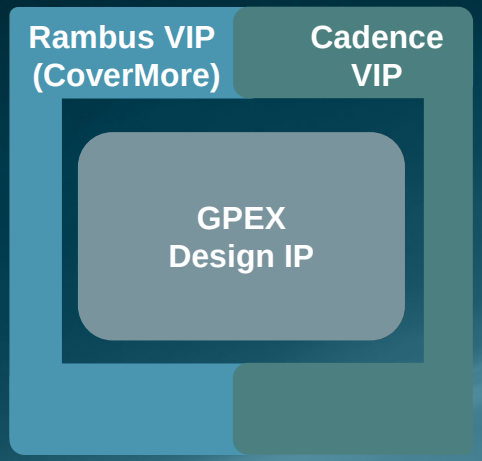
DLL Engineer

Verification Engineer

Verification Engineer

Tool R&D Engineer

MAC Engineer



Huge efforts spent to help the customer integrate IP smoothly

Interoperability Efforts

- Several man-years worth of efforts
  - Design IP Development
  - VIP Development
  - Interoperability efforts
- Tool Licenses
- Methodologies
- Customer approval

Rambus and Cadence Collaboration Deliverables

- Design IP
  - PCI Express Digital controller, PHY
- Verification IPs
  - CoverMore VIP
  - Cadence eVC VIP
    - ✓ PCI Express eVC
    - ✓ Supports *e* and/or SystemVerilog test benches
    - ✓ PCI Express Compliance Management System
      - ✓ Executable verification plan (vPlan)
      - ✓ Test suite to achieve 70% + coverage
    - ✓ Rambus specific package for Verification
      - ✓ Refinement file for PCI Express vPlan
      - ✓ Additional test sequences to maximize coverage

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Summary

Rambus + Cadence collaboration solves IP Integration challenges

- Independently verified
  - Independently created models
  - Independently cross–checked
- Tightest integration of Design IP and VIP
- Combined expertise of Rambus and Cadence
- Most automated solution
  - Cadence CMS automates verification
  - Digital core customizable protocol support

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Thanks!

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