



Integrating Design IP and Verification IP

– To Ensure Quality and Predictability

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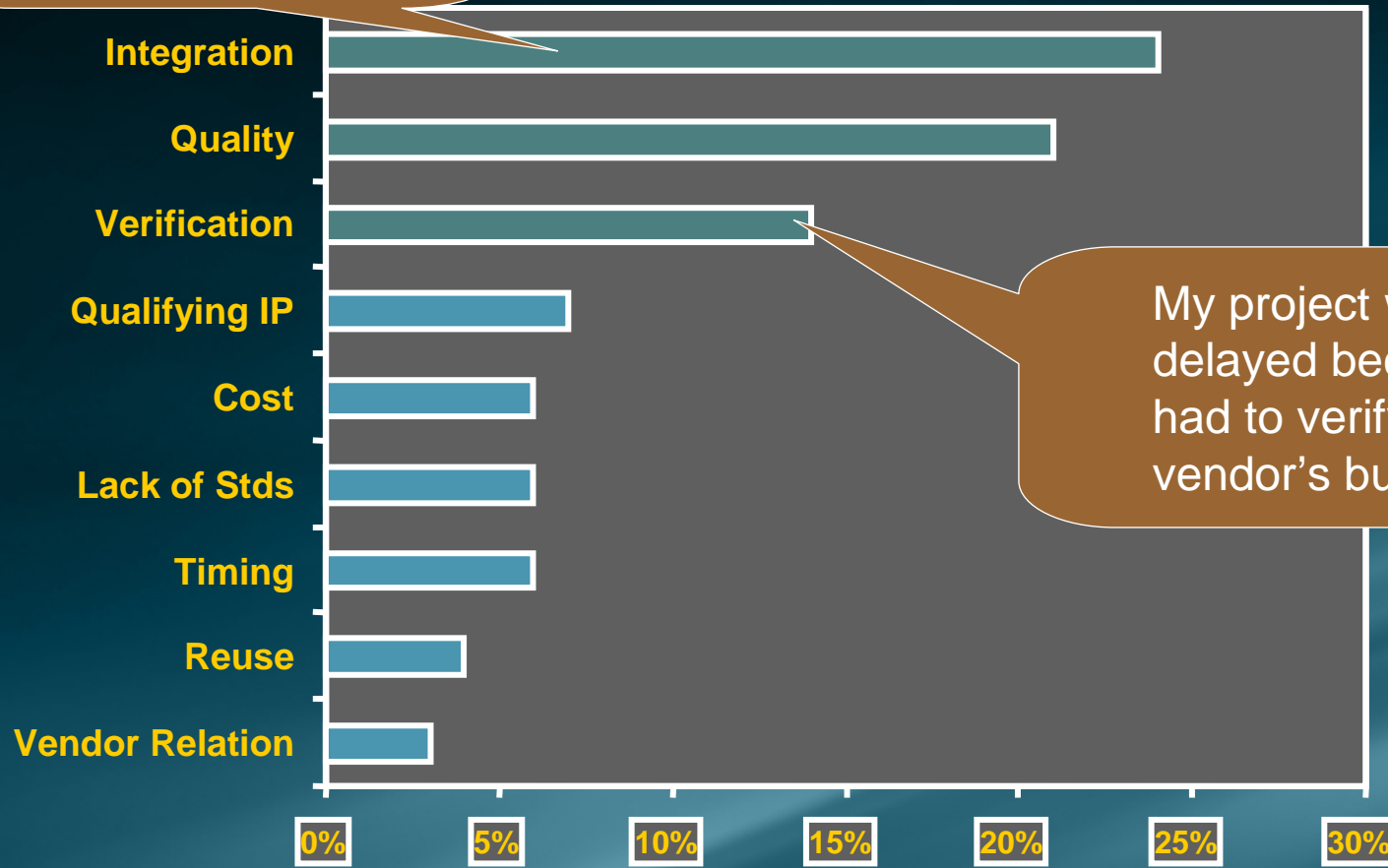
Rambus[®]

Agenda

- IP Challenges
- Rambus Design IP
- Verification IPs
 - Cadence VIP solution
 - Rambus VIP
- Cadence-Rambus collaboration
- Interoperability
- Summary

IP Challenges

“I had to spend time integrating the IP into SoC”



My project was delayed because I had to verify the vendor's bug fix”

Source: Gartner, DAC - 2006

Challenges for IP providers

- **Too much Variability → configuration explosion**
 - Application: SOCs, bridges, switches, mobile, server..
 - Interfaces: proprietary, VCI, AHB, OCP-IP..
 - # of configurations >> 100
- **Lack of standards in EDA space**
 - Languages: Verilog, VHDL, SystemVerilog, e
 - Tools: Simulators, HVL engines, formal engines
 - Methodology: Cadence, Synopsys, Mentor
- **Multiple vendors for Design and VIP**

Challenges for IP consumer

- Correctness of integration
- Correctness of any changes to IP
- Correctness of selected configuration to meet the system goals performance, power..
- Verification after implementation stages
- System level aspects: reset, clock, intr, software access
- Verification of coverage: code, functional..
- Verification of rest of the design through the IP

Is the IP verification environment reusable for the above chip verification tasks?

Rambus - Configurable IP Technology

- Easy IP configuration and integration
- Flexible verification env for all IP configs
- IP fully validated for all the configs
- Quality metrics for all the design modes
- Design aware customization service availability

DICE

Rambus PCI Express DICE - Microsoft Internet Explorer

Back Forward Stop Home Search Favorites Refresh Print Mail My Yahoo! Answers Fantasy Sports Hockey Games Music My Web

Address: http://stage.www.rambus.atomz.com/DICE/config.php

Go Search Web Upgrade Now! Mail My Yahoo! Answers Fantasy Sports Hockey Games Music My Web

Google Go Bookmarks Popups okay Check AutoLink AutoFill Send to Settings

PCI Express DICE

Dynamic IP Configuration and Exploration

"Configure and explore Rambus PCI Express solution using PCI Express DICE"



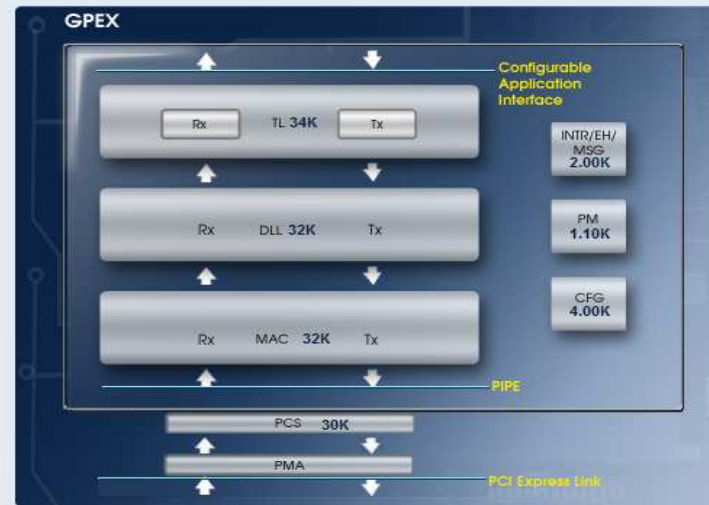
Config Name : Default

Config Box Save Sign Out Help

Main VC Buffer Address BAR

- Specification Compliance: 1.0a
- Device Type: End Point
- Link Width: 4
- Pipe Width: 16
- Data Path Width: 64 Bit
- Same Core-clk and Pipe-clk: Yes
- System/Core Clock in MHz: 125
- Max. Payload size: 128
- No. of Functions: 1
- No. of Virtual Channels: 1
- No. of Downstream Ports: 1
- Exclude PHY: No
- Retry buffer size: 648
- Applications Interface (Rx): L2PI
- Applications Interface (Tx): PUSH_PI
- Cut through support in Rx: Store-Forward
- ASPM L1 support for PM: No
- Targeted Technology for PHY: TSMC 0.13u
- SIMTOOL: NCVerilog

Gate count Memory Latency

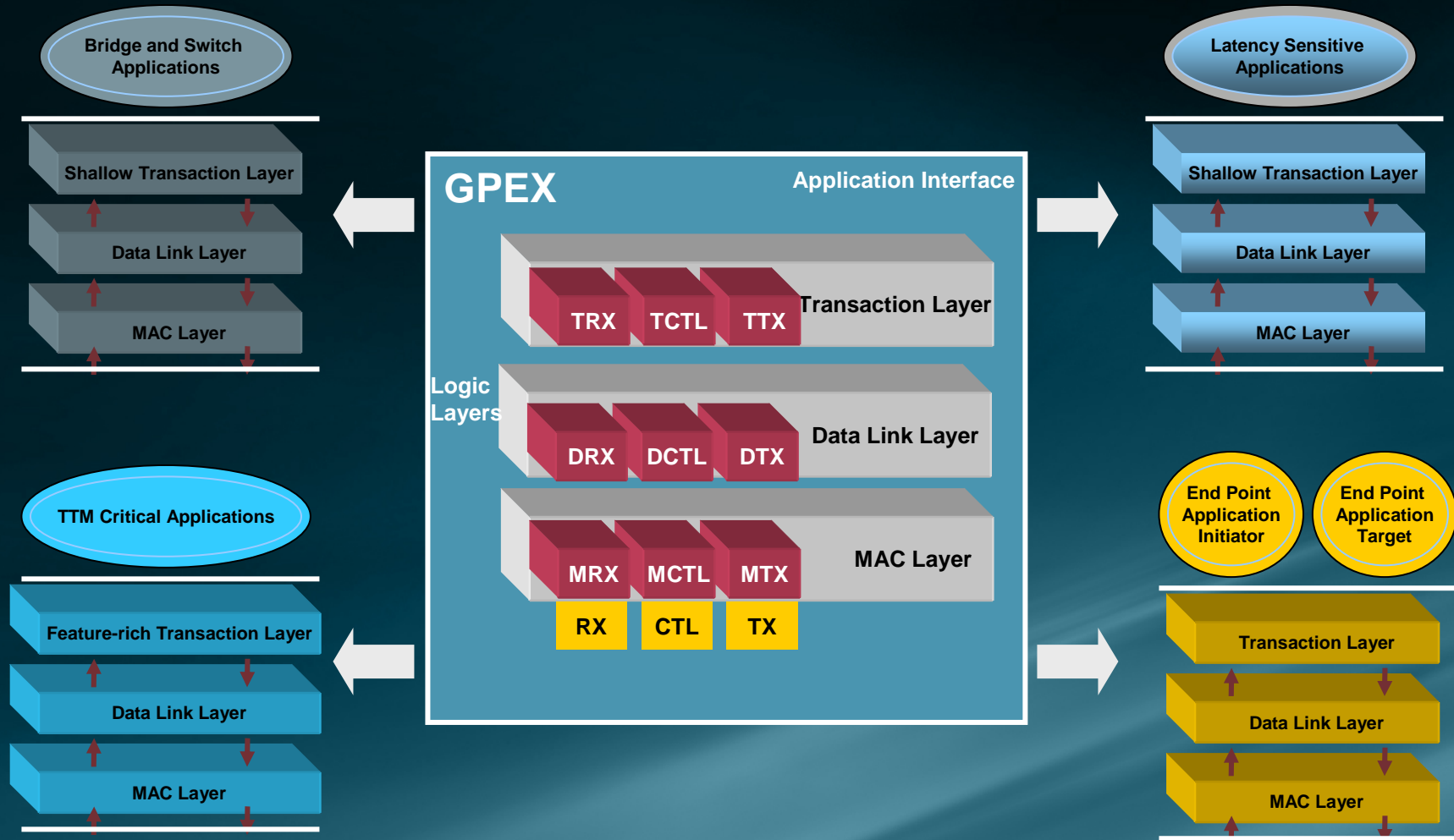


Total Gate Count:	135.10K	Latency:
Total Flops Count:	7K	Core Tx = 8 clocks
Total Memory:	6757 bits	Core Rx = 13 clocks
		PHY Tx = 3 clocks
		PHY Rx = 13 clocks

Done Internet

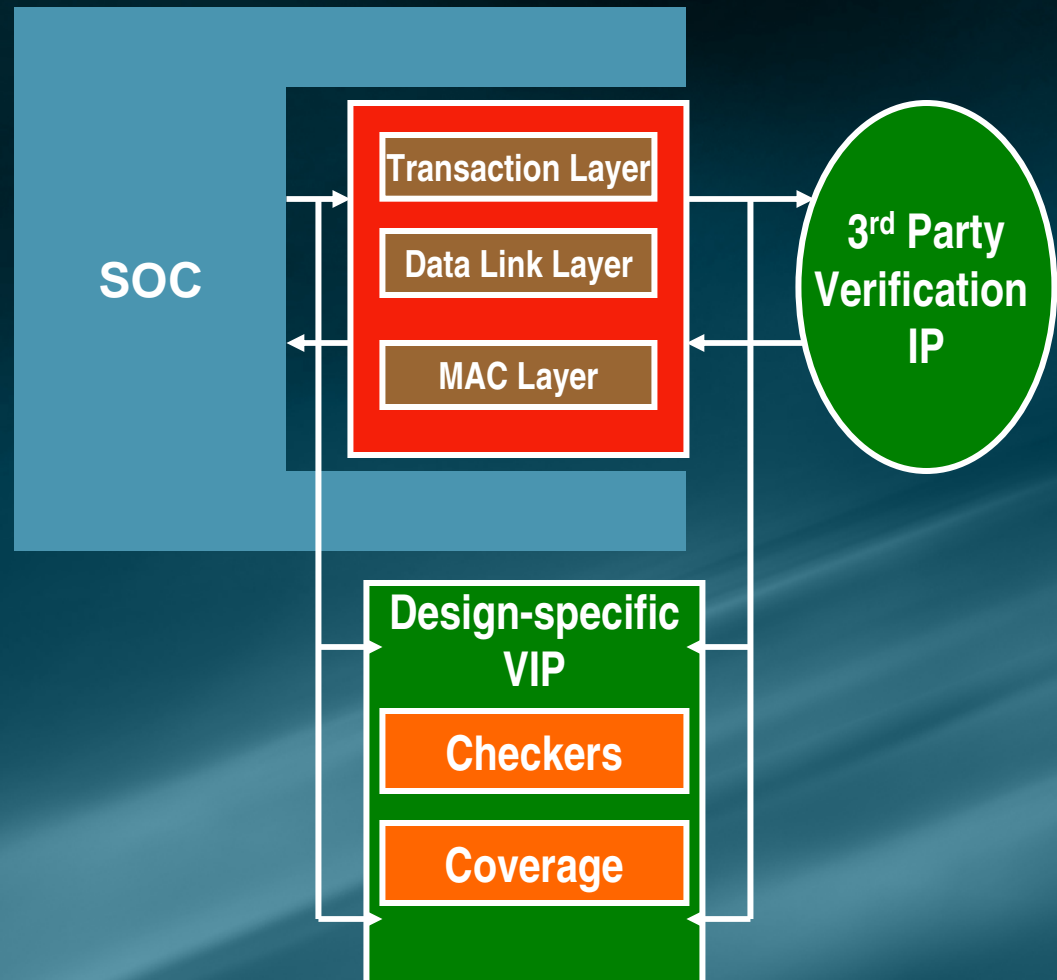
start Inbo... Ram... Micr... Ado... gpex... Remote Access Rambus Apps 11:05 AM

Configurable Design IP Solutions



IP Verification requirement

- Environment needs to be configuration agnostic
- Consider both protocol features and design-specific implementation
- Must be re-usable in SoC environment

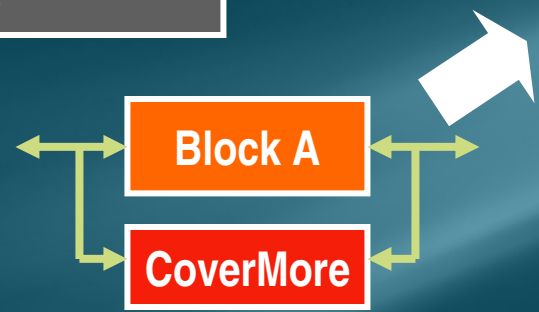
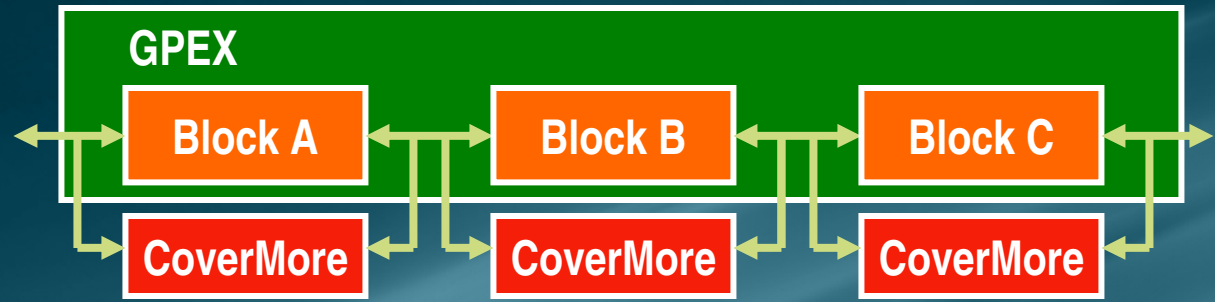


Rambus VIP - CoverMore

- CoverMore
 - Design-specific VIP
 - Highly modular approach
- Reusable across block, IP and chip level
- “Self-checking” Design IP



Coverage and verification based on Modular and reusable IPs



First CoverMore implementation based on Cadence Specman/e

Cadence VIP Strategy

Compliance Mgmt. System

UVC

SystemVerilog Interface | e Interface

Advanced Testbench Core

Transaction-based Acceleration

Incisive Assertion-based VIP

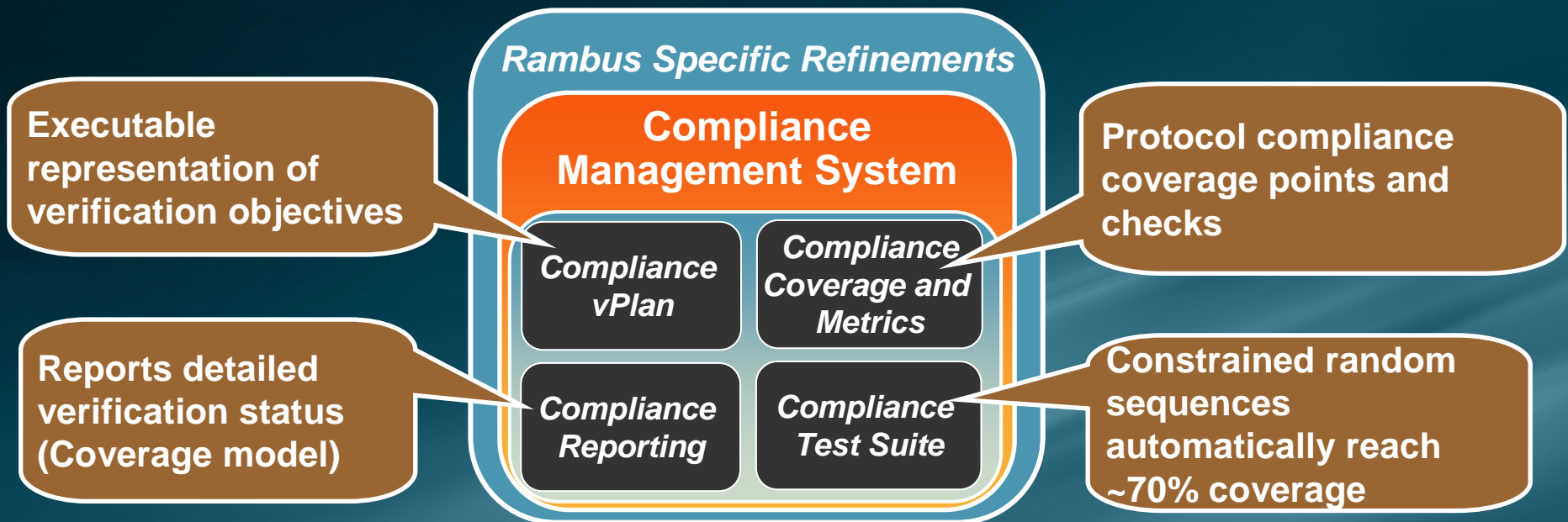
Incisive SpeedBridge™

- Provide *Plan-to-Closure* VIP spanning full verification process
- Support most complex, demanding protocols
- Unique Compliance Management System
- Enable customers & partners to deploy CDNS's VIP development process
- Provide tailored Verification IP for Cadence Vertical Kits

Compliance Management System (CMS)

Automates compliance verification and reporting

- Leverage Cadence uVC Functional Coverage
- Key differentiator
- Optimized for Rambus IP with Rambus refinements



DIP-VIP Interoperability Challenges

- Ensuring the VIP and Design IP have the same configuration
 - In depth design knowledge availability
 - Verification IP expertise
- Achieving targeted coverage of Application Interface
- Debugging
 - Time consuming Root-cause analysis

Cadence-Rambus Collaboration

- Fully Integrated and Independently verified PCIe solution
- Highly adaptable, silicon-proven PCIe digital core and Phy IP from Rambus
- Automated and metric-driven VIP from Cadence
- Leverages several years of expertise

Combine configurable, proven design IP with best of class VIP

Combining Best of Breed Design and Verification IP



Concept

Revenue



- **Cadence & Rambus value proposition**
 - Highest quality
 - Fastest time to revenue
 - Lowest risk

Best of Breed PCI Express Solution

- Design IP and VIP independently cross checked
 - Cadence and Rambus models built independently
- Design IP and VIP most tightly integrated
 - Executable verification plan specific to your IP
 - Customized test suite specific to your IP
 - Automated protocol Compliance Management System

Exclusive!

Exclusive!



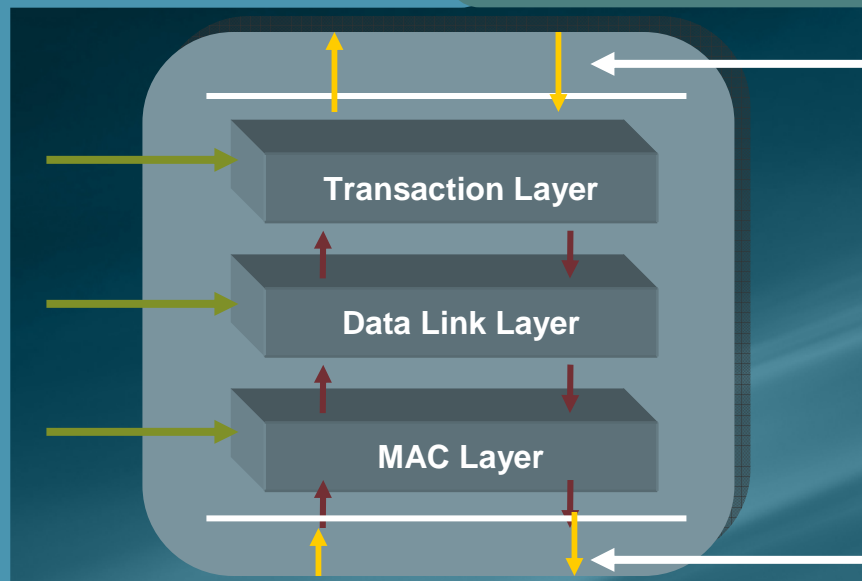
Integrated Environment

Targets Design IP-specific
Functionality

Targets Design IP
Protocol Compliance
and Integration of
Design IP and
Customer Logic

Rambus VIP
(CoverMore)

Cadence VIP
(CMS)



Methodology

- Re-create customer environment
- Maintain Verification independence
- Tool aspects
 - Follow release QA for eVC and Design IP
- Debugging
 - Run regressions at CDN and Rambus
 - Regressions include Cadence + Rambus tests
 - Root-cause analysis
 - VIP/tool anomaly fixes by CDN
 - Design IP anomaly fixes by Rambus

Refinement

- **CDN PCIe compliance vPlan has all features of PCIe**
- **Example - DUT configuration specific features**
 - **DUT acts as End point**
 - **RC related coverage points are disabled**
- **Unsupported PCIe compliance points in the design**
- **Refined vPlan and created required perspective which will load on CDN compliance vPlan**

vManager Regression Session

Incisive Enterprise Manager

File Edit View Analysis Options Help Console eRM Help Support

Export Report Runs vPlan Config Setup DRM Monitor

Start Refresh Read Reload Clear Policy Revert Stop

Sessions Table: Contains 3 sessions

<input checked="" type="checkbox"/>	Status	Session Name	Progress	P	F	R	W	O	Total
<input checked="" type="checkbox"/>		vm_rambus_pcie_sessions.ckappe.07_08_20_22_04_31	<div style="width: 83%; background-color: #90EE90; border: 1px solid #ccc;"></div>	313 [83%]	4 [1%]	0	0	58 [15%]	375 [100%]
<input checked="" type="checkbox"/>		vm_rambus_pcie_sessions.ckappe.07_08_20_22_04_31.ckappe.07_08_21_06_50_05	<div style="width: 69%; background-color: #90EE90; border: 1px solid #ccc;"></div>	40 [69%]	0	0	0	18 [31%]	58 [100%]
<input checked="" type="checkbox"/>		vm_rambus_pcie_sessions.ckappe.07_08_20_22_04_31.ckappe.07_08_21_06_50_05.ckappe.07_08_21_22_30_19	<div style="width: 100%; background-color: #90EE90; border: 1px solid #ccc;"></div>	18 [100%]	0	0	0	0	18 [100%]

HTML File Ready

vPlan Default Perspective

The screenshot displays the vPlan software interface with a hierarchical tree of compliance check lists. The tree is organized into three main categories: 2 Endpoint and Root Complex, 2.1 PCIE_instance no component parameter, and 2.3 PCIE_instance EP. Each category contains several sub-categories, each with a percentage value indicating coverage. The interface also shows the 'vPlan' logo, 'Goal Relative Grade', 'Refinement Mode: local', and 'Perspective: Endpoint and Root Complex, AER = Off, VC 1-7 = Off, Completer Abort = Off, Config Request Retry Status = Off, Poisoning = Off, LTSSM = Passive'.

Default Perspective

Coverage Model for RC/EP/Legacy EP

Root Complex vPlan Tree

End Point vPlan Tree

Category	Sub-Category	Coverage Percentage
2 Endpoint and Root Complex, AER = Off, VC 1-7 = Off, Completer Abort = Off, Config Request Retry Status = Off, Poisoning = Off, LTSSM = Passive	2.1 PCIE_instance no component parameter	25%
	2.1.1 TPL Compliance Check List	15%
	2.1.2 TXN Compliance Check List	13%
	2.1.3 DLL Compliance Check List	52%
	2.1.4 PHY Compliance Check List	33%
	2.1.5 PMG Compliance Check List	30%
	2.1.6 SYS Compliance Check List	15%
	2.1.7 CFG Compliance Check List	13%
2.2 PCIE_instance RC	2.2.1 TPL Compliance Check List	0%
	2.2.2 TXN Compliance Check List	12%
	2.2.3 DLL Compliance Check List	52%
	2.2.4 PHY Compliance Check List	28%
	2.2.5 PMG Compliance Check List	19%
	2.2.6 SYS Compliance Check List	15%
	2.2.7 CFG Compliance Check List	10%
	2.3 PCIE_instance EP	2.3.1 TPL Compliance Check List
2.3.2 TXN Compliance Check List		14%
2.3.3 DLL Compliance Check List		52%
2.3.4 PHY Compliance Check List		42%
2.3.5 PMG Compliance Check List		45%
2.3.6 SYS Compliance Check List		18%
2.3.7 CFG Compliance Check List		17%

vPlan – Loading Rambus Perspective

The screenshot displays the vPlan software interface. At the top, the title bar reads "vPlan" and includes a "Goal Relative Grade" indicator. The main window shows a project tree on the left with various folders and their associated percentages. A dialog box titled "Select Perspective" is open, showing a list of perspectives. A yellow callout bubble points to the dialog box with the text "Loading Rambus Perspective".

vPlan Goal Relative Grade

vPlan: /proj/rmbs_vip/work/ckappe/CDN_REL_1_7/gpex/sim/work_2_3beta3/vplan_file_2_3b3/PCIEvPlan-top-RMBS.xml
Refinement Mode: local
Perspective: Endpoint and Root Complex, AER = Off, VC 1-7 = Off, Completer Abort = Off, Config Request RetryStatus = 0

24% 2 Endpoint and Root Complex, AER = Off, VC 1-7 = Off, Completer Abort = Off, Config Request RetryStatus = Off, Poisoning = Off, LTSSM = Passive

25% 2.1 PCIE_instance no component parameter

15% 2.1.1 TPL Compliance Check List

13% 2 EndPoint, AER = On, VC 1-7 = Off, Completer Abort = Off, Config Request RetryStatus = Off

52% 2 EndPoint, AER = On, VC 1-7 = On, Completer Abort = Off, Config Request RetryStatus = Off

33% 2 EndPoint, AER = On, VC 1-7 = On, Completer Abort = On, Config Request RetryStatus = Off

30% 2 EndPoint, AER = On, VC 1-7 = On, Completer Abort = On, Config Request RetryStatus = On

15% 2 EndPoint, AER = On, VC 1-7 = Off, Completer Abort = On, Config Request RetryStatus = On, Poisoning = On

13% 2 RootComplex, AER = Off, VC 1-7 = Off, Completer Abort = Off, Config Request RetryStatus = Off

13% 2 RootComplex, AER = On, VC 1-7 = On, Completer Abort = On, Config Request RetryStatus = On

19% 2.2 All parameters = On

0% 2.2.1 TPL Compliance Check List

12% 2.2.2 TXN Compliance Check List

52% 2.2.3 DLL Compliance Check List

28% 2.2.4 PHY Compliance Check List

19% 2.2.5 PMG Compliance Check List

15% 2.2.6 SYS Compliance Check List

10% 2.2.7 CFG Compliance Check List

29% 2.3 PCIE_instance EP

12% 2.3.1 TPL Compliance Check List

14% 2.3.2 TXN Compliance Check List

52% 2.3.3 DLL Compliance Check List

42% 2.3.4 PHY Compliance Check List

45% 2.3.5 PMG Compliance Check List

18% 2.3.6 SYS Compliance Check List

17% 2.3.7 CFG Compliance Check List

Select Perspective
[implemented_coverage]

Loading Rambus Perspective

Failure Report - First Failure Description

Runs [1] (First_Failures)

File Edit View Analysis Options

Export Undo Redo vPlan Info Views Lock Close

Chart Rerun Group Filter Add Select Ungroup Unfilter Runs

Runs Grouped by: First Failure Description
 Filtered by: Status == failed

Table: Contains 4 runs in 4 groups (no runs are filtered out)

Run Id	First Failure Description	First Failure Tool	First Failure Kind	First Failure Time	First Failure Log	Top Files	Seed	Status
R00347	ERR_VR_PCIE819_BAD_MAX_PAYLOAD_SIZE_SUPPORTED Invalid value for register In vr_pcie_tl_monitor-@7401 of P_EP TL agent. PCIE Spec : 7.8.3 page 368 Compliance checklist items : CFG.8.3#1 Device: P_EP Packet: vr_pcie_tl_pkt-@7459 Register Name: VR_PCIE_DEVICE_CAPABILITIES Register: VR_PCIE_DEVICE_CAPABILITIES vr_ad_reg-@145 Field Name: Max_payload_Size Supported Cmpl Value: 0 Ref Value: 5 Register value is not as expected	specman	dut_error	6122	local_log.log	.../test_suite_defines .../pio_enum .../vr_pcie_test_suite_top.e .../vr_pcie_test_cfg_read_initial_reqs_value_before_cfg_writ e.e	171979570	failed
R00298	ERR_VR_PCIE333_DLLP_TXD_AFTER_PM_ACK_RXD A DLLP was sent although PMREQ_ACK_DLLP was recieved. DLLPs transmission should be disabled. In vr_pcie_dll_monitor-@7406 of P_EP vr_pcie_dll_agent-@7404. PCIE Spec: 5.3.2.1 page 242. Compliance checklist items: PMG.3.9#6 Sent packet is: vr_pcie_dll_pkt-@7606	specman	dut_error	51526	local_log.log	.../test_suite_defines .../pio_enum .../vr_pcie_test_suite_top.e .../vr_pcie_test_pm_all.e	881853042	failed
R00010	ERR_VR_PCIE339_DLL_FCUPDATE_TIMER UpdateFC timer has expired In vr_pcie_dll_monitor-@7406 of P_EP vr_pcie_dll_agent-@7404. PCIE Spec:	specman	dut_error	79600	local_log.log	.../test_suite_defines .../pio_enum .../vr_pcie_test_suite_top.e .../vr_pcie_test_pl_ltssm_all.e	1577333793	failed

HTML File Ready

Interoperability Efforts



Strategy Managers



TL Engineer



Team Lead

Rambus VIP
(CoverMore)

Cadence
VIP

GPEX
Design IP



Project
Manager



Tool R&D
Engineer



DLL Engineer



Verification
Engineer



Verification
Engineer



Tool R&D
Engineer



MAC Engineer

Huge efforts spent to help the customer integrate IP smoothly

Interoperability Efforts

- **Several man-years worth of efforts**
 - Design IP Development
 - VIP Development
 - Interoperability efforts
- **Tool Licenses**
- **Methodologies**
- **Customer approval**

Rambus and Cadence Collaboration Deliverables

- **Design IP**
 - PCI Express Digital controller, PHY
- **Verification IPs**
 - CoverMore VIP
 - Cadence eVC VIP
 - ✓ PCI Express eVC
 - ✓ Supports e and/or SystemVerilog test benches
 - ✓ PCI Express Compliance Management System
 - ✓ Executable verification plan (vPlan)
 - ✓ Test suite to achieve 70% + coverage
 - ✓ Rambus specific package for Verification
 - ✓ Refinement file for PCI Express vPlan
 - ✓ Additional test sequences to maximize coverage

Summary

Rambus + Cadence collaboration solves IP Integration challenges

- **Independently verified**
 - Independently created models
 - Independently cross-checked
- **Tightest integration of Design IP and VIP**
- **Combined expertise of Rambus and Cadence**
- **Most automated solution**
 - Cadence CMS automates verification
 - Digital core customizable protocol support



Thanks!
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