Casio and Cadence

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The Customer

Casio Computer Co., Ltd. is one of the world's leading manufacturers of consumer electronics products and business equipment solutions. Since its establishment in 1957, Casio has strived to realize its corporate creed of "creativity and contribution" through the introduction of innovative and imaginative products.

In 1995, Casio, developed a digital camera with an LCD display, paving the way for the digital camera of today. The Casio EXILIM, originally launched in 2002, has been well-received for a broad range of sizes, performance, and price points. All are renowned for their ability to shoot images in rapid sequence, with sharp resolution, high-contrast, and true-to-life colors. EXILIM cameras also deliver long battery life.

These capabilities result from the powerful and power-efficient image processing functions performed in the EXILIM camera System LSIs. These SoCs—which typically have millions of gates—perform most of the image capture and processing functions within the camera. The engineers at Casio's Digital Camera Division are responsible for developing these advanced SoCs and are world-class experts with deep experience in algorithm development and architectures for digital cameras.

As process geometries shrink, the maximum performance (i.e., clock speed) of SoCs generally increases, allowing for, among other things, the maximum number of combinational logic elements between shift-registers to grow. This can enable major micro-architecture efficiency improvements—especially for highly pipelined designs, such as those used for image processing applications.

Business Challenges
- Improve product performance while reducing development costs

Design Challenges
- Migrate to a transaction-level modeling (TLM)-driven methodology with high-level synthesis (HLS) capability
- Rearchitect legacy designs to maximize the benefit of new process technologies
- Eliminate the need to manually develop new RTL from scratch

Cadence Solution
- C-to-Silicon Compiler

Results
- Next-generation HLS technology developed at Cadence for production usage at Casio
- Comprehensive design and verification methodologies/flows (specified and developed with Casio engineers) to integrate HLS with the rest of Casio production design flows
- Shorter development time
- 50% reduced debug/verification cycle time

The Challenge

Casio engineers had previously implemented different algorithms and IP blocks using micro-architectures optimized for 130nm. Nonetheless, they wanted to take advantage of new capabilities in the latest process technology to improve performance while reducing area and cost. The question was how. For Casio engineers to rewrite and tailor the legacy RTL code to the new process would have taken a prohibitive amount of time and resources, particularly when many of the engineers who developed the original RTL had since moved to other projects. Using the RTL code designed for old technology would have resulted in unacceptable overhead in area and power. Casio engineers wondered about the capabilities of system-level design/high-level synthesis to resolve these difficulties and significantly improve the reusability of the design for the future. The next question was whether Cadence could help them.

"From working with Cadence on this project we can see how effective system-level IP development can be, and we intend to extend its usage to future projects as we work with Cadence to build a total flow with design and verification."

The Solution

System-level design requires a robust, reliable way to translate high-level descriptions to RTL descriptions. High-level synthesis (HLS) tools had been widely available and tested in Japan since the early 2000s, and many Japanese semiconductor companies, including Casio, were aggressively trying several of these. Unlike many other companies, however, Casio was unwilling to accept the limitations imposed by most HLS tools (which usually relegate them to niche applications). Three major hurdles Casio engineers had experienced were the inability of HLS tools to: separate functionality and constraints (which adversely impact reusability), support low power (e.g., adding effective clock gating), and deliver area results competitive with hand-written RTL.

"We found the Cadence® C-to-Silicon Compiler approach of separating functionality and constraints to maximize reuse, and also the clock-gating capabilities for low power, very interesting," says Masateru Nishimoto, Lead Engineer, QV Digital Camera Division of Casio. "Because the RTL IP elements must be reused across so many designs as well as different process technologies, and because low power is so important, the support for reusability and low power were our paramount concerns."

Putting C-to-Silicon Compiler through its paces

Casio and Cadence engineers decided to test the capabilities of C-to-Silicon Compiler with a key IP block that implemented various image processing and tracking functions. The size of the block was modest—approximately 240k gates. Starting from a serial C/C++ algorithm running purely in software, the Casio/Cadence team partitioned the code and added wrappers to create an implementation-agnostic SystemC® model that C-to-Silicon Compiler could synthesize. The Casio design was a multi-stage pipeline circuit having complex control logic, and the goal was to minimize area while meeting latency, throughput, and power consumption goals. Once the Casio team had fully verified the RTL generated by C-to-Silicon Compiler (vs. the legacy RTL design developed for the old process technology), they integrated it into the rest of the SoC.

"Casio algorithm developers and architects are experts in designing and architecting image processing systems," says Kazuyuki Kurosawa, Section Manager for Casio's QV Digital Camera Division. "But most of them do not like writing RTL very much, and would prefer to use an automation tool if it works well. Therefore, we had high hopes that C-to-Silicon Compiler could match the performance, area, and power consumption of the manual RTL."

A better design sooner, and with less effort

The micro-architecture exploration capabilities of C-to-Silicon Compiler proved extremely valuable to Casio engineers in helping them converge on the optimal micro-architecture. Despite a heavy mixture of control and datapath, the Cadence technology enabled them to try different latency/area tradeoffs and to decide on the optimal architecture within just a few days. Ultimately, the team identified one micro-architecture yielding better area and power than the original hand-written RTL, yet having the same latency and throughput. To do this using a manual RTL approach would have taken several weeks.

The productivity impact was substantial in other respects as well, including faster code development, simulation, and debugging/verification. Due to the higher level of abstraction and fewer lines of code, the synthesizable SystemC code was developed from the original algorithms in less than half the time than would have been required to manually write RTL code. For example, the SystemC code was more compact, averaging one-quarter the number of lines to describe the same functionality as the hand-written RTL. Because C-to-Silicon Compiler delivers at least 5x faster SystemC simulation speeds (and the Cadence verification methodology enables algorithmic testbenches to be shared among the original algorithms, SystemC, and the generated RTL), debug/verification cycle time was also reduced by more than 50%.

The C-to-Silicon automated flow for formal verification using Sequential Logic Equivalence Checking (SLEC) also played an important role in minimizing the debug/verification time. C-to-Silicon Compiler automatically generated scripts for the Calypto SLEC tool, which in one case identified a critical design issue in the communication logic between two different processes in the design—issues inadvertently introduced because of timing/schedule changes during the high-level synthesis process. The problem would have required several weeks to locate and fix using simulation.

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Summary and Future Plans

As a result of this project, Casio engineers obtained new production-quality RTL for highly reused IP, and also learned a new development methodology. And they achieved all this with the same time and effort as would have been required to rewrite manual RTL from scratch. This has convinced Casio to make high-level synthesis a standard approach for RTL development in the future.

The next step going forward will be to develop an enhanced transaction-level modeling (TLM)-driven verification flow based on the industry-standard Open Verification Methodology (OVM), supplemented with C-SystemC and SystemC-RTL equivalence checking. These developments will enable Casio engineers to go beyond just enabling effective high-level synthesis to enabling a comprehensive system-level design solution.

"The digital camera market is extremely competitive and for Casio to maintain its leadership, our engineers must continually focus not just on performance and quality but also on productivity," Kurosawa says. "From working with Cadence on this project we can see how effective system-level IP development can be, and we intend to extend its usage to future projects as we work with Cadence to build a total flow with design and verification."

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