

Cadence Palladium Series with Incisive XE Software

Hardware/software co-verification and system-level verification

The Cadence® Palladium® series of accelerators/emulators is a key component of the Cadence Incisive® functional verification platform. It provides the performance needed to verify embedded software and HW/SW interactions. Palladium systems offer verification speeds of 100 to 1,000,000x faster than RTL simulation alone, fast bring-up time and compile times in minutes. Palladium systems also offer several use models with multi-user capability, remote access, hard and soft IP, and testing with live data through Incisive SpeedBridge rate adaptors.

Palladium Series

The Palladium series consists of three generations of products: Palladium, Palladium II, and Palladium III. They deliver unrivaled speed and support a multi-specialist team approach. With one investment, you get multiple runtime modes along with local and remote access availability for multi-user, multi-project support

Palladium systems provide simulation acceleration and in-circuit emulation in a single system enabling you to achieve first silicon and first software required for successful product delivery.

Simulation Acceleration

Using the industry's most advanced hardware transaction-based acceleration and assertion-based technologies, Palladium systems deliver simulation acceleration performance up to 1,000,000x or more over simulation alone. With Palladium technology, regression runs are compressed from months to hours; overnight tests will complete during a coffee break.

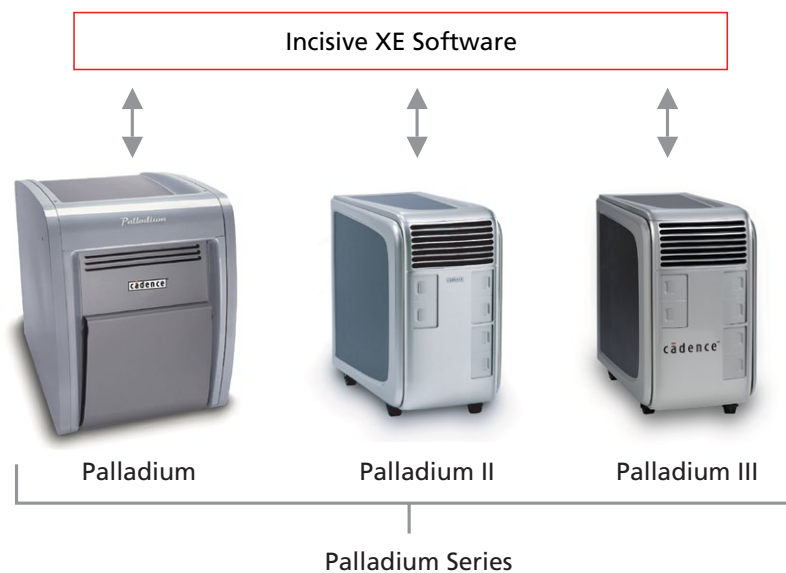


Figure 1: Palladium systems are powered by Incisive XE software

In-Circuit Emulation

For final system verification, in-circuit emulation mode runs up to or more than 1,000,000x faster than simulation on large designs, and it incorporates peripherals, embedded processors, multiple ASICs, and embedded software into a single environment. This level of performance enables the ultimate

goal of SoC verification—comprehensive application-level system and software testing.

First Silicon, First Software

Palladium systems address demanding time-to-market requirements by enabling concurrent, automated, and managed verification of hardware and embedded software. As more and more electronic products have extensive

software content, designers face serious project delays if they wait until silicon is available to begin debugging. It's no longer just first silicon, but first silicon *and* first software that are the key milestones for product delivery.

With Palladium technology, software verification and debugging can begin before silicon is available, often before it is frozen, which can shave months off the software development schedule. Only emulation can provide the performance, debug, and accuracy needed to verify application-level software and hardware prior to first silicon availability.

Palladium III

Compared to earlier generations of Palladium systems, Palladium III demonstrates across-the-board improvements, from runtime performance to automation and verification management. Key enhancements include plan- and metric-driven hardware/software validation, debug productivity, automation, reliability, and, of course, performance. Palladium III raises the bar in terms of reliability, performance, and productivity.

Compared to the first and second generations of Palladium systems, Palladium III offers:

	Palladium III vs. Palladium	Palladium III vs. Palladium II
Average emulation speed	3x	1.7x
Capacity	2x	Same
Density	3x	Same
Debug performance	10x+	Up to 3x
Numbers of I/Os	7x	Same
Numbers of users	2x	Same

Benefits

- Increases verification throughput 100–1,000,000x through simulation acceleration and emulation
- Comprehensively verifies ASIC, SoC, systems, and hardware/software interactions with a real-world environment and/or soft testbench
- Applies advanced metric-driven verification planning to hardware/software

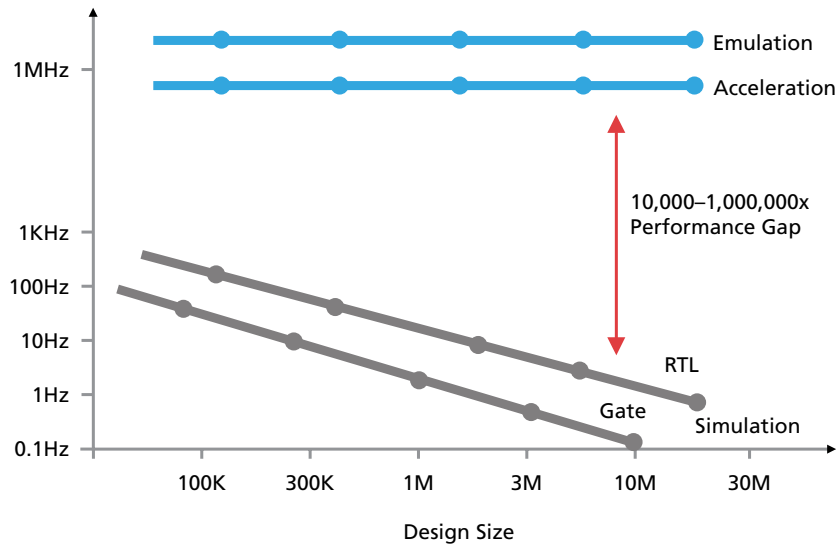


Figure 2: For large designs, in-circuit emulation provides a 10,000–1,000,000x performance increase over simulation

- Provides simulation acceleration and in-circuit emulation in a single system
- Maximizes efficiency with fast compiles on a single workstation
- Delivers 10x the debugging speed over FPGA-based emulators
- Finds system-level hardware/software bugs early and increases system-level quality
- Supports multiple users and remote access

Features

High Throughput and Scalable Capacity

- 100–1,000,000x performance gain over RTL simulation

Palladium systems are massively parallel Boolean compute engines that accelerate verification:

- 10x for a compatible behavioral testbench using signal-based acceleration
- 100x+ with transaction-based acceleration
- 1,000–1,000,000x for embedded testbench acceleration or in-circuit emulation on larger designs

- Compilation at 10-30M gates per hour on a single workstation

Typically, hardware accelerators and emulators require a server farm just to compile a design within one day. Palladium systems use Incisive XE software to compile most designs in less than one hour on a single workstation, dramatically reducing system cost and management overhead cost associated with a server farm. The compiler automatically models memories from your Verilog®, SystemVerilog, or VHDL RTL code including synchronous, asynchronous, and multi-ported memories. The compiler can also calculate runtime performance accurately at the end of the compile process.

- Expandable to 256M gates

Palladium systems have a maximum capacity of up to 256M ASIC gates and 74GB of memory—large enough for the most complex designs of today and tomorrow. With easy capacity upgrades, you can start with the capacity you need now and expand as necessary to meet your future needs.

- Multi-user access

Depending on the configuration, up to 32 users can simultaneously share a Palladium system independently of each other. Palladium systems share the total acceleration/emulation capacity via dynamic reallocation of capacity to users. This is ideal for simultaneous block-level verification by many team members.

Later in the design cycle, as the team assembles blocks of the design into a full chip, they accelerate the entire design simply by allocating more capacity to that user.

Entire organizations can benefit from the Palladium system's multi-user capability. When combined with its remote access capability, a Palladium system can be shared via the corporate WAN as a verification hub, thus providing high-speed access across an entire organization. Merchant semiconductor vendors can even facilitate early design success by offering remote access to design partners via a Palladium system.

- Simple upgrade to in-circuit emulation

When you're ready to verify the entire system, you can upgrade a Palladium base configuration to in-circuit emulation with the simple addition of I/O connection kits. Verification with software and live data in a real-world environment catches bugs and performance issues that cannot be foreseen when writing the testbenches, thus reducing the risk of silicon re-spin.

Superior Debug Environment

- Unified debugging environment

Most of the time spent verifying designs is spent debugging problems, which becomes a time-to-market bottleneck. Incisive XE software provides a unified debugging environment that offers a tightly coupled schematic viewer, waveform viewer, and design/source code browsers. Signal values at a specific point in time can be backannotated onto the schematic and RTL source code can be displayed so you can rapidly trace back through a circuit to find the cause of the observed anomaly.

Taking advantage of custom silicon, Palladium technology has been designed to provide much faster debugging response than FPGA-based emulators. The Incisive XE unified debugging environment has advanced features, including:

- **Integrated logic analyzer:** allows for complex trigger conditions and for changing the trigger condition instantly, using any signal or assertion, without needing to recompile the entire design as in FPGA-based emulators
- **FullVision:** displays any or all signals in the testbench and the design without specifying probes in advance. The system uniquely eliminates downtime by offering full interactive visibility into all tests without having to reset the system or the external interfaces, even if the target is not stoppable. You never need to recompile probes and re-run to see a critical signal during debugging
- **InfiniTrace:** enables unlimited trace capture depth and allows you to revert back to any checkpoint and restart emulation from that point.
- **Save and restore:** allows you to save the debugging state and resume work later
- **Offline debug:** helps you maximize use of the accelerator. You can debug using Incisive SimVision as well as popular third-party tools. Offline debug capability enhances efficient sharing of a Palladium system among users

- Design experiments

Design experiments allow you to make certain design changes and instantly see the results:

- Disable sections of the circuit that are interfering with the section you want to inspect
- Force signals on or off to enable or disable signal effects
- Inject changes into the circuit, including complex time sequences that duplicate the proposed fix, and observe their effect

System-Wide Verification Management

- HW/SW coverage aggregated through Incisive Enterprise Manager
Palladium verification power is amplified when combined with Incisive Enterprise Manager. Enterprise Manager extends

proven hardware plan- and metric-driven verification management to embedded software and system-level verification. Enterprise Manager allows you to capture executable system-level verification plans (vPlans), track and analyze all system-wide verification activities, and aggregate "total" system-level coverage metrics, including assertions, directed tests, and constraint-driven random tests.

These management capabilities result in a much more predictable system-wide verification process, greater utilization of team resources, and much higher hardware, software, and full-system quality. Incisive Enterprise Manager is integrated with the Palladium II and Palladium III environments and includes the following components:

- **Verification plan (vPlan)** for capturing embedded software and system-level verification requirements. Enables automated extraction of coverage information and annotation of progress to the vPlan
- **Optimization of enterprise team resources** through "test ranking," "correlation analysis," and charting of metrics with hierarchical view of hardware, software, and system activities
- **Closure and quality assurance with "total" system coverage** aggregated across hardware, software, and system-level verification activities

Advanced Verification and Automation

- ESL option for Palladium series

The combination of the Incisive Enterprise Simulator ESL option with Palladium systems (Palladium II and Palladium III) enables users for the first time to verify their SoC design and full system, including software, through automation and randomization of embedded software or hardware tests at 100s of KHz performance. The ESL option includes Incisive Enterprise Manager and the Incisive Enterprise Simulator ESL Option, as described below:

- **Incisive Enterprise Manager:** helps the planning and aggregation of the results, and tracks the coverage for both the hardware and the embedded or system-level software
- **Incisive Enterprise Simulator ESL Option:** provides several key capabilities that, when combined with Palladium emulation and Incisive Enterprise Manager, provide a new and powerful means to apply plan- and metric-driven verification methodologies to both hardware and software. New technologies include:
 - **Transaction-based acceleration with Specman Elite® technology:** high-level, object-oriented verification testbench environment that provides intelligent metric-driven stimulus generation for advanced verification. Its new transaction-based methodology helps customers achieve high-speed acceleration with Specman Elite testbenches and Palladium systems
 - **Incisive Software Extensions:** a new technology that allows the Specman Elite environment to apply verification planning and metrics to software. Combined with Specman Elite transaction-based acceleration capability, such metric-driven HW/SW co-verification can be completed at high speed on Palladium systems

- Full testbench language support
Palladium systems feature testbench language support for Verilog, SystemVerilog, VHDL, C, C++, SystemC® Verification Library, and e. You can migrate from system-level modeling to RTL verification and reuse your testbench to verify the accelerated design.
- Assertion-based acceleration
Assertion-based acceleration provides full interoperability by accelerating the assertions through the use of Palladium assertions. This capability allows you to work with any mix of verification engines and standard assertion formats including:
 - Property Specification Language (PSL)
 - SystemVerilog Assertions (SVA)

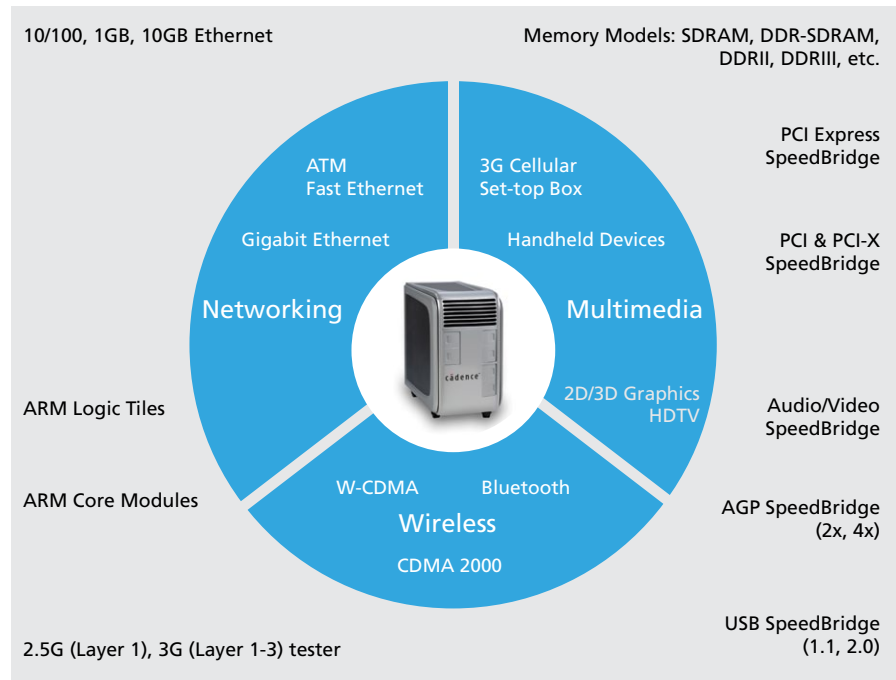


Figure 3: SpeedBridge verification IP provides complete application-specific solutions for verifying complex design

- Open Verification Library (OVL)
- Incisive Assertion Library (IAL)
- Transaction-based acceleration
Transaction-based acceleration (TBA) increases overall acceleration performance and is described in the use models section. Palladium systems can also be used to accelerate fault coverage and code coverage analysis.

Verification IP

- Support for hard and soft IP
Incisive XE software supports both hard IP (physical silicon cores) and soft IP (HDL files) in all use models. It supports HDL files encrypted by IP providers for protection, giving access only to the signals and registers permitted by the IP provider. Bonded-out microprocessor cores, silicon cores, or FPGA logic can be installed into the Palladium IP chassis using Cadence standard IP blocks, making it easy to utilize hard IP during verification.
- Verification IP for in-circuit emulation
SpeedBridge® rate adapters provide an interface to testers and real-world systems. SpeedBridge adapters connect

emulated designs to environments running at 10s of MHz. The following SpeedBridge adapters are available today:

- PCI/PCIX SpeedBridge
- PCI Express SpeedBridge
- Audio/Video SpeedBridge
- Multi-Ethernet SpeedBridge
- SAS/SATA SpeedBridge
- USB SpeedBridge



Figure 4: Universal SpeedBridge chassis

- IP blocks
Palladium systems support hard IP with standard IP blocks through the Palladium IP chassis. Each standard IP block is 100x175mm in size and can have up to

1,248 bi-directional signal pins. Cadence supplies a number of turnkey IP blocks including:

- ARM® Logic Tiles: ARM programmable processor models with connection support to off-the-shelf ARM software debuggers
- Xilinx Virtex-II FPGA for prototyping discrete logic outside the emulator
- Generic pin-grid array for user-mounting of any discrete components

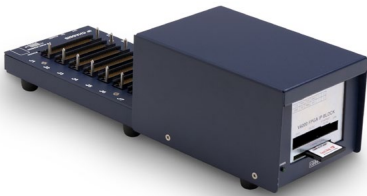


Figure 5: Palladium series IP chassis

- TBA VIP

The Palladium series supports a suite of industry-standard transactors such as PCI Express, Ethernet, AMBA™ AHB, and AXI.
- ABA VIP

The Palladium series supports a suite of industry-standard protocol monitors built from assertions including USB, Ethernet, AMBA AHB, and AXI.

Multiple Use Models for Maximum Value

- Signal-based acceleration

Signal-based acceleration with Palladium systems delivers up to 1,000x performance over simulation and is a natural first step when the need for verification performance increases. The synthesizable RTL and memory models are moved into the accelerator where they run several orders of magnitude faster than on the workstation. Behavioral testbench code continues to run on the workstation.

Because performance can be limited by the behavioral code running on the workstation, the Palladium system utilizes a unique signal-guided synchronization

algorithm that reduces the communication between the workstation and the accelerator. The Palladium system's Incisive XE compiler also synthesizes many behavioral statements, which further improves performance. These technologies greatly increase performance compared with earlier acceleration technologies.

- Transaction-based acceleration

Transaction-based acceleration (TBA) is an acceleration mode that supports a transaction-oriented testbench modeling style. TBA uses message-level communication between the SystemC testbench components running on the workstation and the rest of the environment running on the Palladium system. By using message-level communication rather than signal-level communication, TBA reduces the amount of communication and thereby increases overall acceleration performance.

Unique productivity features, including support for variable length messages, faster streaming mode, and transaction recording, are available with Palladium TBA. Incisive XE software supports a timed modeling style of testbench components in addition to an untimed modeling style. The Incisive Enterprise Simulator has also been optimized to provide high-speed, low-latency communication with the Palladium system, further increasing performance.

- **Congruent TBA:** allows users to create a transaction-based environment without using the hardware. Using only the Incisive Enterprise Simulator, engineers can fully develop their models, optimizing environment bring-up time. Once the models are fully functional, engineers then migrate painlessly to hardware, where these same models will run unchanged at up to **100x faster** than standard simulation. With congruent TBA, results are guaranteed to be the same, regardless of which engine (Incisive or Palladium) is used for execution

- **Concurrent TBA:** allows users to achieve near-emulation performance with designs being driven from a testbench. With this mode, the design runs continuously (free running) at full emulation speed, while the testbench is running on the workstation. This exclusive feature is ideal for running large regression suites, where maximum performance is essential

- SCE-MI-based and SystemVerilog-DPI interfaces

The Palladium series SCE-MI-based interface supports C, C++, and SystemC languages, and it allows testbenches written in these languages to drive the Palladium system directly. The synthesizable RTL is moved into the accelerator. The C/C++/SystemC code running on the workstation is interfaced to the accelerator through the SCE-MI-based interface. This can deliver higher performance than an HDL-based testbench. SystemVerilog-DPI is also available for interfacing SystemVerilog designs to a C, C++, or SystemC model or testbench.

- Vector-based acceleration

Vector-based acceleration is handy when large sets of vectors are used for regression testing of small changes in the design. The vectors may come from simulation, testers, or other sources. Typically, vector regression is used close to tapeout after small logic changes that require verification.

- Embedded testbench acceleration

Embedded testbench acceleration is used when the testbench is written in synthesizable RTL code and the design and testbench are both running in the accelerator at full speed. Writing a synthesizable testbench is worth the extra effort when innumerable cycles are required to verify the circuit, as with processor, networking, and multimedia applications. Embedded testbench acceleration is also used to run computer object code at full speed.

- In-circuit emulation

In-circuit emulation connects the Palladium emulator to a prototype of the system you're designing. Palladium

systems typically replace the ASIC(s) being designed for the target system, enabling system-level and application software testing prior to silicon availability. In some simple environments, the target system may be a piece of test equipment (such as a network tester) that generates and/or verifies test data. When the target system is static, the Palladium emulator can start and stop the clocks, enabling a software debugging-like paradigm—running the emulator for a time, stopping on a defined condition, inspecting the circuit and memory states, and then running again.

- HW/SW co-verification

Emulation alone provides the performance necessary to run and debug application-level software against the chip or complete system. Teams can fully verify embedded software while waiting for first silicon, thereby shrinking the development cycle dramatically. Running software prior to tapeout finds bugs and performance issues that can be fixed optimally in silicon, rather than patched into the software later.

Palladium systems offer unique support for dynamic targets—essential for JTAG connections to software development environments—while still incorporating high performance FullVision into the ASIC. Palladium systems have already been tested with most software development environments, including Motorola Metrowerks, Wind River, TI Code Composer, Green Hills, PowerTap, ARM AXD, and ARM RVD. Incisive Software Extensions (ISX), part of the Incisive Enterprise Simulator ESL Option, can automate HW/SW co-verification scenario creation.

State-of-the-Art Technology

Palladium processor-based technology provides some unique capabilities. Compile speed is reduced to minutes. Debug productivity is high, even on the largest designs. Palladium systems are capable of handling a large number of asynchronous clocks without suffering a performance impact. They can instantly probe new signals and change trigger conditions without requiring re-compilation, which greatly improves the interactivity of

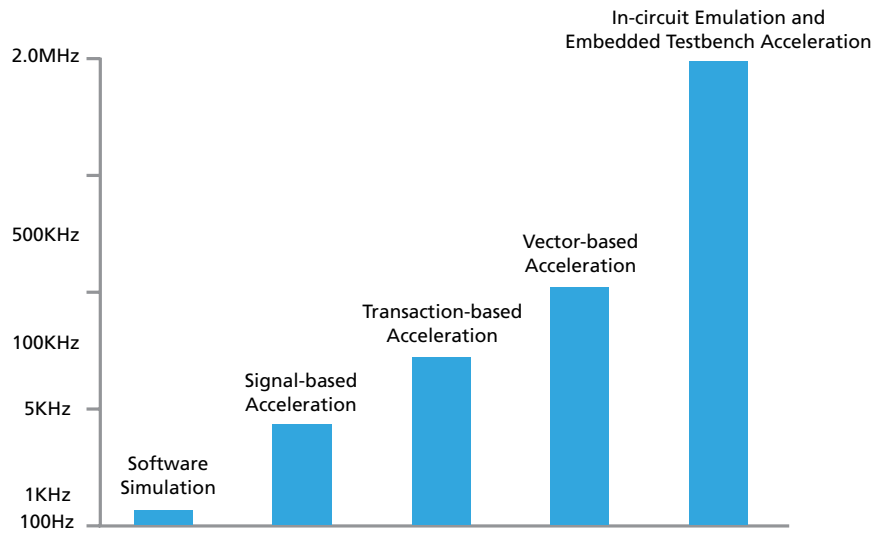


Figure 6: Multiple use models accelerate verification at every stage

debugging. Palladium systems also offer precise control over I/O timing, which may be crucial for target environment interfacing. And with a unique ability to support JTAG ports for software debuggers while using FullVision for the hardware, Palladium systems deliver the highest speed for HW/SW co-verification. Consistently delivering many design turns per day, Palladium systems dramatically reduce time to market for new products and increase revenue.

Specifications

Two Configurations

Palladium systems come in two configurations. *Fully licensed* systems come with all physical capacity already enabled. *License-expandable* systems come with physical capacity that is partially enabled. Additional domains of capacity can be enabled with “always-on” licenses. Your incremental capacity needs for a week or a month can be met by purchasing licenses with a Cadence eDA Card (subject to physical capacity available).

Flexible Allocation of Capacity

Palladium systems allow the total capacity to be dynamically allocated among users in “domains.” For example, if nine domains are available in a system, user A can use two domains for simulation acceleration while user B runs in-circuit emulation of a larger design with the other seven

domains. When both are finished, user C might use all nine domains for an even larger design.

	Palladium	Palladium II	Palladium III
Maximum capacity	Up to 128M gates	Up to 256M gates	Up to 256M gates
Domain capacity	1M gates	1.8M gates	1.8M
Domains per board	8	9	9
Gates per board	8M	16M	16M
Memory per board	4GB	4.6GB	4.6GB
Maximum speed	750KHz	1.5MHz	2MHz

In-Circuit Target System Connections

Palladium systems allow easy interfacing to virtually any target environment. They provide direct support for all popular signal interfaces and have a vast number of I/O pins to support even the largest multi-user environments. When interfacing to the real world, it is sometimes necessary to control the relative timing of individual output signals from the emulator. A DRAM memory interface is one such example— all the address lines must be stable before asserting write enable. Palladium systems reduce emulation bring-up time with a unique output timing control feature that allows each emulator output to be precisely and independently

adjusted to accommodate varying setup and hold timing requirements. Input timing can be similarly controlled.

	Palladium	Palladium II/III
Maximum I/O pins	8,448	61,440
I/O pins per cable	88	192
I/O pins per kit	352	192
Cost per pin	1X	1/3X
Logic levels supported	CMOS3.3V, 5V	CMOS3.3V, 2.5V, 1.8V, 1.5V, LVDS, HSTL, SSTL
I/O timing resolution	7.5ns	5.3ns

Flexible Clocking

Palladium systems support both internally generated and externally supplied clocks. Palladium systems utilize unique algorithms that enable them to handle any number of synchronous, asynchronous, and gated clocks, either internal or external, while maintaining high levels of performance. When used for simulation acceleration, a variety of simulator synchronization techniques are available to maximize performance over conventional lockstep synchronization.

Simulation Acceleration Kits

Simulation acceleration kits provide a high-bandwidth, low-latency connection between Palladium hardware and a PCI- or PCI Express-compatible workstation. Each simultaneous user needs one kit. A maximum of one kit can be connected to each domain.

Workstation Requirements

In addition to simulation acceleration connections to individual workstations, each Palladium system uses a host workstation. This host is connected via high-speed connection(s) handling the bulk data transfers to and from the Palladium system. On larger Palladium systems, the first two simulation acceleration connections require 3.3V PCI slots in the simulation workstations; additional connections require a 5V PCI slot. The host computer must also have an RS-232 or RS-422 port capable of at least 56Kbits/sec. For designs greater than 20M gates, workstations require 350MB RAM for each million gates of design size. For designs less than 20M gates, workstations require 200MB RAM for each million gates of design size with a minimum of 2GB.

	Palladium	Palladium II/III
Simulation acceleration communication channel	3.3V PCI slot	3.3V PCI slot
Palladium to host workstation	FibreChannel one 3.3 or 5V PCI slot	FibreChannel and gigabit Ethernet: two 3.3 or 5V PCI/PCI Express slots

Operating System Support

- Sun Solaris (32-bit, 64-bit)
- Linux PC (32-bit, 64-bit)
- HP-UX (32-bit)

Cadence Services and Support

- Cadence application engineers can answer your technical questions by telephone, email, or Internet—they can also provide technical assistance and custom training
- Cadence certified instructors teach more than 70 courses and bring their real-world experience into the classroom
- More than 25 Internet Learning Series (iLS) online courses allow you the flexibility of training at your own computer via the Internet
- Cadence Online Support gives you 24x7 online access to a knowledgebase of the latest solutions, technical documentation, software downloads, and more



Cadence is transforming the global electronics industry through a vision called EDA360. With an application-driven approach to design, our software, hardware, IP, and services help customers realize silicon, SoCs, and complete systems efficiently and profitably. www.cadence.com