



CADENCE AND RENESAS ENHANCE PRODUCTIVITY WITH NEW SYSTEM-LEVEL DESIGN APPROACH

Industry leaders join forces to move next-generation EDA technology from the lab to the real world

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Osamu Tada, Senior Chief Engineer of Design Technology Division, Renesas Technology Corp.

CORPORATE PROFILE

- One of world's largest designers and manufacturers of LSIs and SoCs for mobile phones and automotive applications

DESIGN CHALLENGES

- Migrate Renesas engineers to a new system-level design methodology based on next-generation high-level synthesis (HLS)
- Demonstrate significant productivity improvements in creation and retargeting of RTL designs

CADENCE SOLUTIONS

- Two-year R&D partnership with Renesas engineers to adapt HLS technology developed at Cadence for production usage at Renesas

- Next-generation Cadence HLS technology tailored and refined for real production based on feedback from Renesas engineers
- Comprehensive design and verification methodologies/flows specified by and developed with Renesas engineers in order to integrate HLS with other Renesas production design flows

CADENCE PRODUCTS

- Cadence C-to-Silicon Compiler

Renesas Technology Corp., a joint venture of Hitachi, Ltd. and Mitsubishi Electric Corporation based in Tokyo, is one of the largest manufacturers of highly integrated SoCs. Like most companies in the semiconductor industry, Renesas faces tremendous business pressures coming from a number of directions—challenges such as accurately getting complex specifications of the application, verifying the system with software, and dealing with shorter market delivery windows. The spec-to-RTL design stage consumes the most engineering resources. These considerations motivated Renesas engineers to seek ways of starting the design process from a high level of abstraction.

EVALUATING THE POTENTIAL OF HIGH-LEVEL SYNTHESIS

The task of finding a solution fell to the System-Level Design and Verification Technology Department (SLDVTD), Design Technology Division, Design and Development Unit at Renesas, whose mission is to improve quality and efficiency for IC front-end design by identifying promising new EDA technologies, and getting such technologies adopted into Renesas design groups.

A key requirement for system-level design is having a robust and reliable way to translate high-level descriptions to RTL descriptions. High-level synthesis (HLS) tools have been widely available and tested in Japan since the early 2000s, and many Japanese semiconductor companies were aggressively trying several of these. The Renesas SLDVTD was no exception. However, unlike many other companies, Renesas was unwilling to accept the typical limitations imposed by other HLS tools that usually relegate them to niche applications. Two major hurdles Renesas engineers kept coming up against were the inability of HLS tools to synthesize designs with complex control or to support incremental synthesis/engineering change orders (ECOs).

Renesas had looked at HLS technologies from many different vendors during previous years, and Cadence® C-to-Silicon Compiler was the first technology Renesas had seen that purported to not only synthesize both control and datapath designs but to also support incremental/ECO synthesis. Cadence engineers explained to their counterparts at Renesas that these capabilities were made possible by embedding logic synthesis within C-to-Silicon Compiler for better timing estimates, and by creating a Behavior Structure Timing (BST) database that would track the underlying design changes during the synthesis process.

“We examined many HLS tools in the early days and were disappointed with the quality of results and the support for incremental synthesis. When we were presented with Cadence C-to-Silicon Compiler technology in early 2005, we thought this could be the solution for our requirements,” said Osamu Tada, Senior Chief Engineer of Design Technology Division, Renesas Technology Corp.

PARTNERING FOR A COMPLETE SYSTEM-LEVEL DESIGN SOLUTION

Having found what appeared to be the most promising HLS technology wasn't the only reason Renesas decided to partner with Cadence. Cadence was also capable of offering a complete TLM-to-GDSII implementation flow under one roof. Renesas saw major potential value in trying to apply promising new HLS technology to “real” projects. However, to minimize the risk, they wanted to be assured of receiving a high level of support.

According to Osamu Tada, “Cadence provides a comprehensive portfolio of EDA tools and services. We were not so interested in a point tool, but saw the potential to work with Cadence for a complete system-level solution. So we were very open to a long-term partnership with Cadence.”

The Cadence team was eager to have C-to-Silicon Compiler applied on real projects and, in the process, learn all that was needed to turn C-to-Silicon Compiler into a commercially viable, mainstream solution. Both companies saw potential for huge rewards, and their mutual trust and respect made them decide to work together.

PUTTING C-TO-SILICON COMPILER TO THE TEST

Renesas and Cadence engineers decided to test the capabilities of C-to-Silicon Compiler with two “shadow projects,” using real Renesas production designs. In essence, they duplicated parts of a real production design and applied C-to-Silicon Compiler to those aspects of the design in a parallel shadow project. This would allow the real project to realize substantial cost and schedule benefits if C-to-Silicon Compiler was successful, while also eliminating downside risk.

THE FIRST TEST: IMAGE PROCESSOR

Starting from a paper specification, the Renesas-Cadence team created a SystemC® model with the goal of completing the RTL for an image processor design within one month, and RTL verification a month later.

Their design was a multi-stage pipeline circuit, and the goal was to minimize area while meeting latency, throughput, and frequency goals. The circuit contained a relatively simple input/output protocol, including one synchronous reset, one asynchronous reset, and a pipeline stall signal. Despite the mixture of control and datapath, Renesas engineers were able to explore latency-area tradeoffs using C-to-Silicon Compiler and decide the optimal architecture within just half a day.

Not only did Renesas engineers succeed, but their design actually ended up having smaller area compared to what would have been expected from handmade RTL (based on a similar design) and shorter latency as well. Renesas engineers were also more efficient than originally expected. The number of lines in the SystemC design description turned out to be much smaller than the equivalent functionality described in RTL Verilog®, and the SystemC simulation runtime was commensurately shorter.

The Renesas team was so pleased with the results that they decided to use the C-to-Silicon Compiler-generated RTL on the real project instead of the hand-coded version. Later in the project, when it was necessary to explore other architectures to meet additional requirements, the Renesas team was able to make the necessary changes to the input SystemC source code and verify there was no adverse impact on the design—all within two days, using equivalence checking. Renesas engineers estimated that if they had been working with manually created RTL, those design changes and subsequent verification activities would have taken about five times longer.

THE SECOND TEST: MEDIA PROCESSOR

On this design, Renesas engineers started with just algorithmic C code not initially intended for HLS. Their design was a pipeline circuit similar to the first test case, with the goal of minimizing area while satisfying their latency, throughput, and frequency constraints. This function in particular contained many loops and Renesas engineers expected to have a sophisticated parallel processing implementation in order to meet their performance target.

Despite a few challenges requiring some minor enhancements to C-to-Silicon Compiler, the tool's performance exceeded the team's expectations. Using C-to-Silicon Compiler, the team was able to rapidly synthesize a circuit that satisfied the multi-hundred MHz performance target with acceptable area.

"Our designs stretched the capabilities and maturity of C-to-Silicon Compiler a great deal, in many ways. Yet we were very impressed with the tool's performance and enjoyed working with it. Our team provided a lot of feedback and requests for enhancements, and we improved the tool with Cadence R&D through a very tight collaboration. As a result, C-to-Silicon Compiler matured very much in a short time," said Osamu Tada.

CURRENT AND FUTURE IMPACT

The collaboration between Renesas and Cadence engineers allowed identifying and addressing broader system-level design methodology issues. These included ways to support simulation-based verification by identifying the manual tasks to prepare the verification wrappers for the C-to-Silicon Compiler-generated RTL (later versions of the tool generate these wrappers automatically).

Renesas engineers also helped identify the types of RTL assertions C-to-Silicon Compiler should produce to support a verification flow. Finally, the team worked to create a verification flow using Sequential Logic Equivalence Checking (SLEC) by specifying what SLEC scripts C-to-Silicon Compiler should produce automatically, plus any manual tasks associated with creating those scripts.

All of these efforts helped Cadence and Renesas to go beyond just enabling an effective high-level synthesis point tool—it allowed them to focus on enabling a comprehensive system-level design solution. Today, both companies are collaborating on integrating transaction-level models (TLMs) with C-to-Silicon Compiler Fast Hardware Model (FHM) generation to enable a seamless system-level design and verification flow, from algorithm to implementation. They are also working together to enable "power-aware" micro-architecture exploration and synthesis to allow system-level tradeoffs among power consumption, cost, and performance.

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