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Interview: By Popular Demand—SystemVerilog Open Verification Methodology

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This week, Cadence and Mentor Graphics announced that the new Open Verification Methodology for SystemVerilog is available for download. To understand the relevance of the announcement, we talked to Tom Anderson, Cadence Verification Product Marketing director; Mike Stellfox, Cadence Verification Solutions Architecture team lead; and Erik Panu, Cadence Incisive Plan-to-Closure Methodology and Verification IP Development group director.

cdnusers: We've been hearing about OVM as an interoperable methodology for a while. Can you describe what OVM is and what it does?

Erik: OVM, which stands for Open Verification Methodology, is a SystemVerilog methodology that we created in collaboration with Mentor Graphics to help the industry establish a framework for companies to create interoperable Verification IP. It was first announced in August. We have been working hard since then to iron out the details and to create a scalable joint product that is now available to the market.

Tom: Basically, it's a tool-independent methodology for designers and verification engineers that promotes SystemVerilog interoperability with a standard library.

cdnusers: Why did Cadence and Mentor decide to collaborate on a standardized methodology?

Tom: It's what our customers wanted. Before the introduction of OVM, Cadence had the Universal Re-use Methodology (URM) and Mentor had the Advanced Verification Methodology (AVM). Synopsys and other companies had their own proprietary methodologies.

EDA users felt this was not a very effective way for the industry to promote the use of SystemVerilog. As a standard universal language, SystemVerilog had the promise of unifying a lot of things, but what users found was that, because each vendor had its own methodology—and that methodology was tied to its own simulator—it really was not effective to use a standard language.

Users want to have support across multiple tools and multiple simulator platforms. As a supplier, it's hard to disagree with that. When we approached Mentor about the concept of a standardized methodology, we realized that our philosophies on what constitutes a methodology were pretty well aligned.

Erik: From my experience in verification, this is the single biggest response from our customers I have ever seen. There is clear demand for this solution.

cdnusers: How does this affect current Cadence SystemVerilog users who are using URM?
Erik: The transition is very straightforward. The feedback we got from our early access partners was "wow"—this is very stable and practically identical to what we were doing with URM. So, on one level, it means Cadence customers are getting what they already had as well as leverage into a new domain with other partners. They get multiple language interoperability with e and SystemC as well. So OVM is a very good bridge from SystemVerilog to other languages.

Mike: That did not happen accidentally; it was by design. From the beginning, we wanted to make sure that, as much as possible, we could maintain backward compatibility for our users. Because OVM is a layered methodology, we were able to ensure the layer for building reusable verification IP for Cadence URM users was familiar. For Mentor AVM users, the class-based library maintained a similar level of backward compatibility.

cdnusers: Were any other companies involved in defining or verifying the OVM release?
Erik: Yes; our primary goal was to work with both customers and partners who make verification IP as well. Both Mentor and Cadence customers have put the open source code to the test.

Tom: We found our verification partners were very happy when we introduced the idea of OVM to them. In some ways, they have an even tougher job than our mutual customers, because they have to produce verification IP that works with all simulators and all different methodologies. They are faced with different verification IP for the three major methodologies—so the idea that they could reduce that number by a third and have only two methodologies out there to support was very exciting to them. They have been very much a part of this process, both establishing and validating OVM.

cdnusers: Is it fair to say that OVM is all that's required to be successful with SystemVerilog verification of complex chips?
Tom: OVM is an absolutely essential part of developing a SystemVerilog verification environment and sophisticated testbench reusable IP, but it is not everything. There is a lot more that is needed to be successful in the verification of a large chip.

To be successful, you really have to look at the overall verification solution. In the Incisive platform there are planning and management tools. There is the Specman e environment, which interacts with the OVM environment for multi-language verification. There are special SystemVerilog techniques oriented toward designers so that their testbenches interact with chip-level OVM testbenches. There is formal analysis, a rich assertion-based verification methodology, and many different aspects of the verification solution that surround, enhance, and complement the OVM

libraries.

So again, the OVM library is absolutely essential, a critical part of the process, something we have put a great deal of effort in, but, in fact, Cadence offers a much broader solution to solve verification problems.

Mike: Talking to customers today, they say that while building a good reusable constrained-random coverage-driven testbench is an essential part of their verification flow, it is not the full solution to verifying large, complex chips. So, not only are we providing these different technologies, we have included OVM within the Plan-to-Closure Methodology, which prescribes a set of flows spanning formal analysis through simulation and testbench techniques including OVM and URM through system-level concern including transaction-level models, hardware/software co-verification, leveraging emulators for verifying large systems, and so forth. We are really looking at OVM in the context of the solution and flow that is driven from a verification plan with very much a metric-based approach to achieving closure of verification

cdnusers: Who will benefit most from OVM?
Mike: Anyone who is interested in adopting SystemVerilog for building or leveraging reusable coverage-driven verification IP that will run consistently across multiple vendor simulators will benefit, as well as anyone who has been using eRM and would like to share or reuse SystemVerilog VIP. OVM will enable design and verification engineers to choose the verification language that best fits their needs (SystemVerilog or e) while still ensuring plug & play VIP across languages.

Tom: In terms of the relevance of OVM to the Cadence customer base we expect it will be very important to verification engineers who are responsible for verifying large chips or portions of large chips. Certainly, some logic designers will benefit as well.

cdnusers: OVM is now available on the ovmworld.org **Web site.**
Erik: Yes, in the download you get the open source for the class libraries and also the methodology examples and the reference documentation for OVM. It is true open source, so it is available to anyone.

Tom: There is no screening process, when you download, you enter your e-mail address—it is strictly an automatic process. You click to accept the Apache 2.0 license and get the download. The only restriction on the Apache license is that users need to maintain the copyrights source code notice, so everyone knows where the material is derived from.

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About the authors

Tom Anderson Biography

Tom is a Product Marketing director at Cadence; his responsibilities include formal analysis, assertion-based verification, and SystemVerilog. His previous positions include Director of Technical Marketing in the Verification Group at Synopsys, Vice President of Applications Engineering at 0-In Design Automation, and Vice President of Engineering at Virtual Chips. He holds an MS in Electrical Engineering and Computer Science from MIT and a BS in Computer Systems Engineering from the University of Massachusetts at Amherst.

Erik Panu Biography

Erik serves as Group Director for Cadence verification IP and methodology. He is responsible for the development and productization of Cadence Universal Verification Components (UVCs), which include simulation, formal, and acceleratable verification IP and the Incisive Plan-to-Closure Methodology. Erik has more than 15 years of professional experience in verification and holds a B.S. and M.S. in Computer Science from the University of Georgia. He can be reached at erik@cadence.com.

Mike Stellfox Biography

Mike joined Cadence in April 2005 as the Group Director of the Verification Technical Field Organization. He came to Cadence with the Verisity acquisition. He was with Verisity since 1998 in a variety of technical management positions. Prior to joining Verisity, he worked at Viewlogic as an Applications Engineer. He began his career at IBM, where he was an ASIC Design Engineer responsible for the design and verification of 2D and 3D graphics chips. Mike holds a Bachelor of Science degree in Electrical Engineering from the University of North Carolina at Charlotte. Mike can be reached at stellfox@cadence.com.