NAND Flash Datasheet

NAND Flash PHY IP

Overview

Cadence IP Factory delivers custom, synthesizable IP to support specific design requirements.

The **Cadence NAND Flash PHY IP** is an all digital, soft PHY with a DFI 2.0, or FIFO interface, controller interface. It also has a register interface for setup, configuration and calibration external register interface.

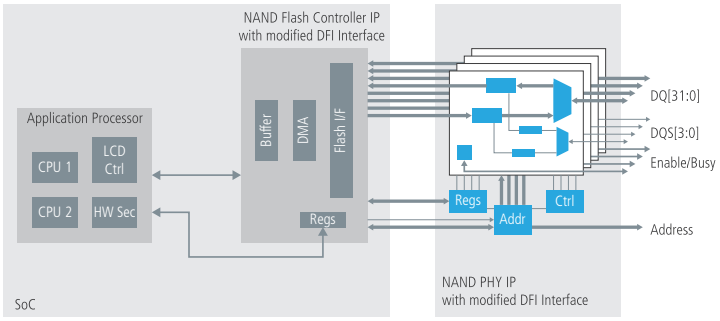

Figure 1: System Level Block Diagram

The **Cadence NAND Flash PHY IP** supports ONFI 3, 2 and Toggle 1,2 interfaces, as well as legacy asynchronous interfaces. It is compatible with all major NAND devices, and supports a bypass mode to support legacy asynchronous devices within a single interface. The **Cadence NAND Flash PHY IP** is scalable from one to four 8-bit channels.

The **Cadence NAND Flash PHY IP** is architected to quickly and easily integrate into any SoC, and to connect seamlessly to the **Cadence NAND Flash Controller IP**, or a third party NAND Flash controller that supports either a DFI 2.0 interface modified for NAND, or a FIFO interface. Implemented for the most popular fabs and processes, the **Cadence NAND Flash PHY IP** provides a cost-effective, low power solution for demanding applications. It offers SoC integrators the advanced capabilities and support that not only meet, but exceed the requirements of high-performance designs and implementations. The **Cadence NAND Flash PHY IP** supports speeds up to 300MHz (100MHz over current specifications), and is structured so that future clock rate increases can be easily accommodated.

The **Cadence NAND Flash PHY IP** offers an automated design flow with advanced synthesis and static timing analysis (STA) scripts that permits RTL-to-placed gates in as little as four hours.

Based on our DDR DRAM PHY design, the **Cadence NAND Flash PHY IP** is silicon proven, and has been extensively validated with multiple hardware platforms. **Cadence IP Factory** offers a comprehensive IP solution that is in volume production, and has been successfully implemented in more than 400 applications.

Key Features

- DFI 2.0 interface modified for NAND or FIFO interface
- Register interface for PHY programming
- Supports asynchronous, ONFI 1,2,3, and Toggle 1,2 devices
- Integrated DLL supports speeds up to 300MHz (100MHz over current specifications)
- High-performance design using standard tool implementation flows
- Slice-based architecture supports one to four channels
- Full digital implementation
- Advanced test-mode capabilities, BIST, Loopback, DFT

Product Details

The **Cadence NAND Flash PHY IP** is based on the proven **Cadence Mobile DDR PHY IP** design, and has been widely deployed across a range of silicon nodes.

PHY Architecture

For total control over the NAND Flash interface implementation, the **Cadence NAND Flash PHY IP** provides complete flexibility with process, library, floorplan, I/O pitch, packaging, metal stack up, routing and other physical parameters.

The **Cadence NAND Flash PHY IP** is implemented with a slice based architecture, which supports up to four 8-bit channels.

Data Slice

The Data Slice is an 8-bit wide design that interfaces to the data, and control connections of the NAND Flash. Each Data Slice connects to an Address/Control Slice, which is also provided. The Data Slice and the Address/Control Slice are duplicated as many times as necessary to create the appropriate data width.

NAND Flash Controller and Register Interfaces

The NAND Flash Controller Interface is compliant to DFI 2.0 with NAND modifications. A FIFO based interface is also available for controller applications that organize commands, but require all device timing to be handled by the PHY.

The Register Interface is a Cadence Proprietary interface to access the Data Slice registers, for configuration, calibration and test modes.

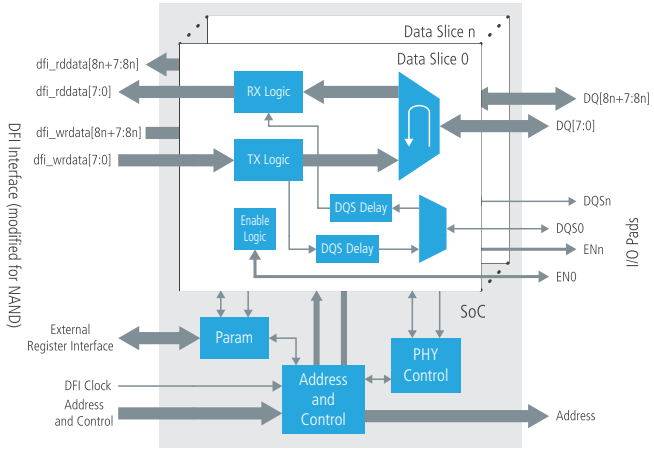

Figure 2: IP Level Block Diagram

PHY Control Block

The PHY Control Block provides initialization and control logic for the Data Slices.

Cadence IP Factory

Cadence IP Factory can deliver various configurations of **Cadence NAND Flash PHY IP** to meet your design requirements. With 10+ years of experience and 400+ successful designs in process nodes ranging from 180nm to 22nm, **Cadence IP Factory** solutions have been proven in everything from low-power MP3 players to leading edge supercomputers.

For more information, visit http://www.cadence.com/solutions/dip/memorystorage/nand_flash_phy/

Benefits

- High performance with extremely low area and low power
- Highly integrated IP speeds system integration and reduces design costs
- Wide support of standards enables system flexibility
- Configurability ensures the perfect fit for your design

Related Products

- NAND Flash Controller IP

Deliverables

- Clean, readable, synthesizable Verilog RTL
- Synthesis and STA scripts
- Documentation – Integration and User Guide, Release Notes
- Verilog testbench with memory model, configuration files, and sample tests

Available Products

- NAND Flash PHY IP

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