



CADENCE AND STMICROELECTRONICS

STMicroelectronics Employs Xtreme Verification and Significantly Shortens Simulation Cycles of Extremely Advanced Telecom Chip

“The methodology supported by the Incisive Xtreme verification system works very effectively in our environment. It boosts our productivity by minimizing errors, facilitating setup. It allows us to accelerate our verification process with the performance of hardware and the flexibility of software.”

Remi Francard, *Project Leader, Cellular Infrastructure Division, STMicroelectronics*

CORPORATE PROFILE

- STMicroelectronics is a leader in developing and delivering semiconductor solutions across the spectrum of microelectronics applications

DESIGN CHALLENGE

- Verify a 100-million-transistor IC on a tight schedule using existing verification environment

CADENCE SOLUTION

- HW-based verification system

CADENCE PRODUCTS AND SERVICES

- Incisive® Design Team Xtreme series

The world’s leading supplier of application-specific analog ICs and a major driving force in advanced System-on-Chip (SoC) technologies, STMicroelectronics provides semiconductor solutions across the spectrum of microelectronics applications.

STMicroelectronics’ Cellular Infrastructure Division needed to verify a tremendously complex baseband modem chip for use in customers’ UMTS base stations. The 100-million-transistor IC features two internal DSPs and an ARM 926EJS CPU. ST’s verification team was facing several challenges, including:

- An extremely tight schedule, which did not permit the team to develop all the tests from scratch. The existing verification environment had to be re-used.
- In addition, the hardware and software had to be verified in parallel to meet the schedule.

- The integration design of the software using a simulation-based environment was problematic.
- The mapping effort had to be small to secure benefits from the project schedule.

THE SOLUTION – XTREME HW/SW CO-VERIFICATION

Design and test engineers at ST’s Cellular Infrastructure Division decided to try the Incisive Xtreme system for hardware/software co-verification. They integrated the ARM Instruction Set Simulator into the environment to take advantage of the co-verification debugging capabilities.

“The methodology supported by the Incisive Xtreme system works very effectively in our environment,” said Remi Francard, project leader at STMicroelectronics’ Cellular Infrastructure Division. “It boosts our productivity by minimizing errors, facilitating setup. It

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communication between our hardware and software people. By connecting the traditionally separate techniques of simulation and emulation, the tool significantly contributes to improving the efficiency of system verification."

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NEW APPROACH HAS MULTIPLE BENEFITS

Xtreme is a versatile verification system that supports simulation acceleration and emulation. The system has fit well into ST's environment and delivered immediate results. Xtreme delivers:

- **High performance** - runtime performance of up to 500K cycles/second. The Cadence XoC coverification environment provided a unified toolset for hardware and software engineers to verify and debug the ARM microprocessor, resulting in an increase of run performance by more than a factor of 1000.
- **Flexible debug** - maximum parallel processing through its patented ReConfigurable Computing (RCC) technology. As a result, system verification delivered software simulation at the speed of hardware emulation. The Xtreme system's VCD-

on-Demand functionality extracts all node history values without resimulation, thereby taxing computing resources far less and making debug much faster.

- **Fast bring-up** - shortened simulation lead time. When a new RTL model of the chip was released, one designer spent less than a week to complete the setup and start the debug operation running again. The set up was reduced from three weeks to less than two days. In this short amount of time, ST was able to run system tests, focusing on the verification task.

The Xtreme system demonstrated the benefits of an integrated continuous flow from RTL to hardware-based verification. Right from the start, ST was able to accelerate parts of the circuit. The flow allowed small and simple iterations to port the full environment of verification to hardware without impacting the continuous verification effort in parallel.

"The Xtreme tool was a breakthrough for our design process. It fit extremely well into our design environment and allowed us to close design verification in a very short time," said Francard. "The co-verification debugger really facilitated

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